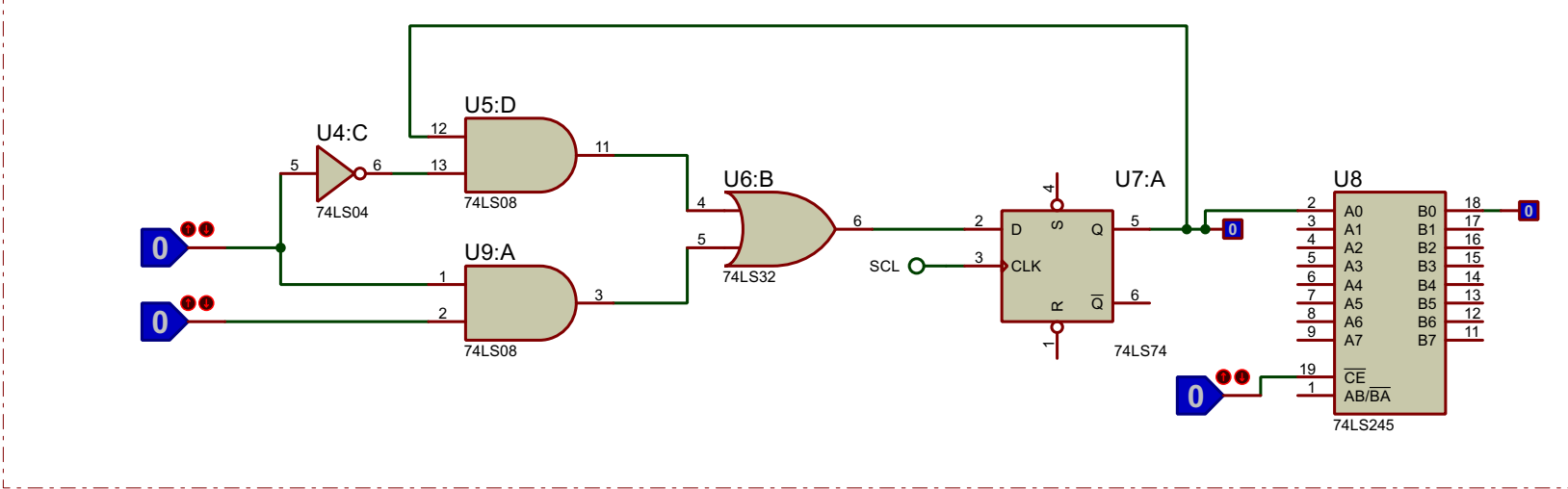
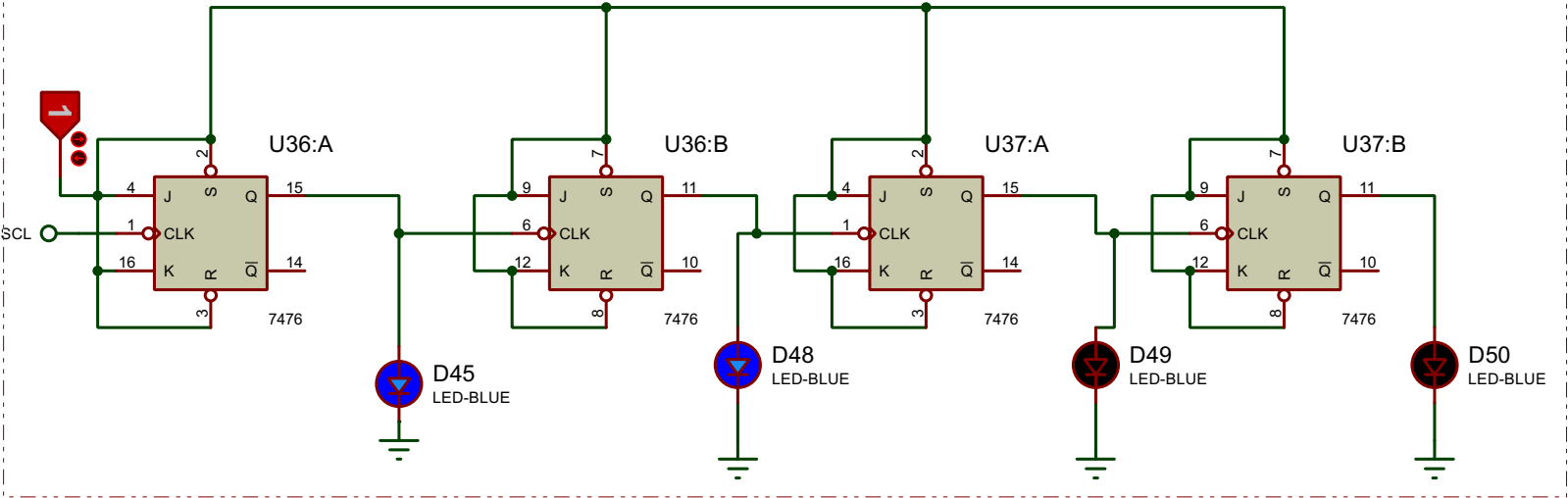


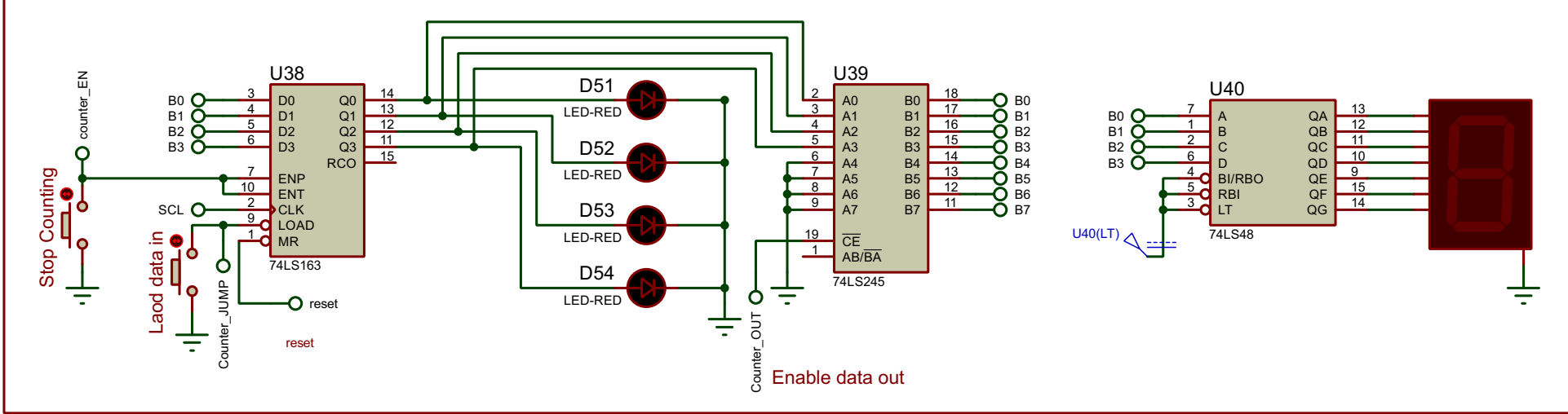
Model of regestor Design



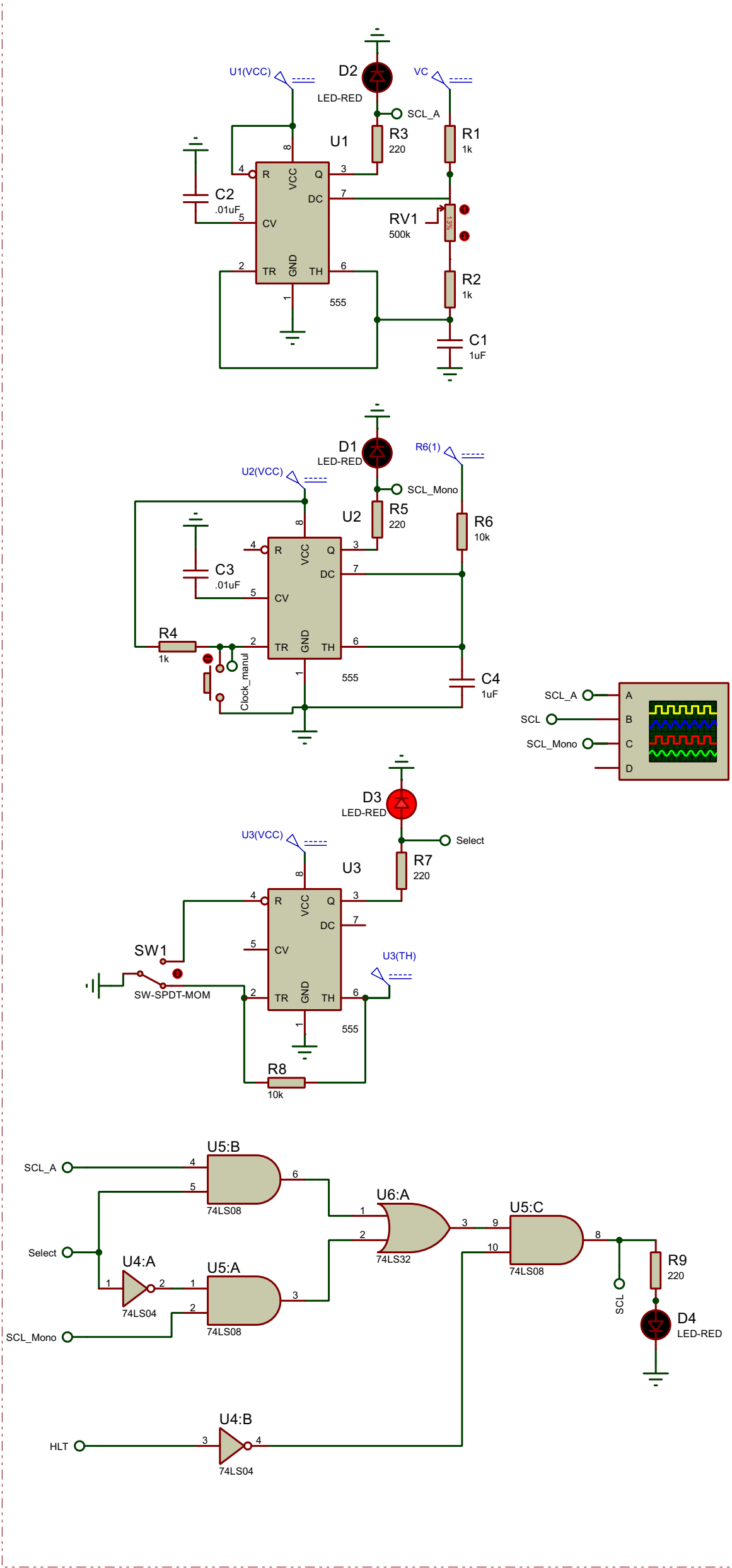
Model of Counter Design



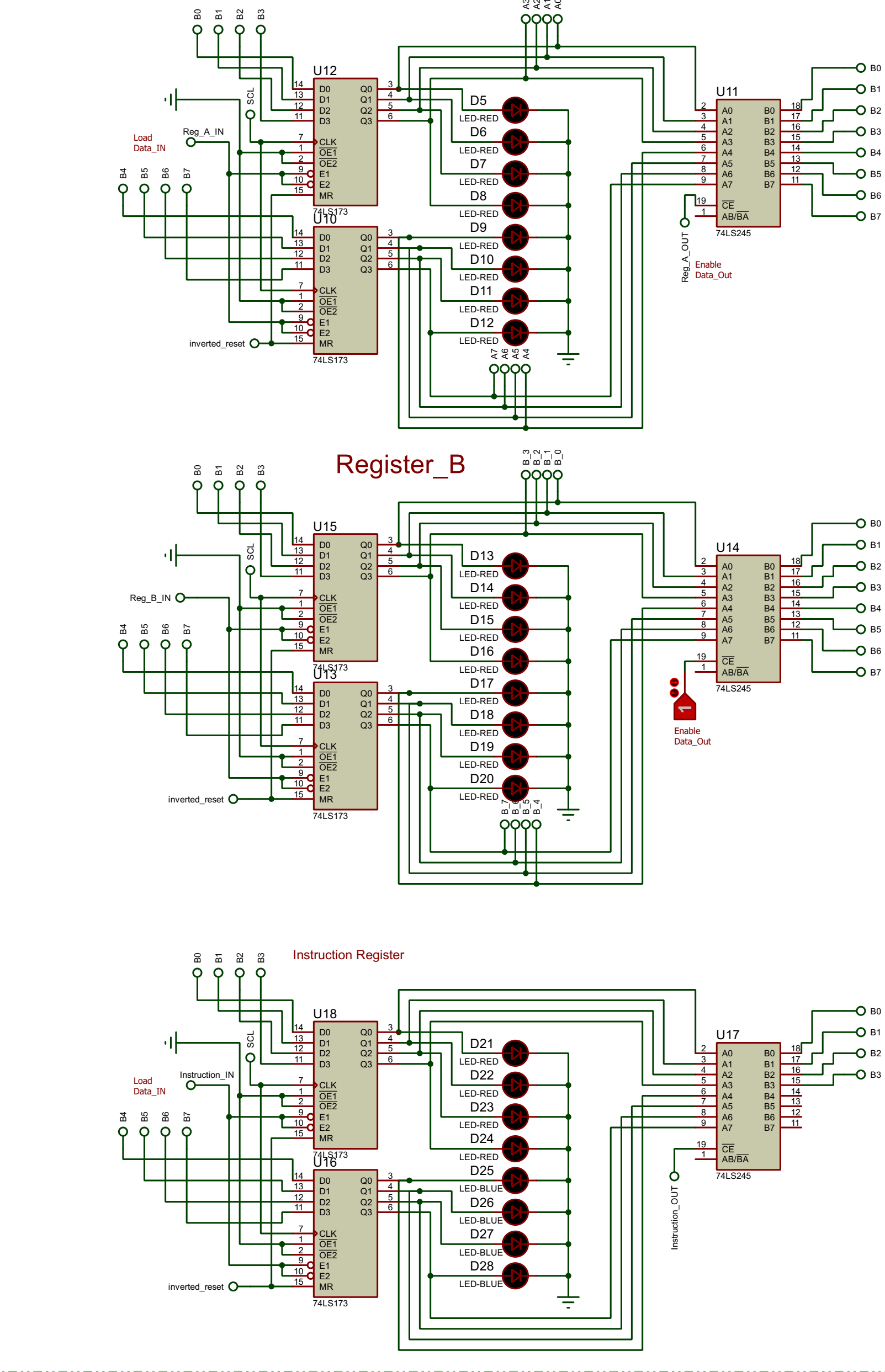
4-Bit Counter



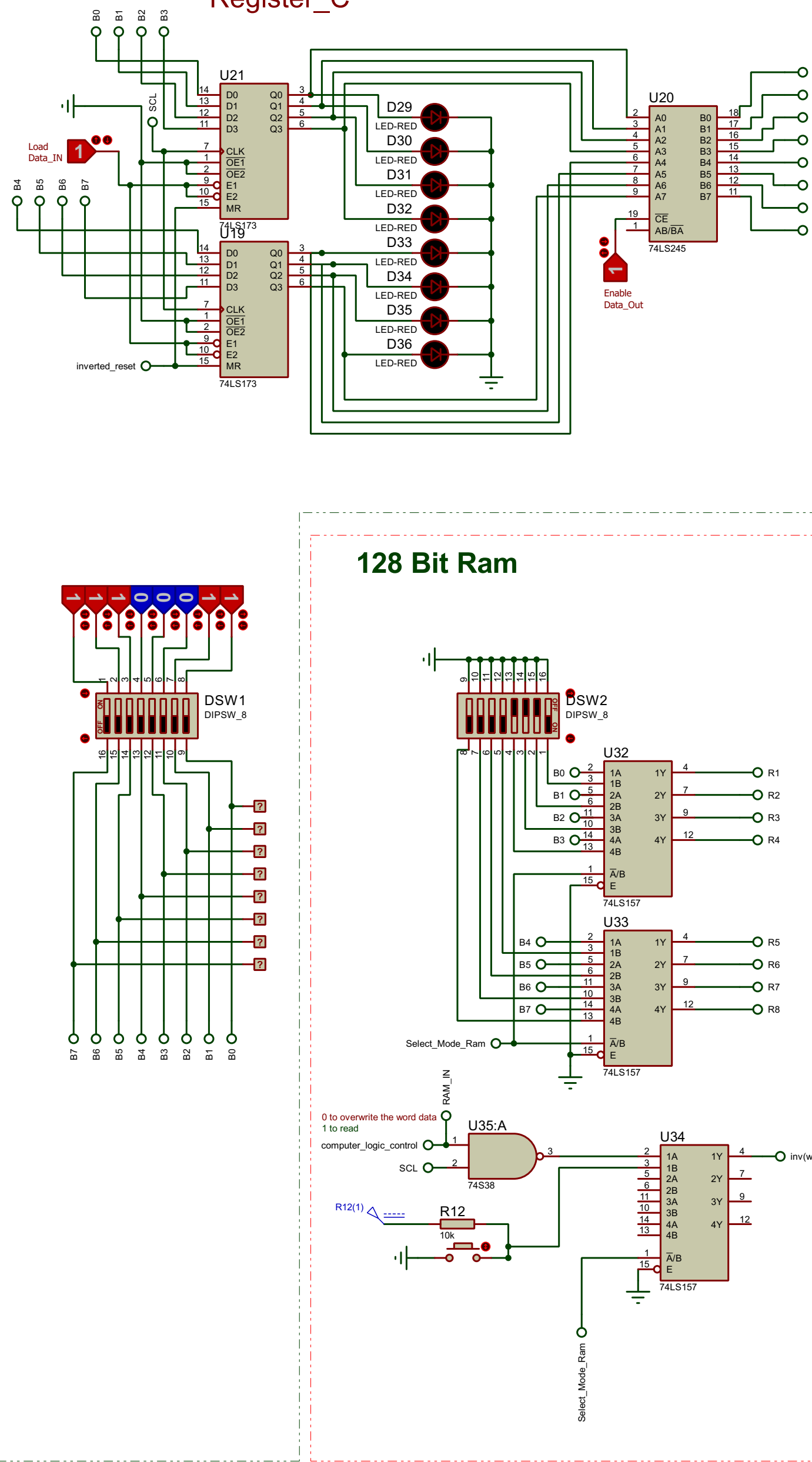
CLOCK



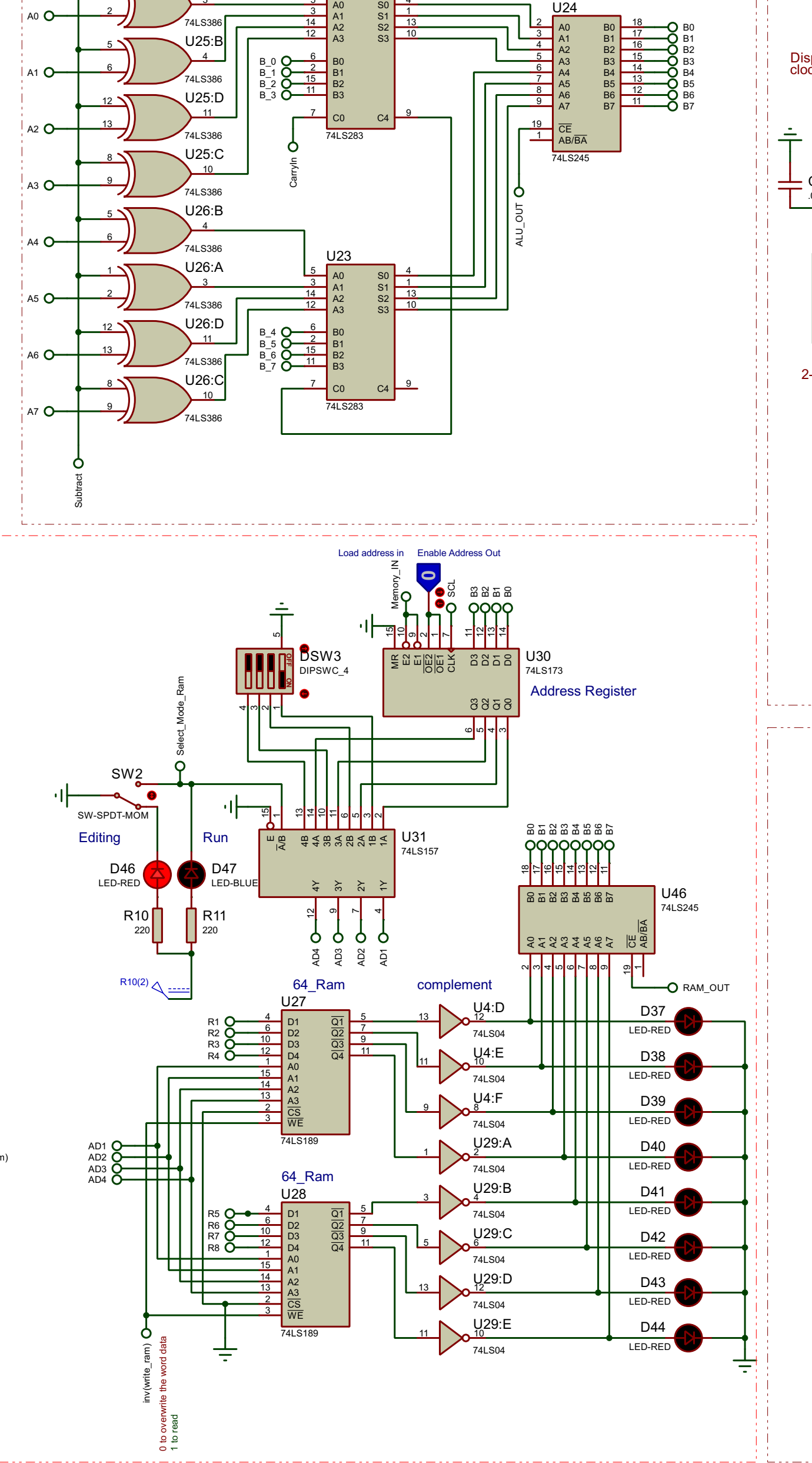
Registers & Bus



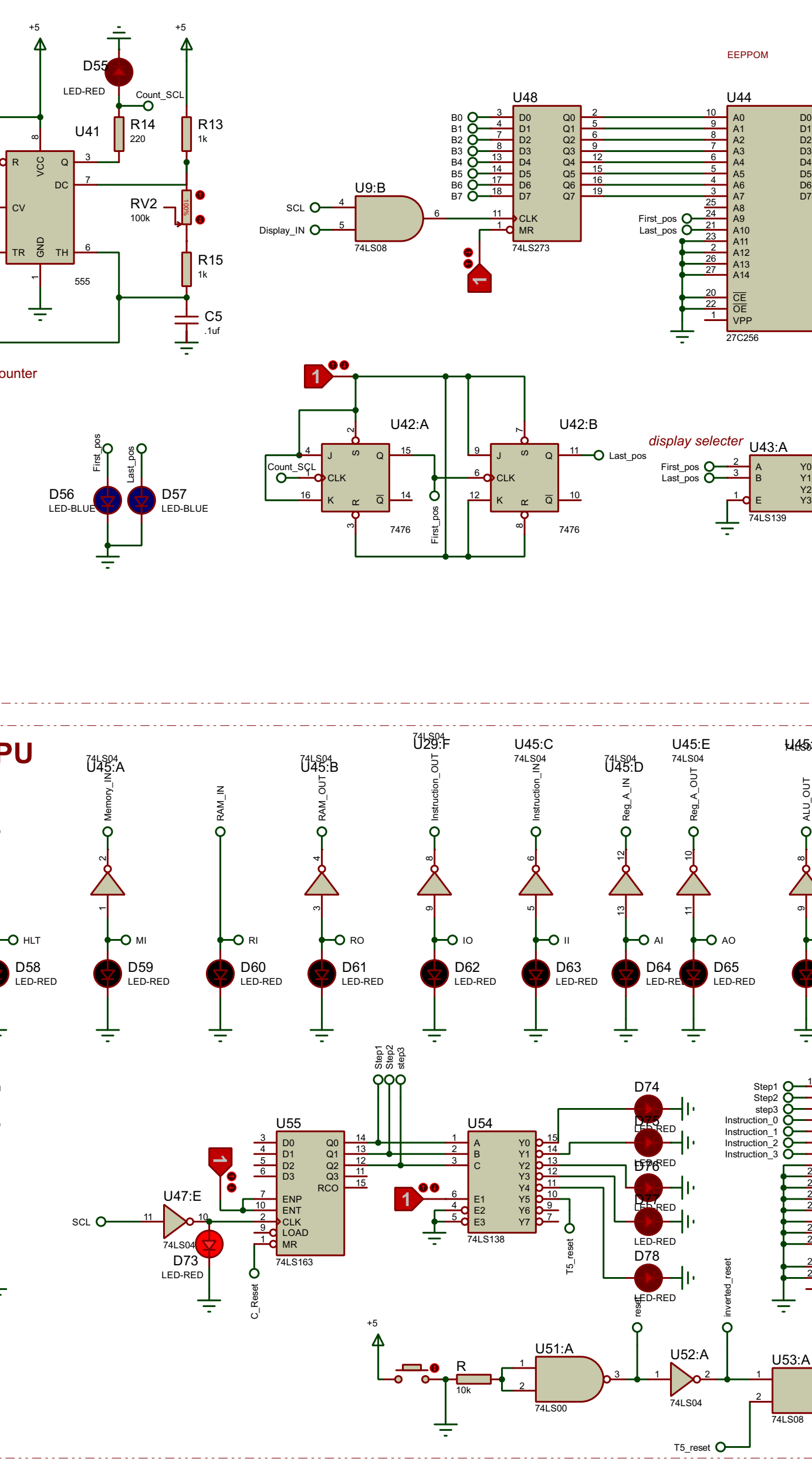
Register_A



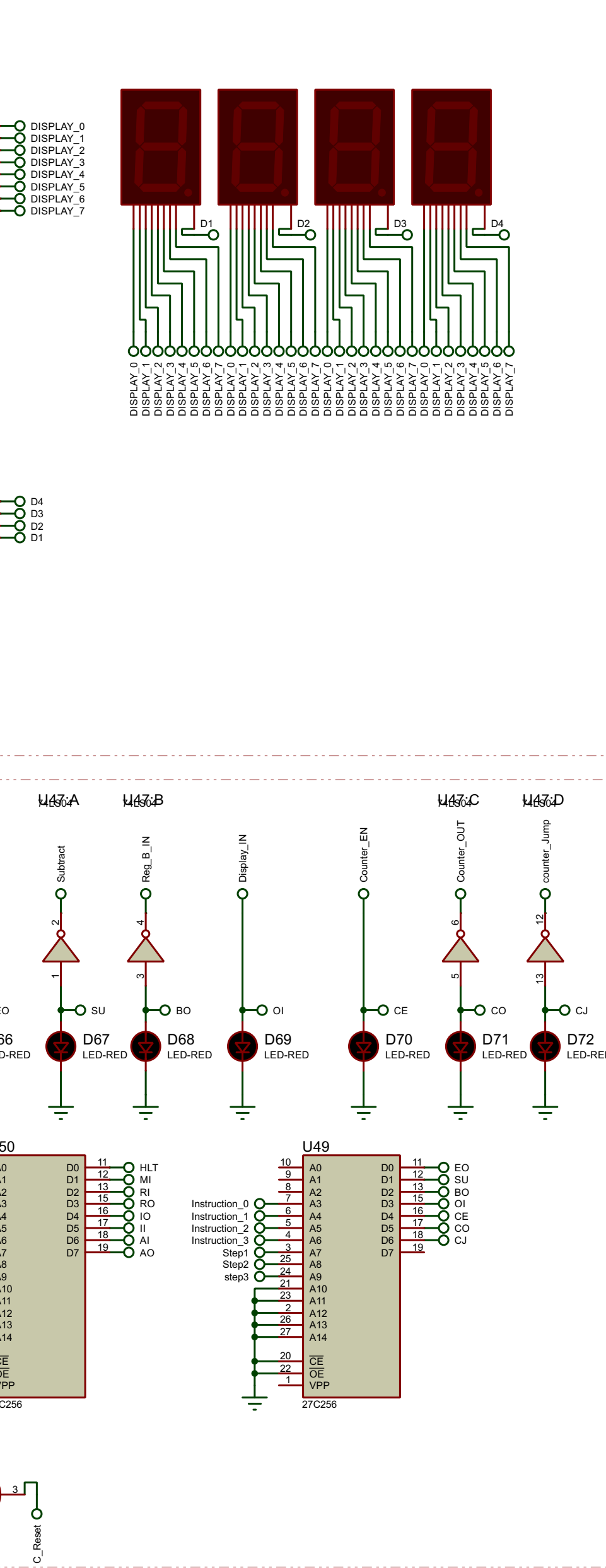
Register_B



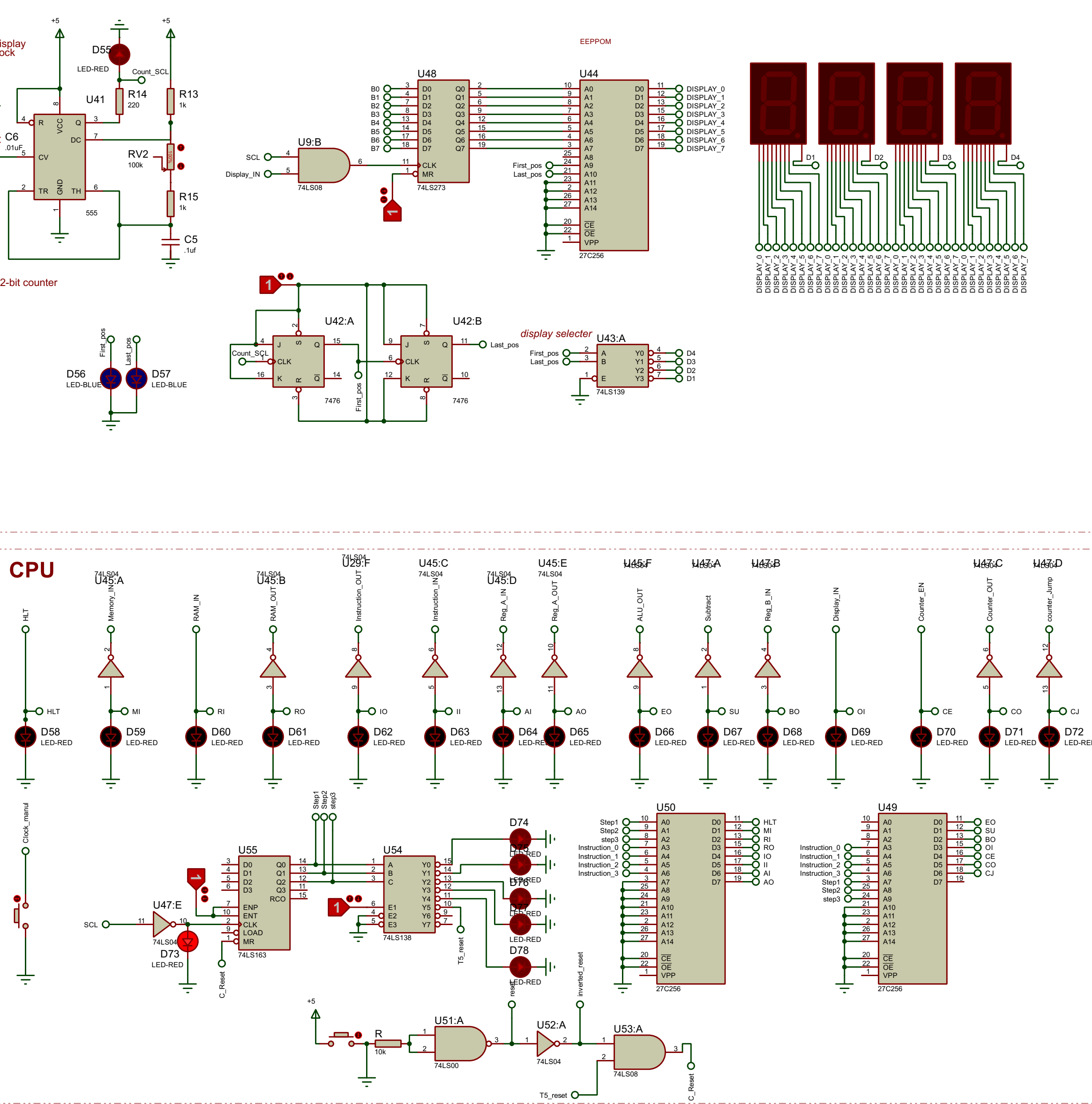
Register_C



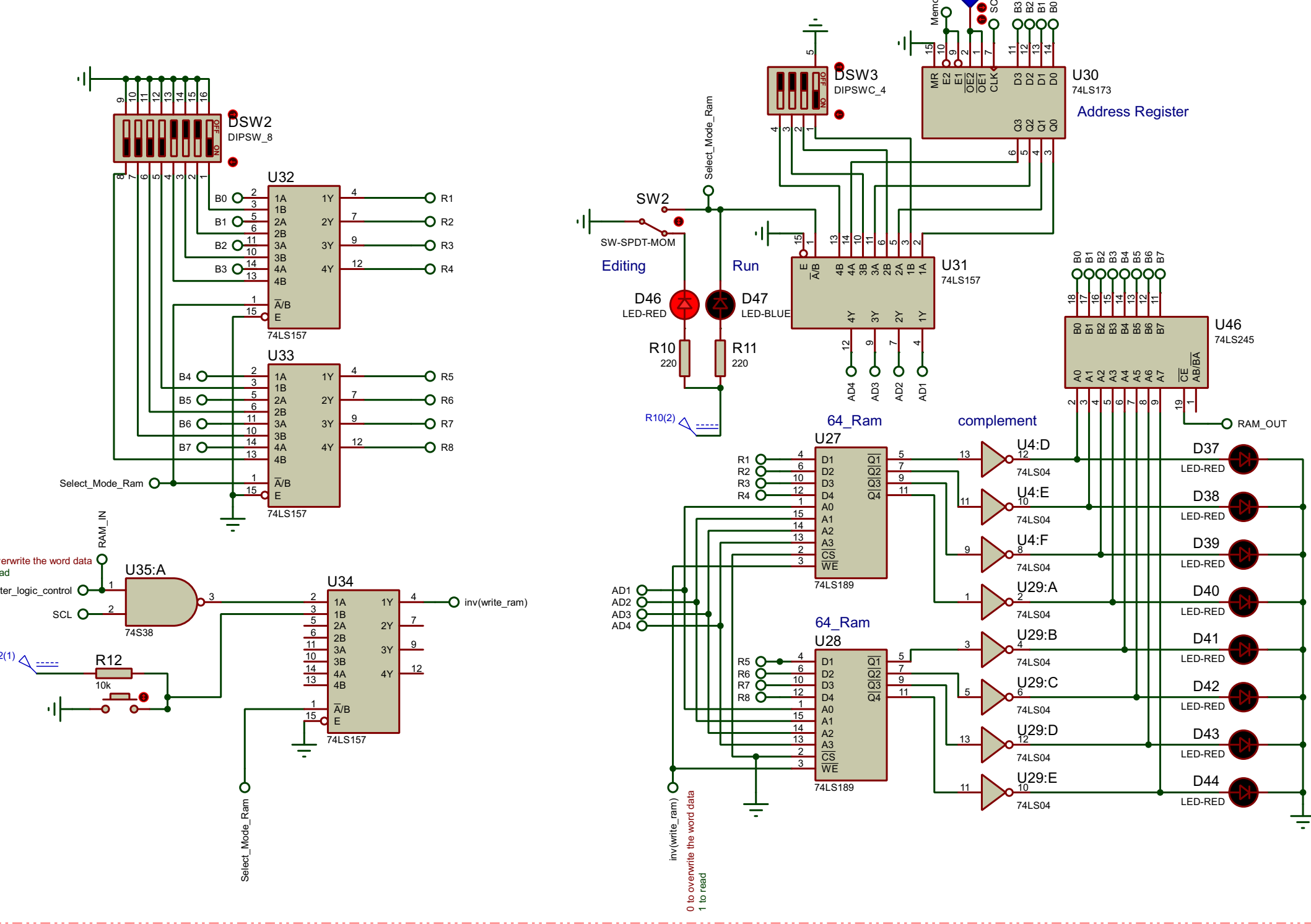
Adder/Subtractor



8-bit Display EERROM decoder Counter



128 Bit Ram



CPU

