Group:4 ECE Section-1

Frequency detector Using STM32.

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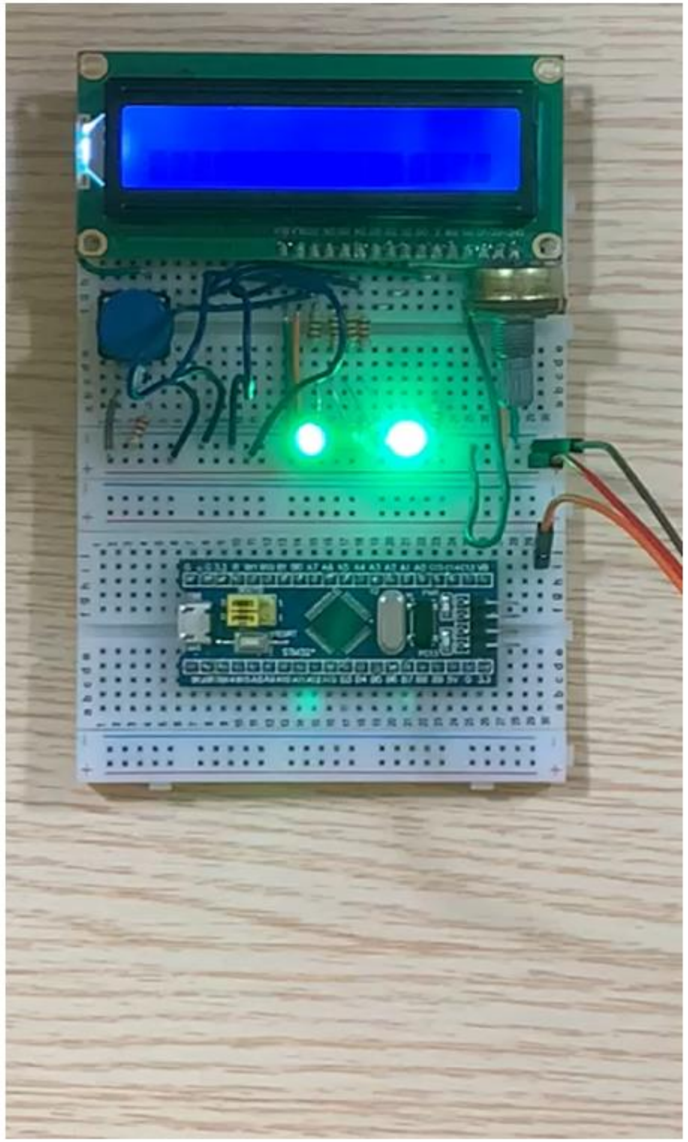
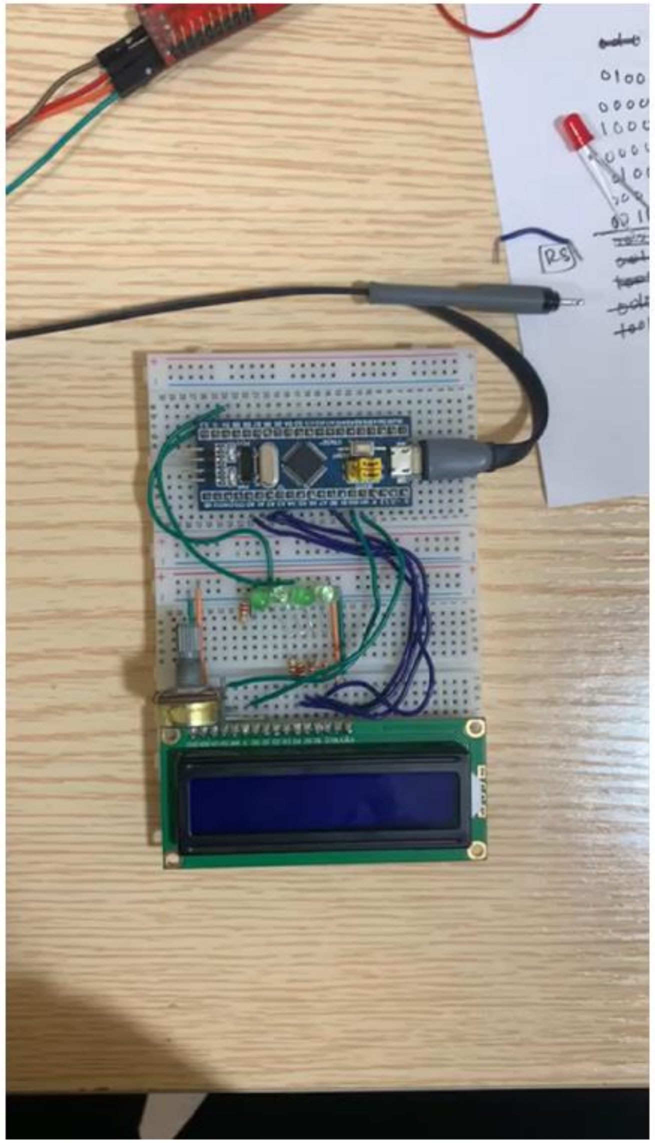
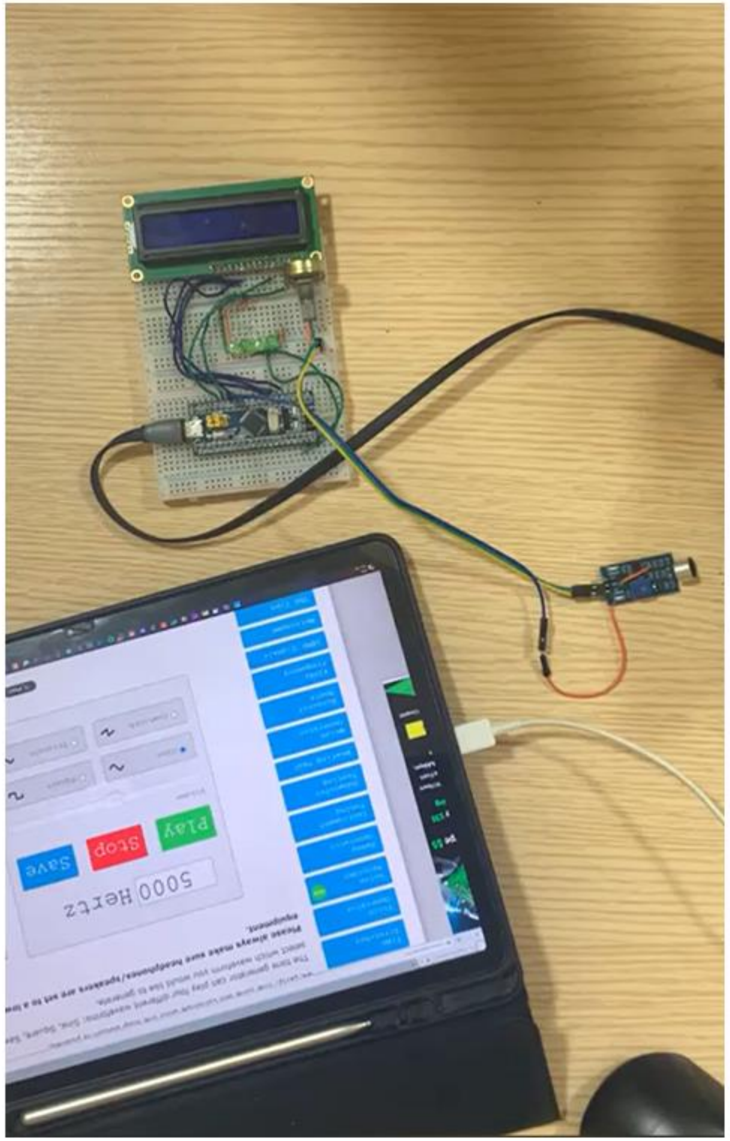
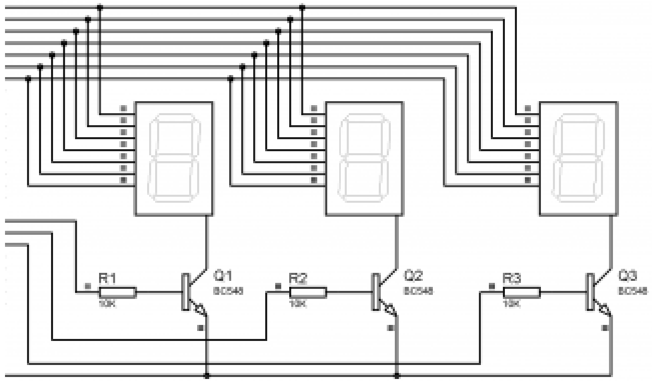
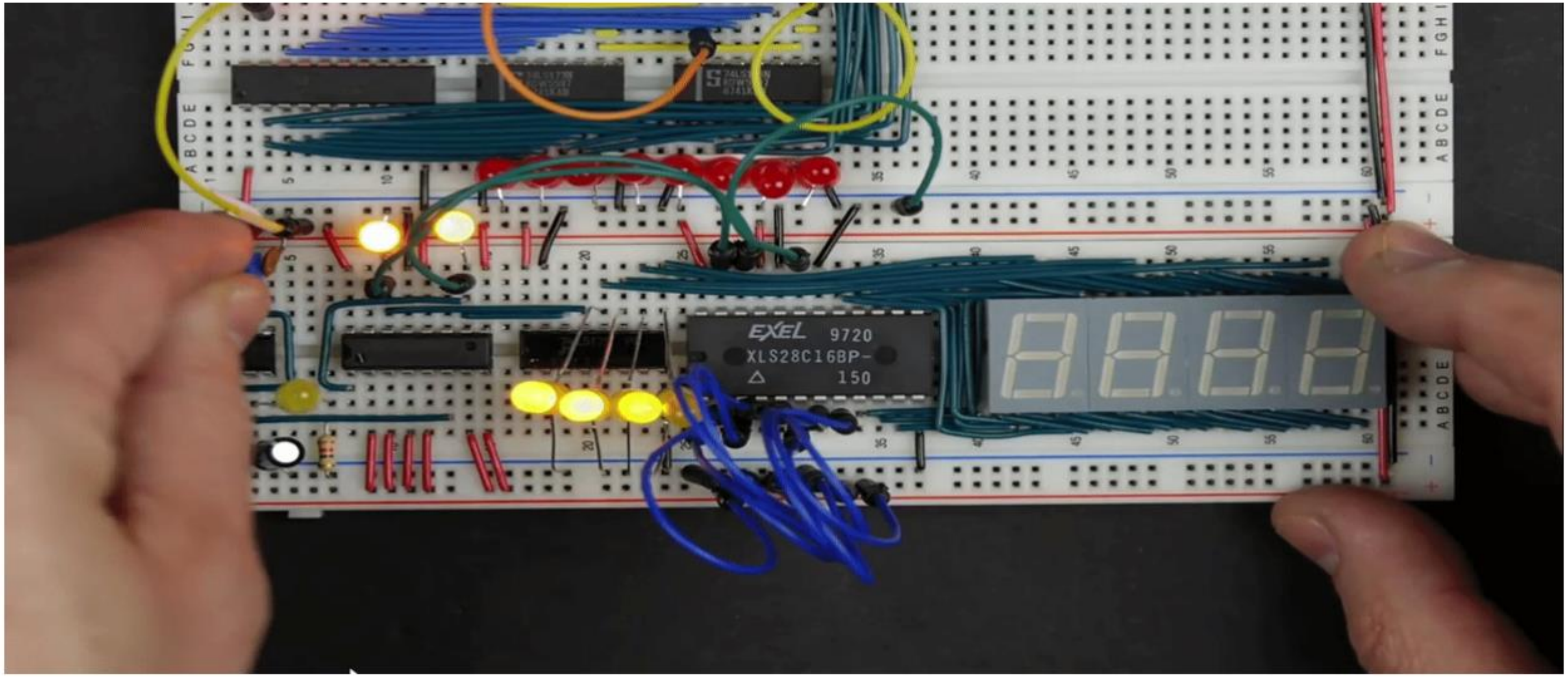
E-JUST

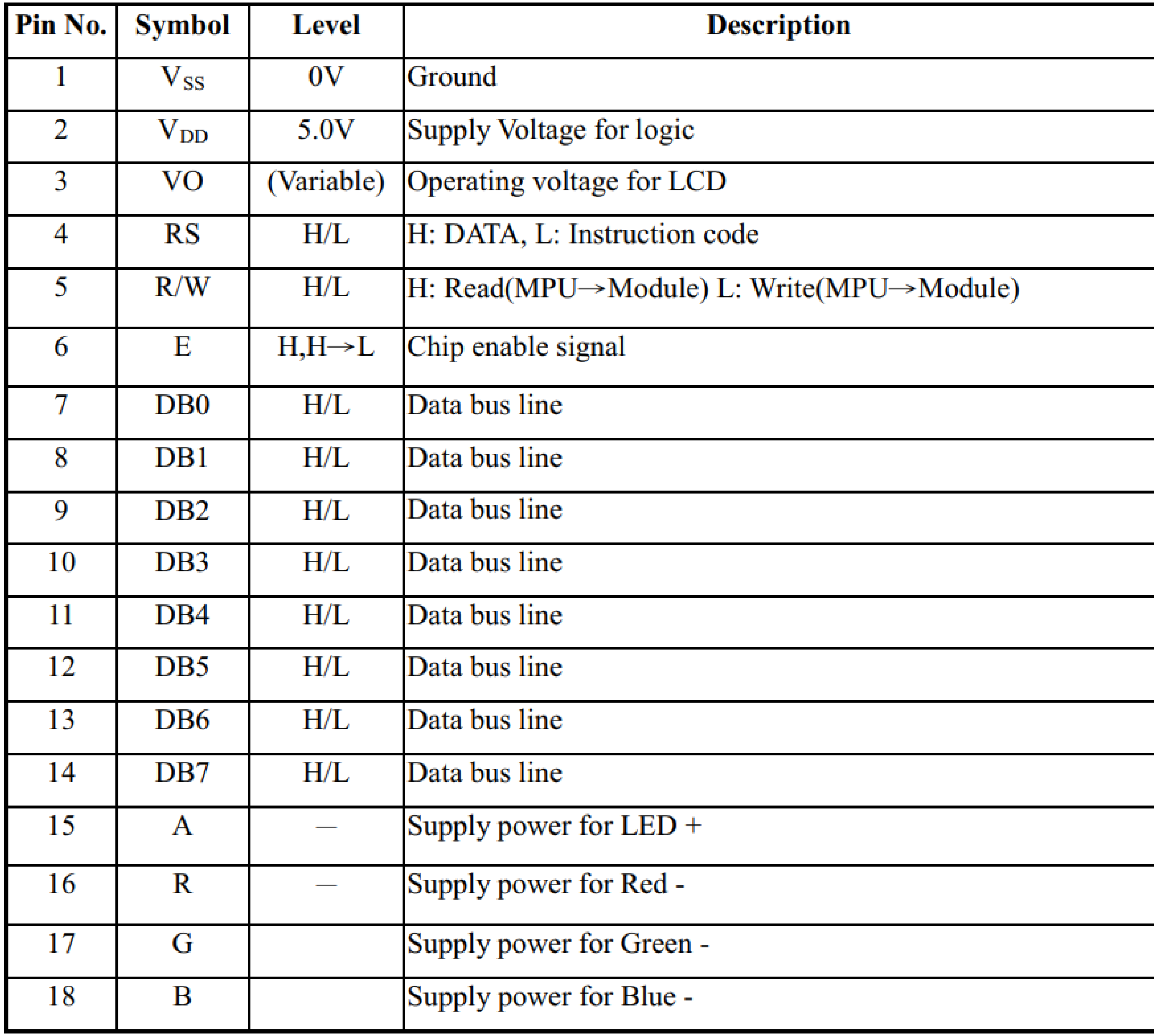



RS

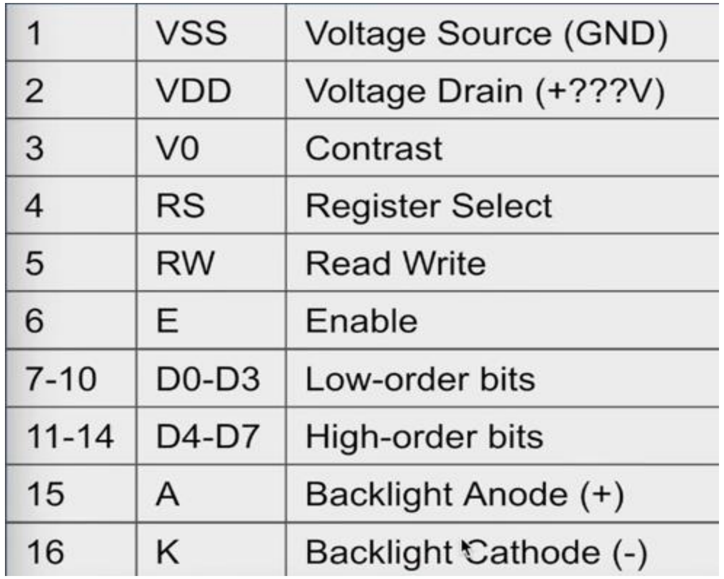

Play
Stop
Save
5000 Hertz


R1
10K
Q1
BC548
R2
10K
Q2
BC548
R3
10K
Q3
BC548

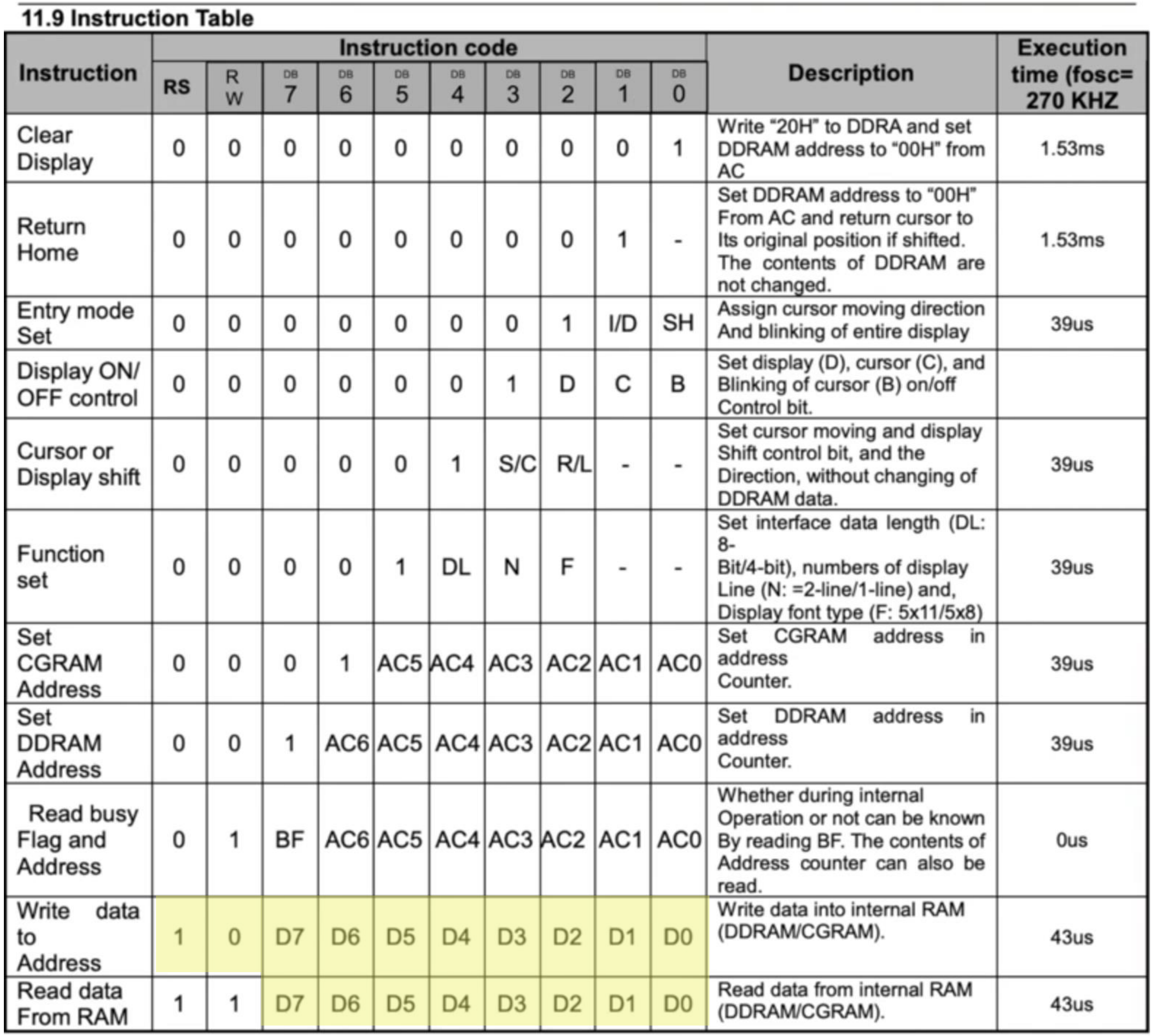

EXEL 9720
XLS28C16BP-
150



Pin No.	Symbol	Level	Description
1	V_{SS}	0V	Ground
2	V_{DD}	5.0V	Supply Voltage for logic
3	VO	(Variable)	Operating voltage for LCD
4	RS	H/L	H: DATA, L: Instruction code
5	R/W	H/L	H: Read(MPU→Module) L: Write(MPU→Module)
6	E	H,H→L	Chip enable signal
7	DB0	H/L	Data bus line
8	DB1	H/L	Data bus line
9	DB2	H/L	Data bus line
10	DB3	H/L	Data bus line
11	DB4	H/L	Data bus line
12	DB5	H/L	Data bus line
13	DB6	H/L	Data bus line
14	DB7	H/L	Data bus line
15	A	—	Supply power for LED +
16	R	—	Supply power for Red -
17	G		Supply power for Green -
18	B		Supply power for Blue -



1	VSS	Voltage Source (GND)
2	VDD	Voltage Drain (+???V)
3	V0	Contrast
4	RS	Register Select
5	RW	Read Write
6	E	Enable
7-10	D0-D3	Low-order bits
11-14	D4-D7	High-order bits
15	A	Backlight Anode (+)
16	K	Backlight Cathode (-)



11.9 Instruction Table

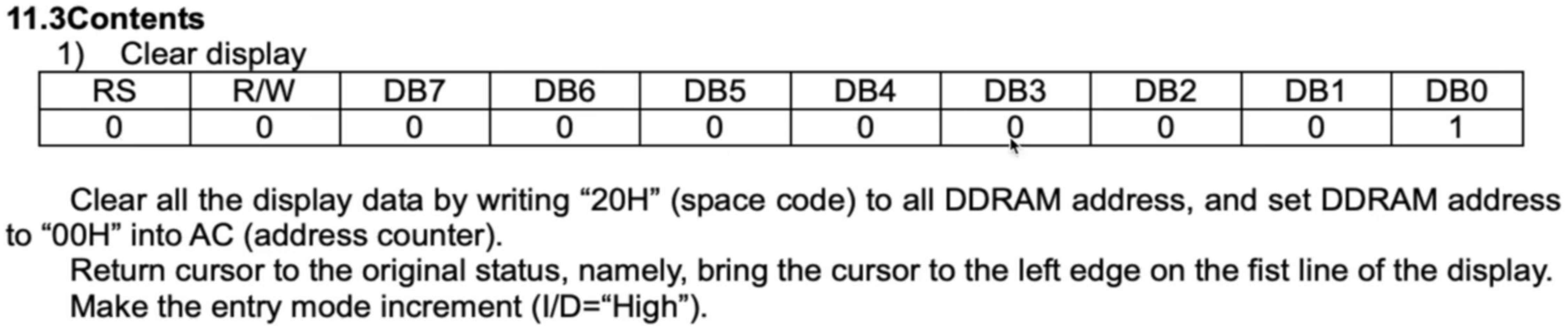
Instruction	Instruction code										Description	Execution time (fosc= 270 KHZ
	RS	R W	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRA and set DDRAM address to "00H" from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" From AC and return cursor to Its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction And blinking of entire display	39us
Display ON/ OFF control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and Blinking of cursor (B) on/off Control bit.	
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display Shift control bit, and the Direction, without changing of DDRAM data.	39us
Function set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-Bit/4-bit), numbers of display Line (N: =2-line/1-line) and, Display font type (F: 5x11/5x8)	39us
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address Counter.	39us
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address Counter.	39us
Read busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal Operation or not can be known By reading BF. The contents of Address counter can also be read.	0us
Write data to Address	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43us
Read data From RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43us

00: 0000 0001 Clear Display

00: 0000 001X Return Home

00: 0000 0100 Display /cursor on

00: 0001 0000 (4-Bit Mode)



11.3Contents

1) Clear display

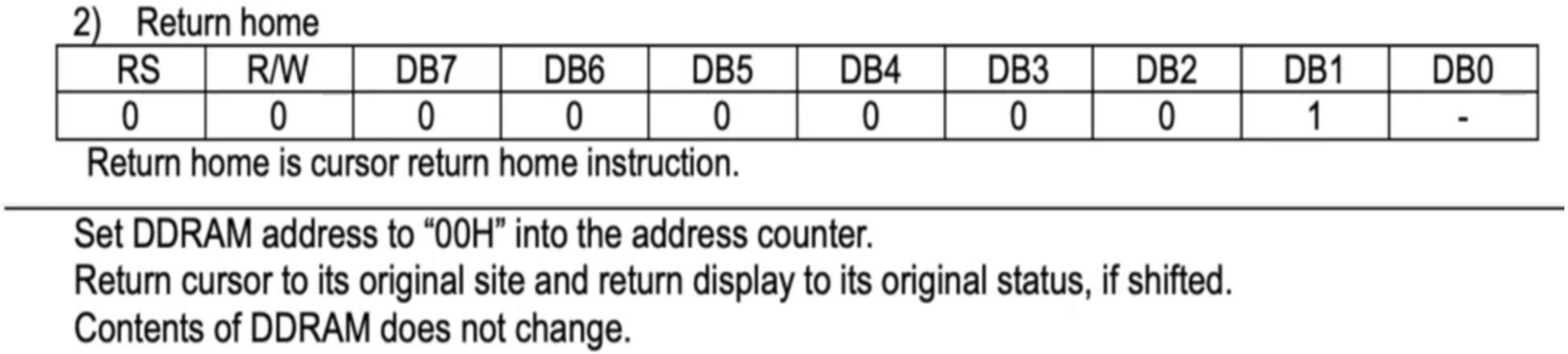
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter).

Return cursor to the original status, namely, bring the cursor to the left edge on the fist line of the display.

Make the entry mode increment (I/D=“High”).

00: 0000 0001 Clear Display



2) Return home

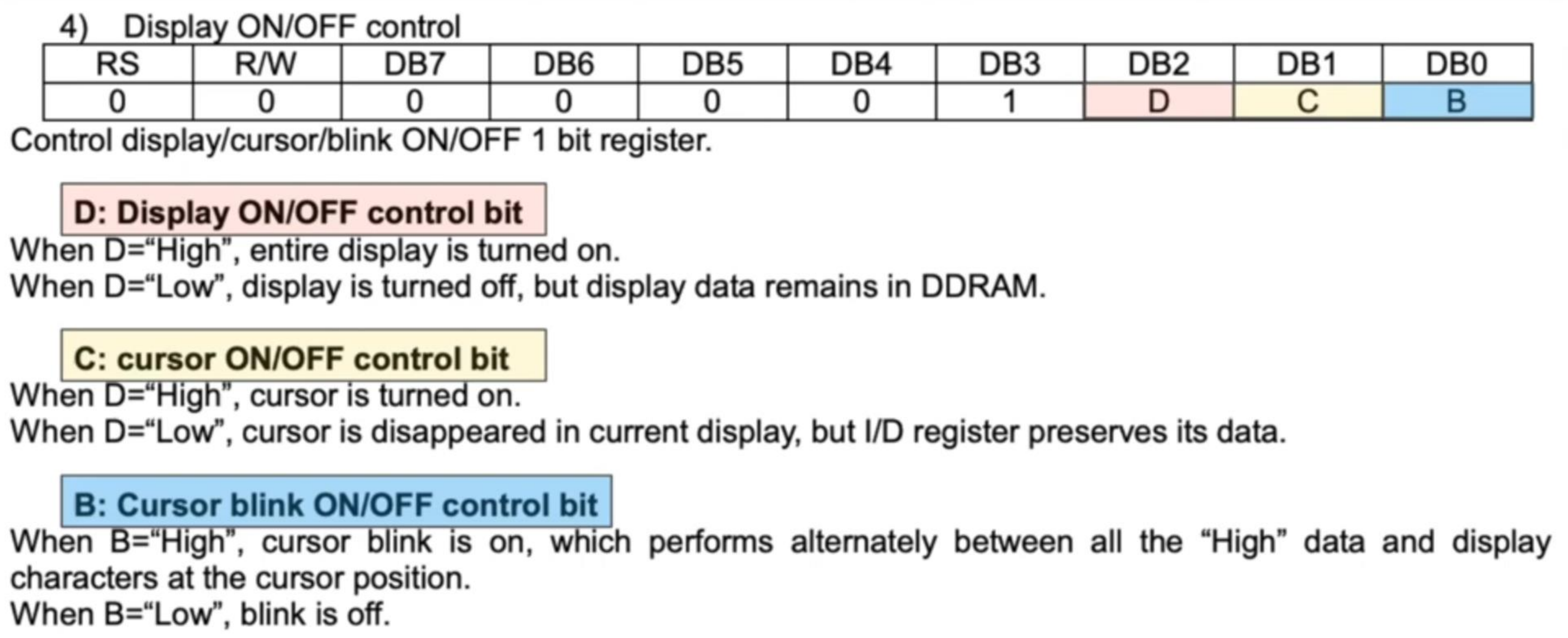
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Return home is cursor return home instruction.

Set DDRAM address to “00H” into the address counter.
Return cursor to its original site and return display to its original status, if shifted.
Contents of DDRAM does not change.

00: 0000 0001 Clear Display

00: 0000 001X Return Home



4) Display ON/OFF control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit

When D="High", entire display is turned on.
When D="Low", display is turned off, but display data remains in DDRAM.

C: cursor ON/OFF control bit

When D="High", cursor is turned on.
When D="Low", cursor is disappeared in current display, but I/D register preserves its data.

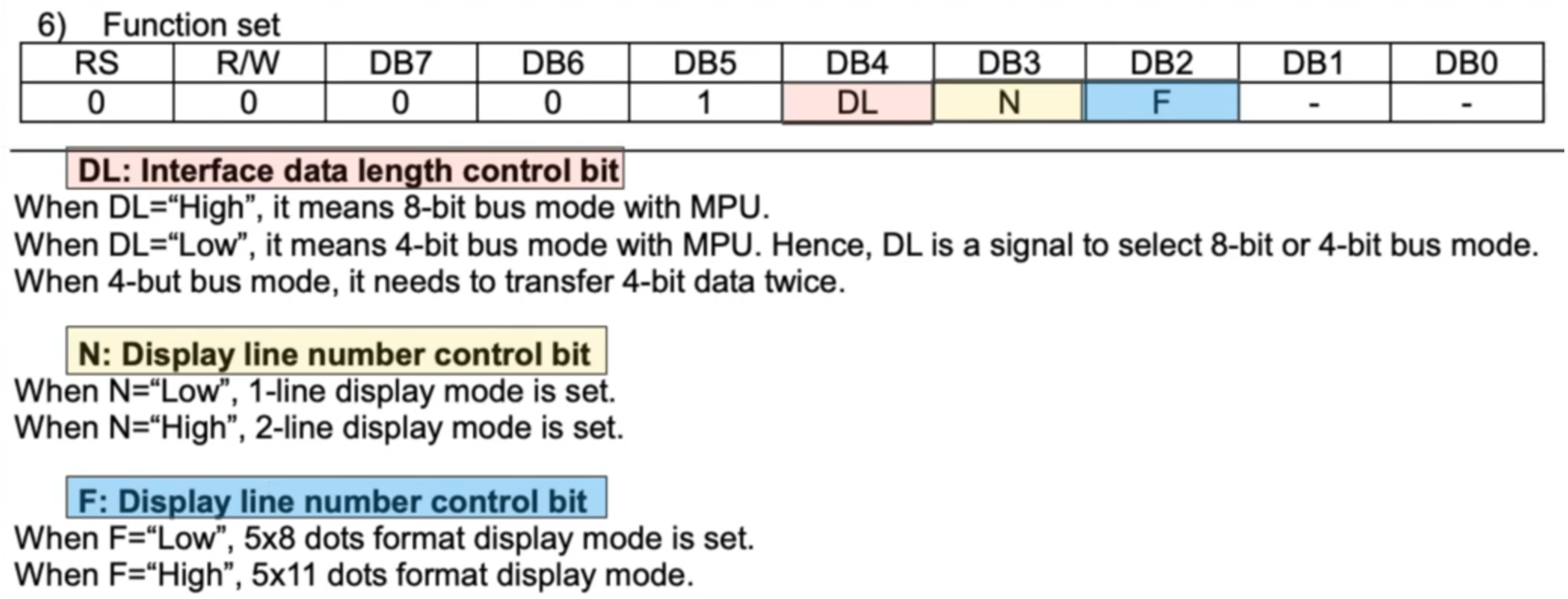
B: Cursor blink ON/OFF control bit

When B="High", cursor blink is on, which performs alternately between all the "High" data and display characters at the cursor position.
When B="Low", blink is off.

00: 0000 0001 Clear Display

00: 0000 001X Return Home

00: 0000 0101 Display /cursor on



6) Function set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL: Interface data length control bit

When DL="High", it means 8-bit bus mode with MPU.
When DL="Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-but bus mode, it needs to transfer 4-bit data twice.

N: Display line number control bit

When N="Low", 1-line display mode is set.
When N="High", 2-line display mode is set.

F: Display line number control bit

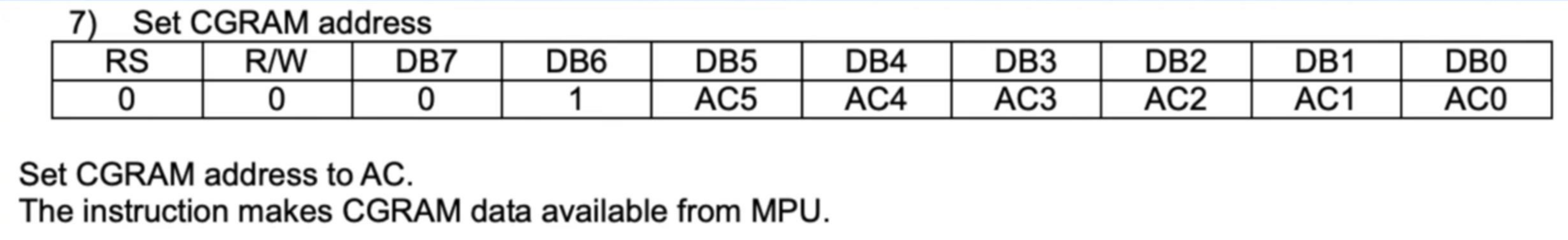
When F="Low", 5x8 dots format display mode is set.
When F="High", 5x11 dots format display mode.

00: 0000 0001 Clear Display

00: 0000 001X Return Home

00: 0000 0100 Display /cursor on

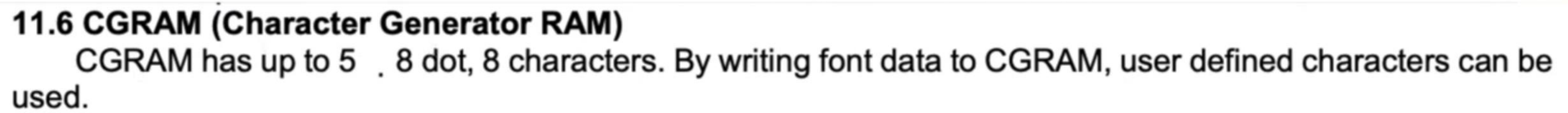
00: 0001 0000 (4-Bit Mode)



7) Set CGRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
The instruction makes CGRAM data available from MPU.



11.6 CGRAM (Character Generator RAM)

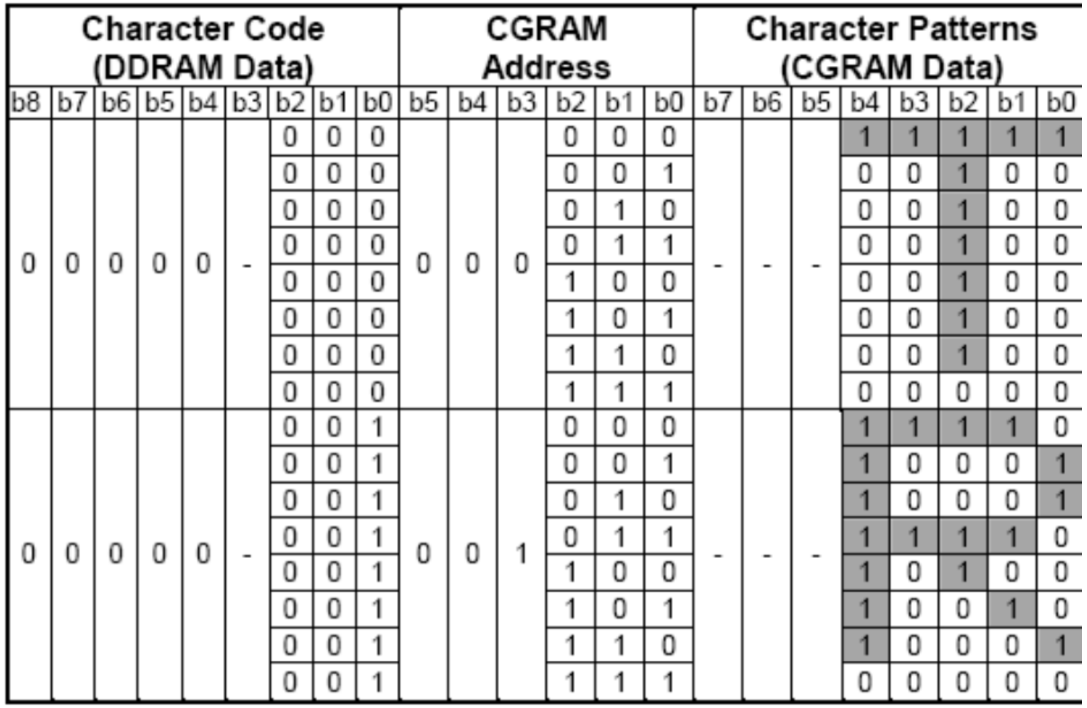
CGRAM has up to 5 . 8 dot, 8 characters. By writing font data to CGRAM, user defined characters can be used.

00: 0000 0001 Clear Display

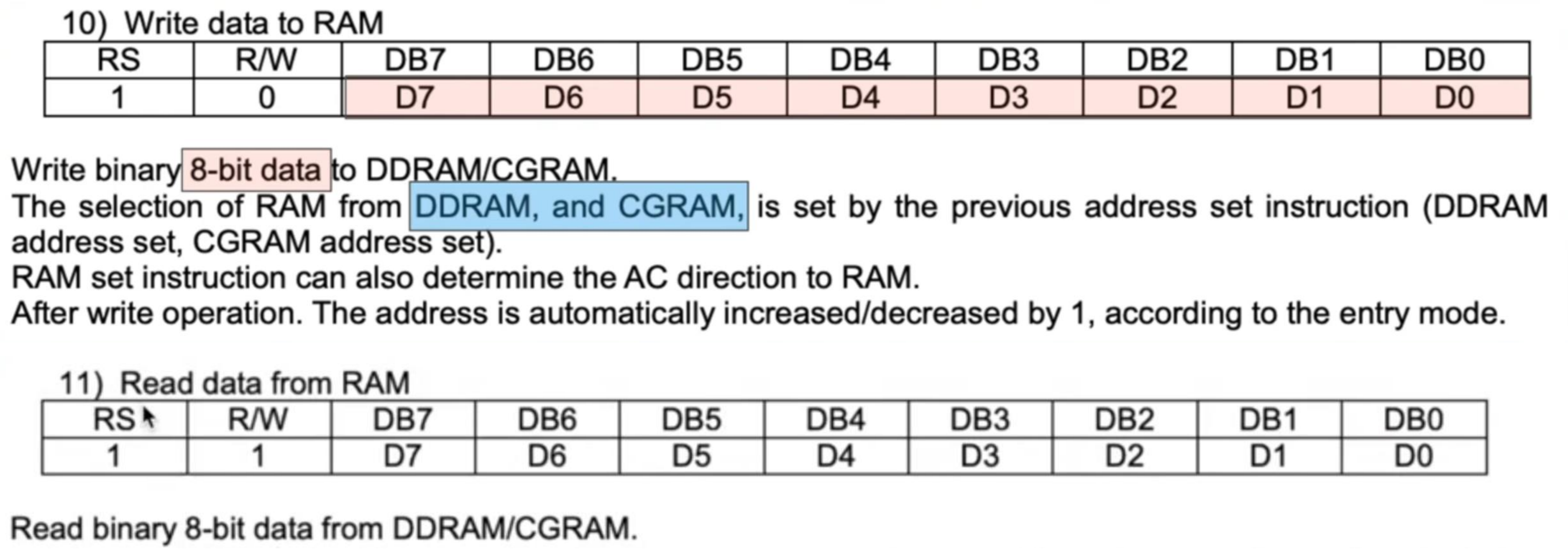
00: 0000 001X Return Home

00: 0000 0100 Display /cursor on

00: 0001 0000 (4-Bit Mode)



Character Code (DDRAM Data)									CGRAM Address						Character Patterns (CGRAM Data)							
b8	b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	-	0	0	0	0	0	0	0	0	0	-	-	-	1	1	1	1	1
						0	0	0				0	0	1				0	0	1	0	0
						0	0	0				0	1	0				0	0	1	0	0
						0	0	0				0	1	1				0	0	1	0	0
						0	0	0				1	0	0				0	0	1	0	0
						0	0	0				1	0	1				0	0	1	0	0
						0	0	0				1	1	0				0	0	1	0	0
						0	0	0				1	1	1				0	0	0	0	0
0	0	0	0	0	-	0	0	1	0	0	1	0	0	0	-	-	-	1	1	1	1	0
						0	0	1				0	0	1				1	0	0	0	1
						0	0	1				0	1	0				1	0	0	0	1
						0	0	1				0	1	1				1	1	1	1	0
						0	0	1				1	0	0				1	0	1	0	0
						0	0	1				1	0	1				1	0	0	1	0
						0	0	1				1	1	0				1	0	0	0	1
						0	0	1				1	1	1				0	0	0	0	0



10) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set).
RAM set instruction can also determine the AC direction to RAM.
After write operation. The address is automatically increased/decreased by 1, according to the entry mode.

11) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

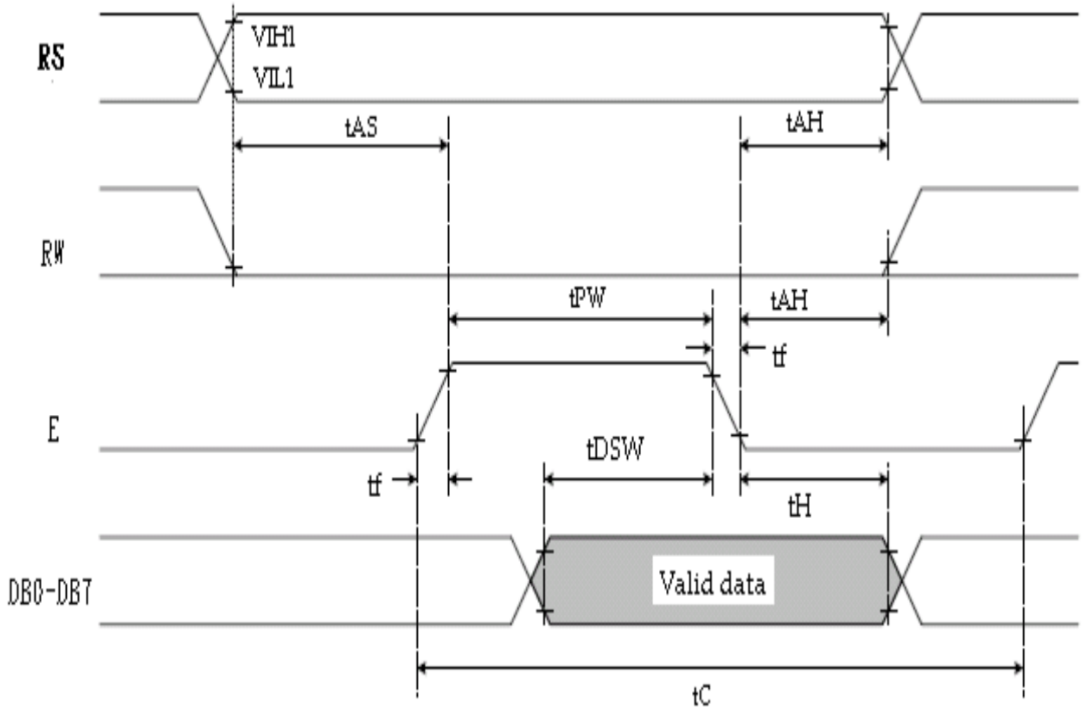
Read binary 8-bit data from DDRAM/CGRAM.

00: 0000 0001 Clear Display

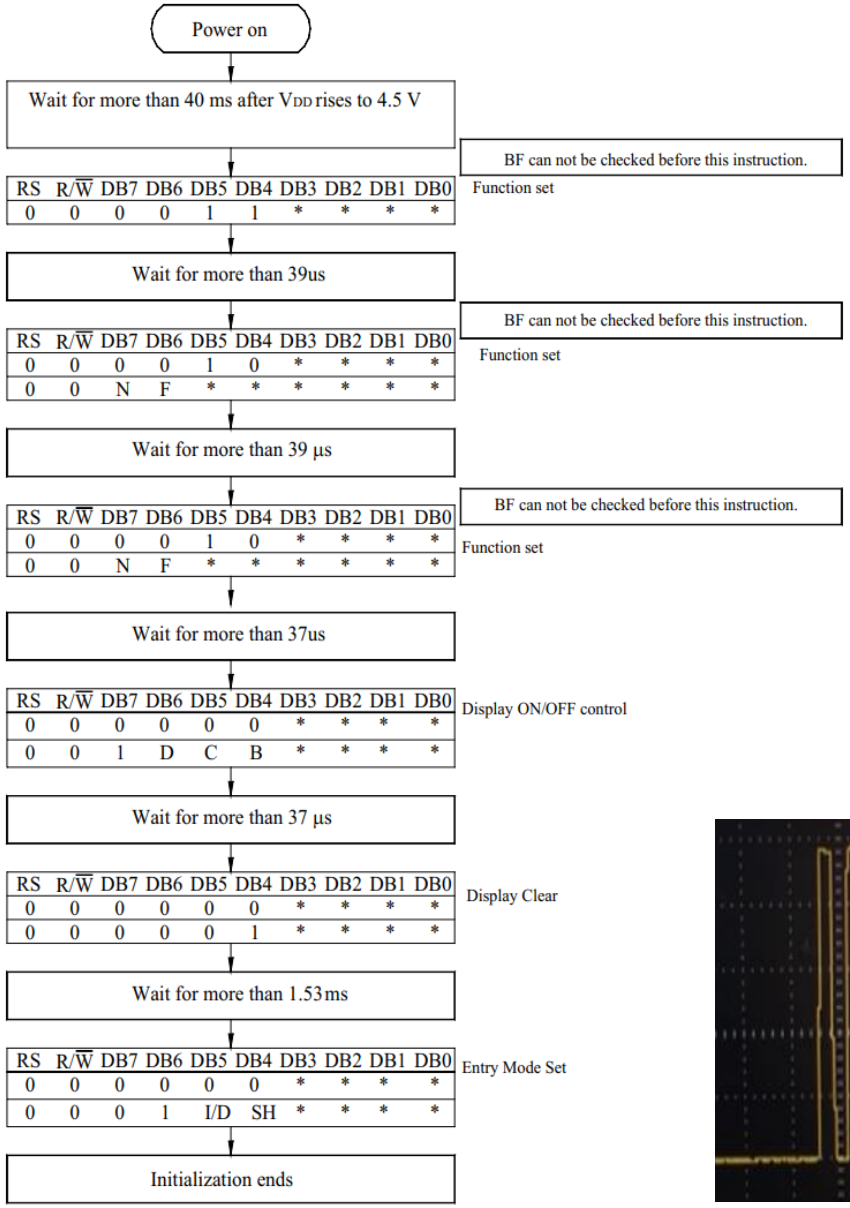
00: 0000 001X Return Home

00: 0000 0100 Display /cursor on

10: xxxx xxxx Display char



Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	T_C	1200	–	–	ns
Enable pulse width	T_{PW}	140	–	–	ns
Enable rise/fall time	T_R,T_F	–	–	25	ns
Address set-up time (RS, R/W to E)	t_{AS}	0	–	–	ns
Address hold time	t_{AH}	10	–	–	ns
Data set-up time	t_{DSW}	40	–	–	ns
Data hold time	t_H	10	–	–	ns



Power on

Wait for more than 40 ms after V_{DD} rises to 4.5 V

BF can not be checked before this instruction.

Function set

RS	R/W̄	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	*	*	*	*

Wait for more than 39us

BF can not be checked before this instruction.

Function set

RS	R/W̄	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	*	*	*	*
0	0	N	F	*	*	*	*	*	*

Wait for more than 39 μs

BF can not be checked before this instruction.

Function set

RS	R/W̄	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	*	*	*	*
0	0	N	F	*	*	*	*	*	*

Wait for more than 37us

Display ON/OFF control

RS	R/W̄	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	*	*	*	*
0	0	1	D	C	B	*	*	*	*

Wait for more than 37 μs

Display Clear

RS	R/W̄	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	*	*	*	*
0	0	0	0	0	1	*	*	*	*

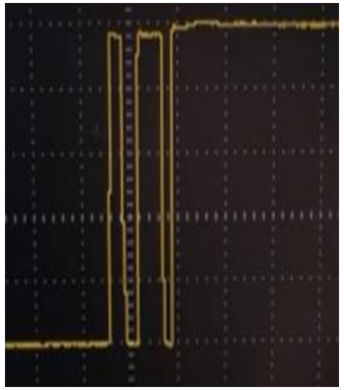
Wait for more than 1.53ms

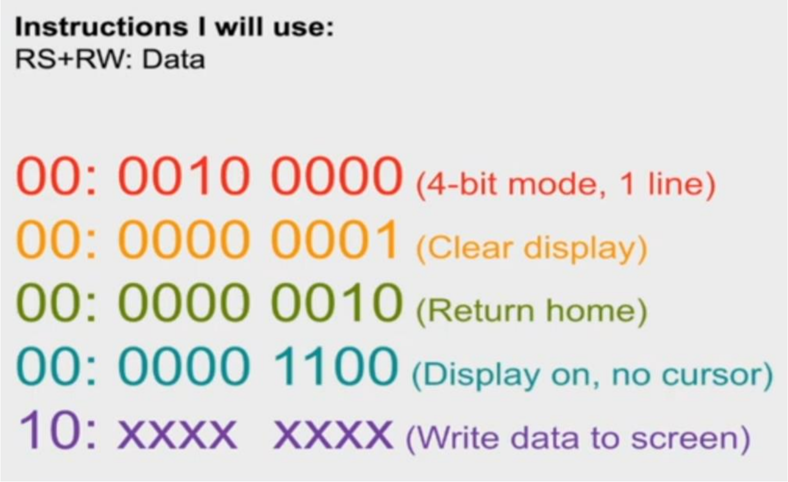
Entry Mode Set

RS	R/W̄	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	*	*	*	*
0	0	0	1	I/D	SH	*	*	*	*

Initialization ends

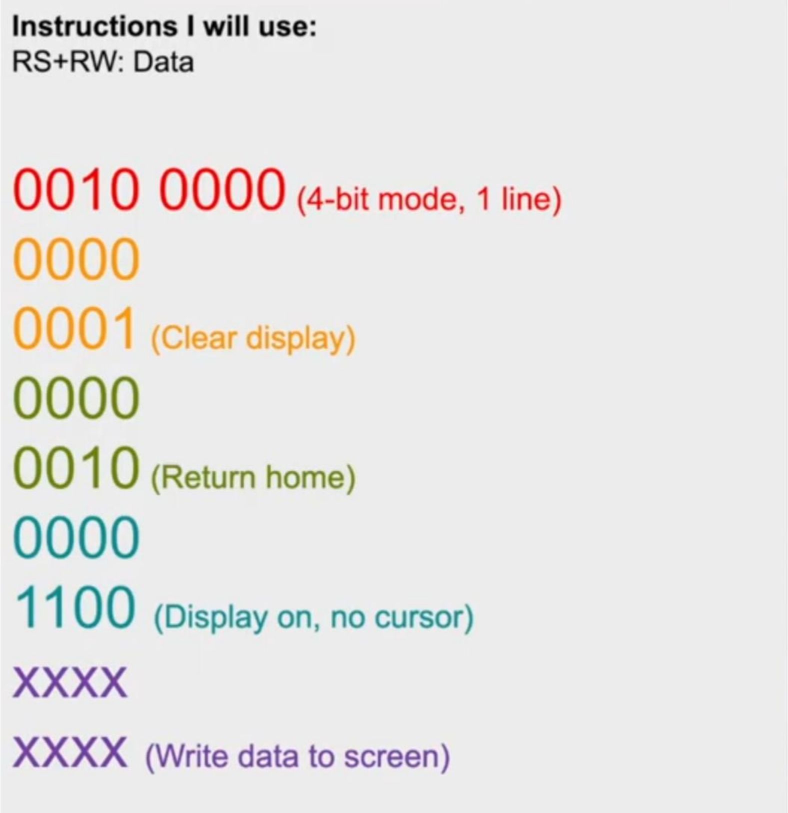
4-Bit Ineterface





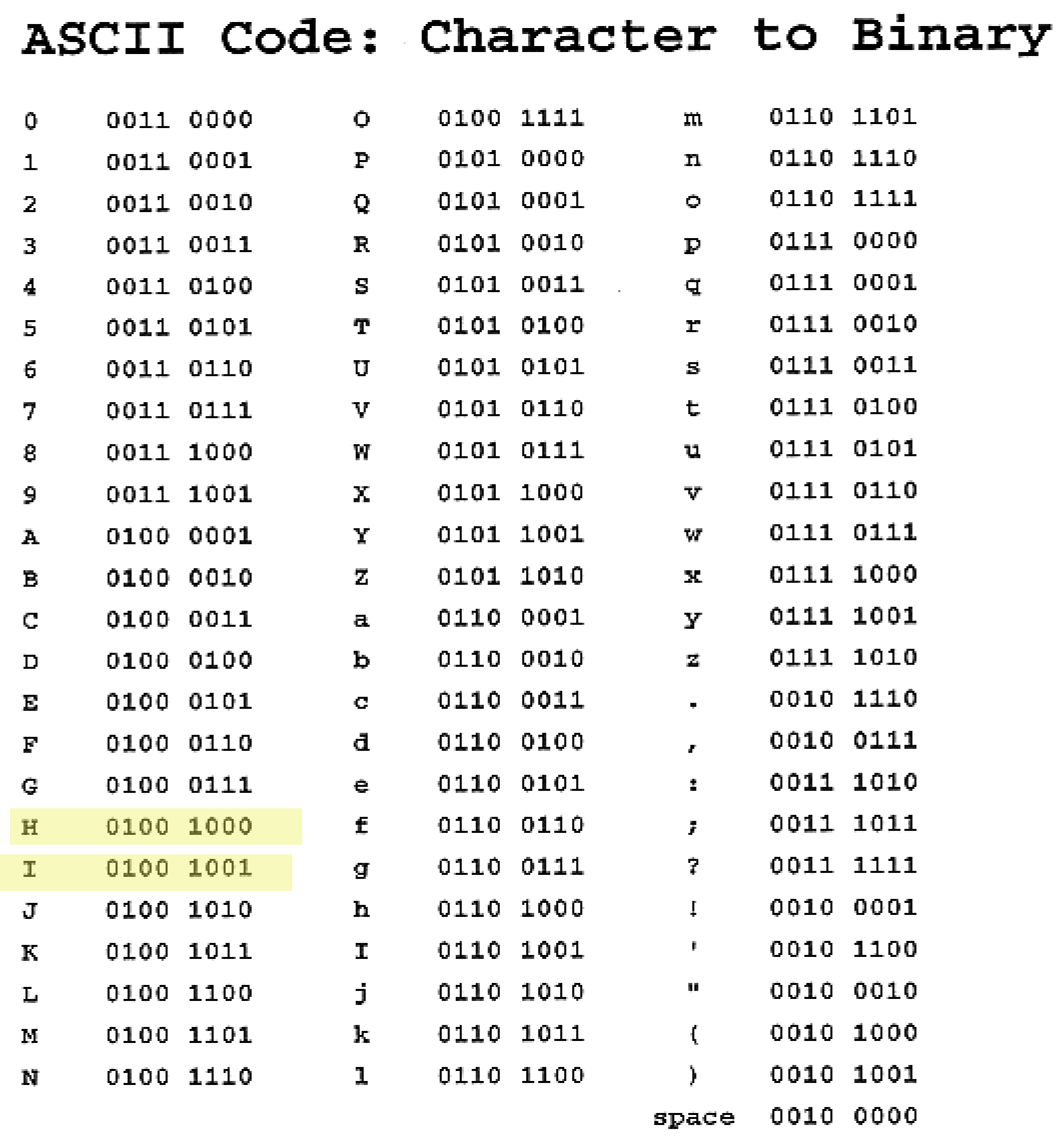
Instructions I will use:
RS+RW: Data

00: 0010 0000 (4-bit mode, 1 line)
00: 0000 0001 (Clear display)
00: 0000 0010 (Return home)
00: 0000 1100 (Display on, no cursor)
10: XXXX XXXX (Write data to screen)



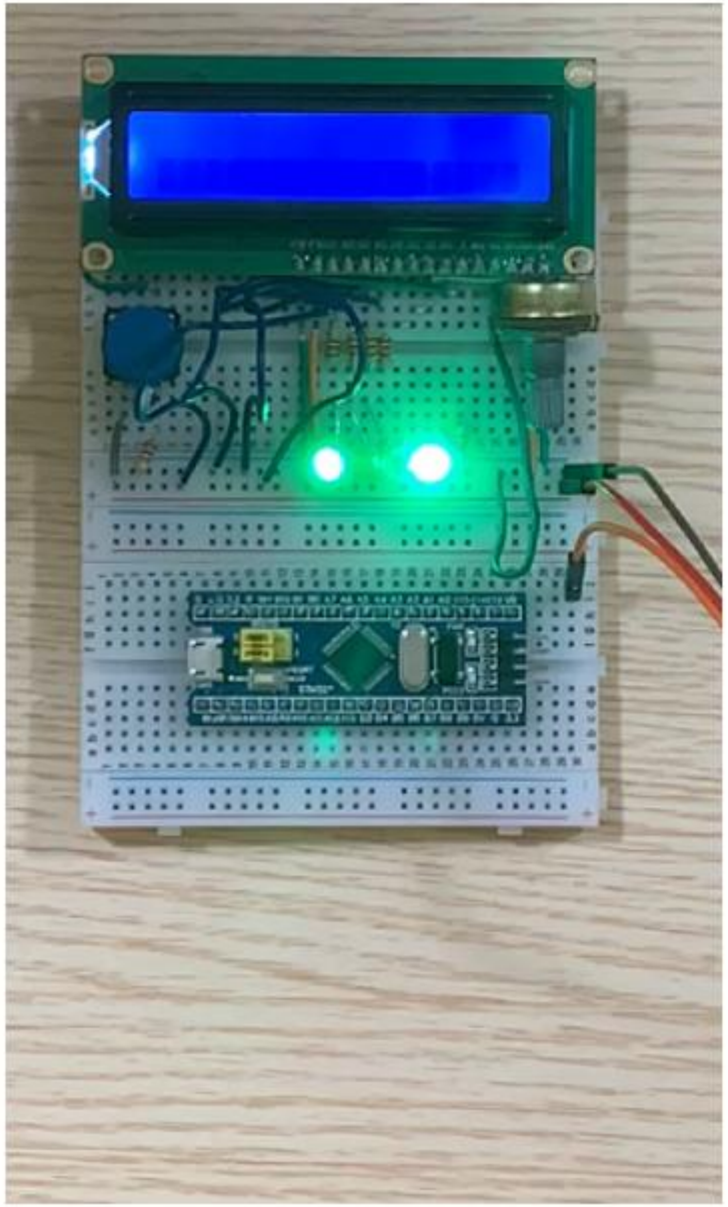
Instructions I will use:
RS+RW: Data

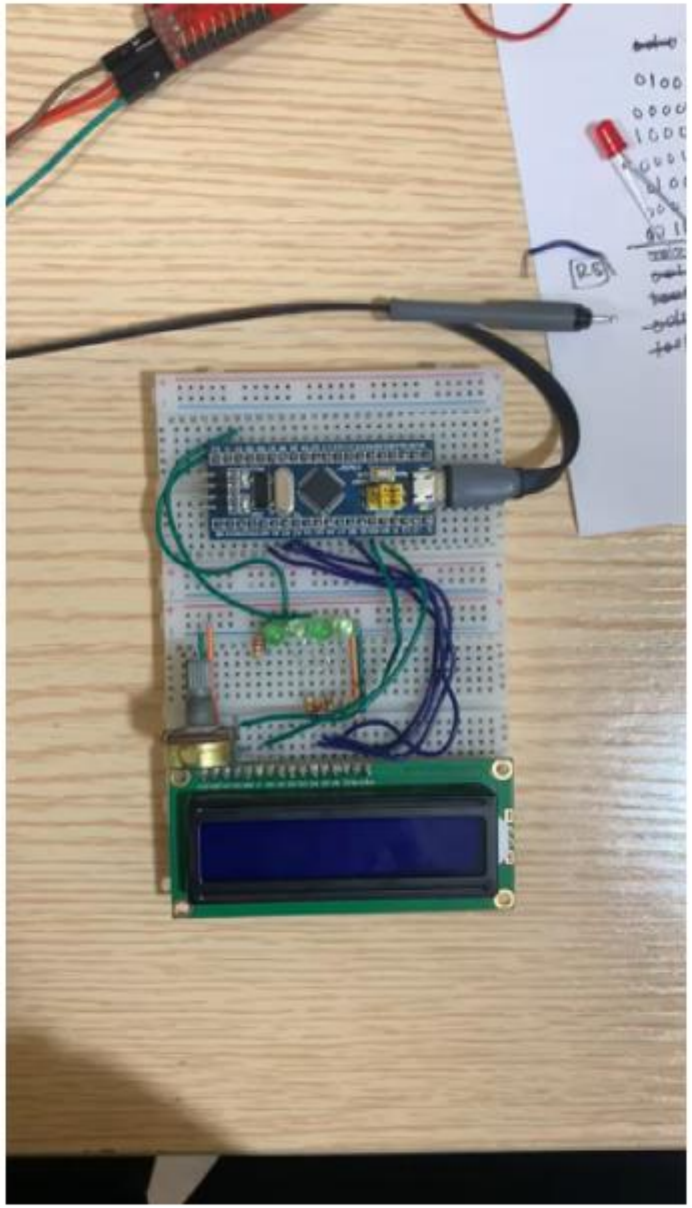
0010 0000 (4-bit mode, 1 line)
0000
0001 (Clear display)
0000
0010 (Return home)
0000
1100 (Display on, no cursor)
XXXX
XXXX (Write data to screen)



ASCII Code: Character to Binary

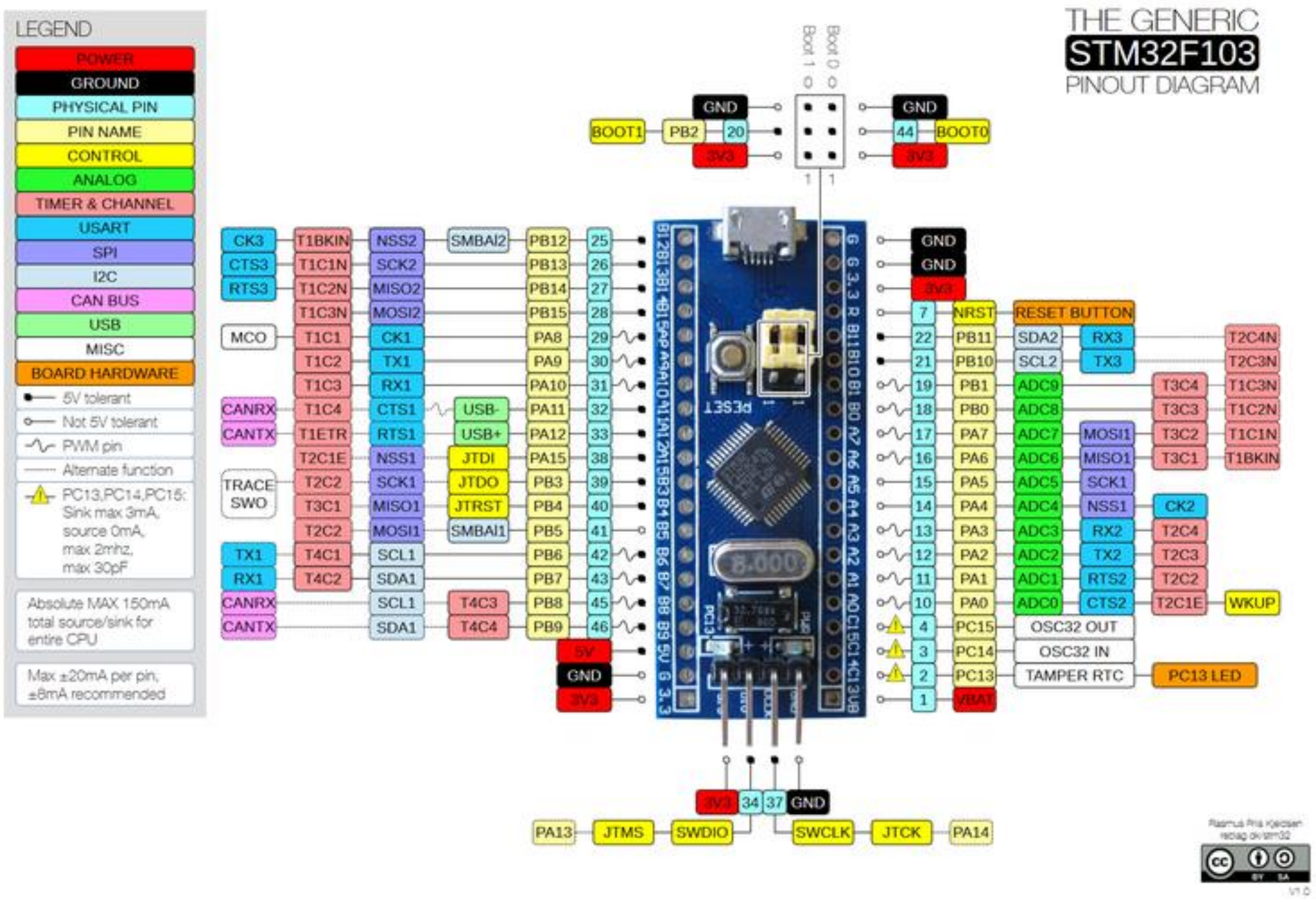
0	0011 0000	O	0100 1111	m	0110 1101
1	0011 0001	P	0101 0000	n	0110 1110
2	0011 0010	Q	0101 0001	o	0110 1111
3	0011 0011	R	0101 0010	p	0111 0000
4	0011 0100	S	0101 0011	q	0111 0001
5	0011 0101	T	0101 0100	r	0111 0010
6	0011 0110	U	0101 0101	s	0111 0011
7	0011 0111	V	0101 0110	t	0111 0100
8	0011 1000	W	0101 0111	u	0111 0101
9	0011 1001	X	0101 1000	v	0111 0110
A	0100 0001	Y	0101 1001	w	0111 0111
B	0100 0010	Z	0101 1010	x	0111 1000
C	0100 0011	a	0110 0001	y	0111 1001
D	0100 0100	b	0110 0010	z	0111 1010
E	0100 0101	c	0110 0011	.	0010 1110
F	0100 0110	d	0110 0100	,	0010 0111
G	0100 0111	e	0110 0101	:	0011 1010
H	0100 1000	f	0110 0110	;	0011 1011
I	0100 1001	g	0110 0111	?	0011 1111
J	0100 1010	h	0110 1000	!	0010 0001
K	0100 1011	I	0110 1001	'	0010 1100
L	0100 1100	j	0110 1010	"	0010 0010
M	0100 1101	k	0110 1011	(	0010 1000
N	0100 1110	l	0110 1100	)	0010 1001
				space	0010 0000

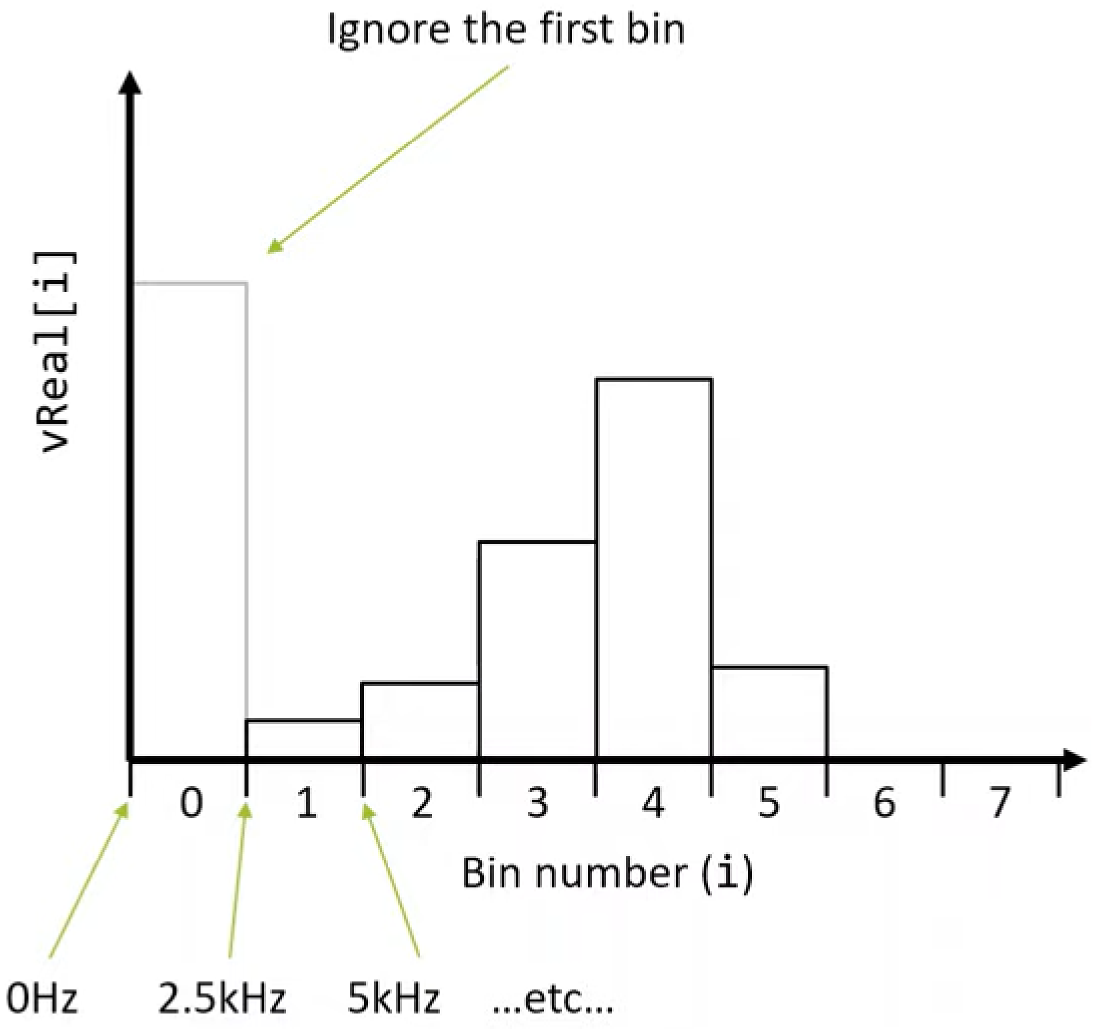


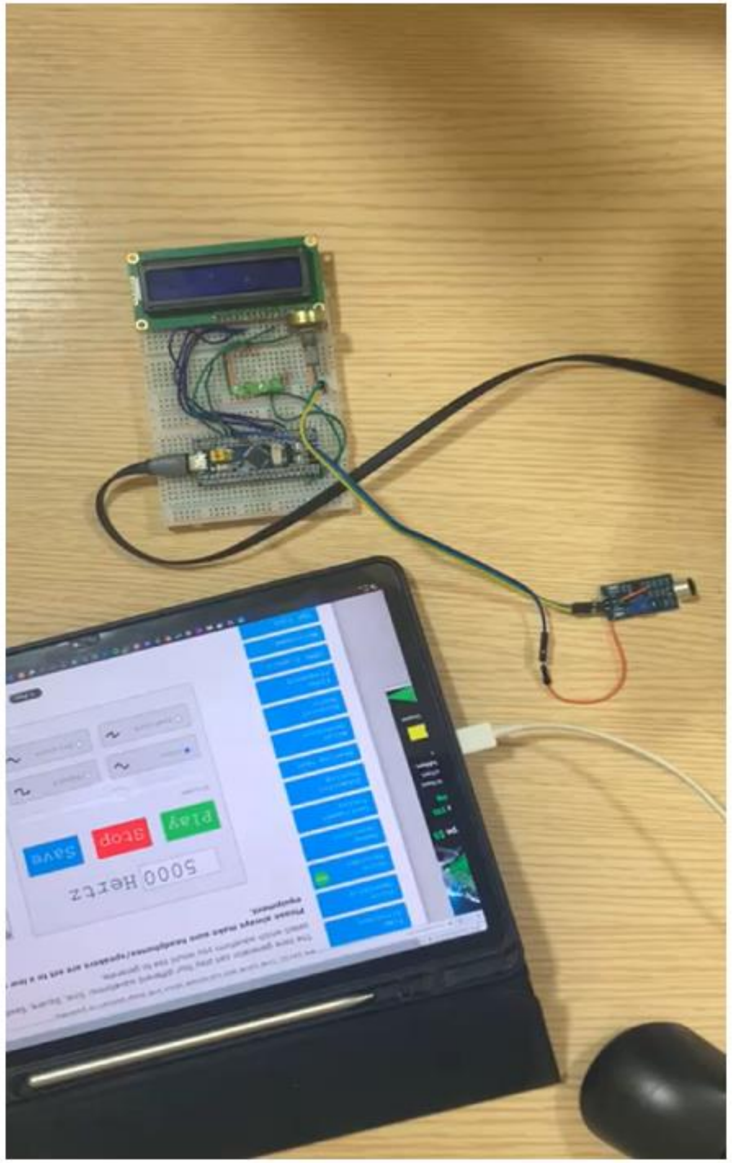


```
void writeHexBits(byte hexValue, bool high) {
  byte lastFourBits = (hexValue >> 4) & 0x0F; // Get the first 4 bits of the hex value
  byte firstFourBits = hexValue & 0x0F; // Get the last 4 bits of the hex value
  digitalWrite(RS, LOW);
  digitalWrite(EN, LOW);

  for (int i = 0; i < 4; i++) {
    digitalWrite(pinMap[i], (firstFourBits >> i) & 0x01); // Write the first 4 bits to pins 0 to 3
  }
  delay(50);
  digitalWrite(EN, HIGH); delay(50); digitalWrite(EN, LOW);
  delay(100);
  if (high) {
    for (int i = 0; i < 4; i++) {
      digitalWrite(pinMap[i], (lastFourBits >> i) & 0x01); // Write the last 4 bits to pins 0 to
    }
    delay(50);
    digitalWrite(EN, HIGH); delay(50); digitalWrite(EN, LOW);
    delay(100); // Wait for 1 second
  }
```

```
void writeCharBits(char c) {
  digitalWrite(RS, HIGH);
  digitalWrite(EN, LOW);
  byte firstFourBits = (c >> 4) & 0x0F; // Get the first 4 bits of the ASCII character
  byte lastFourBits = c & 0x0F; // Get the last 4 bits of the ASCII character

  for (int i = 0; i < 4; i++) {
    digitalWrite(pinMap[i], (firstFourBits >> i) & 0x01); // Write the first 4 bits to pins 0 to 3
  }
  delay(50); // Wait for 0.1 second
  digitalWrite(EN, HIGH); delay(50); digitalWrite(EN, LOW);
  delay(100);
  for (int i = 0; i < 4; i++) {
    digitalWrite(pinMap[i], (lastFourBits >> i) & 0x01); // Write the last 4 bits to pins 0 to 3
  }
  delay(50);
  digitalWrite(EN, HIGH); delay(50); digitalWrite(EN, LOW);
  delay(100);
  digitalWrite(RS, LOW);
}
```


THE GENERIC
STM32F103
PINOUT DIAGRAM
LEGEND
POWER
GROUND
PHYSICAL PIN
PIN NAME
CONTROL
ANALOG
TIMER & CHANNEL
USART
SPI
I2C
CAN BUS
USB
MISC
BOARD HARDWARE
5V tolerant
Not 5V tolerant
PWM pin
Alternate function
PC13,PC14,PC15: Sink max 3mA, source 0mA, max 2mhz, max 30pF
Absolute MAX 150mA total source/sink for entire CPU
Max ±20mA per pin, ±8mA recommended
Boot 1
Boot 0
GND
BOOT1 PB2 20
3V3
GND
44 BOOT0
3V3
CK3 T1BKIN NSS2 SMBAI2 PB12 25
CTS3 T1C1N SCK2 PB13 26
RTS3 T1C2N MISO2 PB14 27
T1C3N MOSI2 PB15 28
MCO T1C1 CK1 PA8 29
T1C2 TX1 PA9 30
T1C3 RX1 PA10 31
CANRX T1C4 CTS1 USB- PA11 32
CANTX T1ETR RTS1 USB+ PA12 33
T2C1E NSS1 JTDI PA15 38
TRACE SWO T2C2 SCK1 JTDO PB3 39
T3C1 MISO1 JTRST PB4 40
T3C2 MOSI1 SMBAI1 PB5 41
TX1 T4C1 SCL1 PB6 42
RX1 T4C2 SDA1 PB7 43
CANRX SCL1 T4C3 PB8 45
CANTX SDA1 T4C4 PB9 46
5V
GND
3V3
GND
GND
3V3
7 NRST RESET BUTTON
22 PB11 SDA2 RX3 T2C4N
21 PB10 SCL2 TX3 T2C3N
19 PB1 ADC9 T3C4 T1C3N
18 PB0 ADC8 T3C3 T1C2N
17 PA7 ADC7 MOSI1 T3C2 T1C1N
16 PA6 ADC6 MISO1 T3C1 T1BKIN
15 PA5 ADC5 SCK1
14 PA4 ADC4 NSS1 CK2
13 PA3 ADC3 RX2 T2C4
12 PA2 ADC2 TX2 T2C3
11 PA1 ADC1 RTS2 T2C2
10 PA0 ADC0 CTS2 T2C1E WKUP
4 PC15 OSC32 OUT
3 PC14 OSC32 IN
2 PC13 TAMPER RTC PC13 LED
1 VBAT
3V3 34 37 GND
PA13 JTMS SWDIO
SWCLK JTCK PA14
RESET
8.000
Rasmus Friis Kjeldsen
reblag.dk/stm32
V1.0

Ignore the first bin
vReal[i]
0
1
2
3
4
5
6
7
Bin number (i)
0Hz
2.5kHz
5kHz
...etc...


5000 Hertz
Play
Stop
Save

VCC
GND
OUT
FC-04