
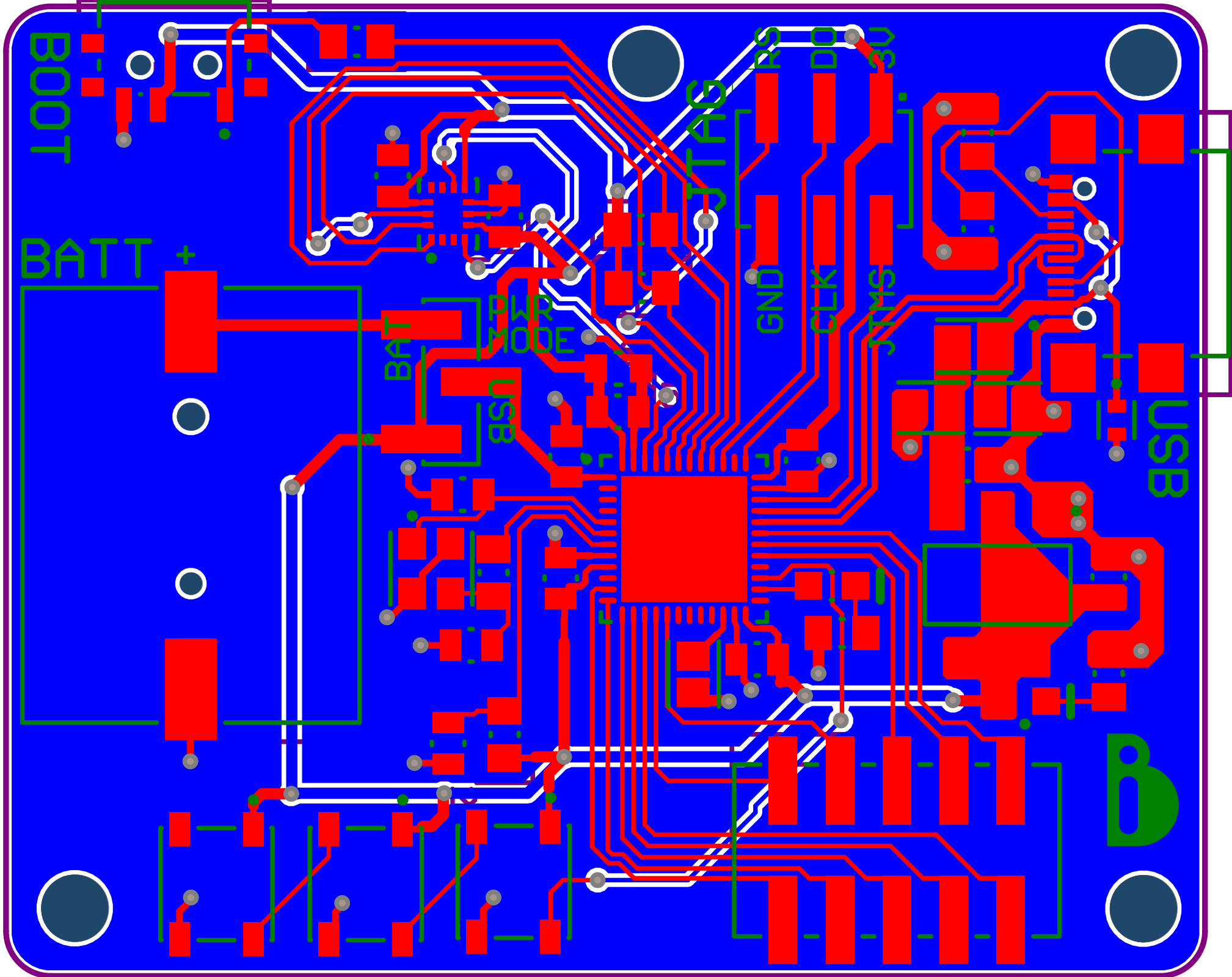


APPROVALS		PROJECT			
ENG:	DATE	PROJECT #			
DSN:		PROJECT REVISION			
CHK:		DOCUMENT REVISION		DESIGN TEXT	
REFERENCE DOCUMENTS		TITLE		26ac61983a2f29b0d201e60011334420100696c1f8bc9a259fa9	
BOM:		*		A	
ASSY DWG:	SIZE	CAGE CODE	DWG NO.	REV	
FAB DWG:	B				
PCB DWG:	SCALE:	FILE NAME	MCU_SchDoc	SHEET	1 of 1



BOOT

BATT +

BATT

USB

PLW
MODE

JTAG

GND

CLK

JTAG

RS

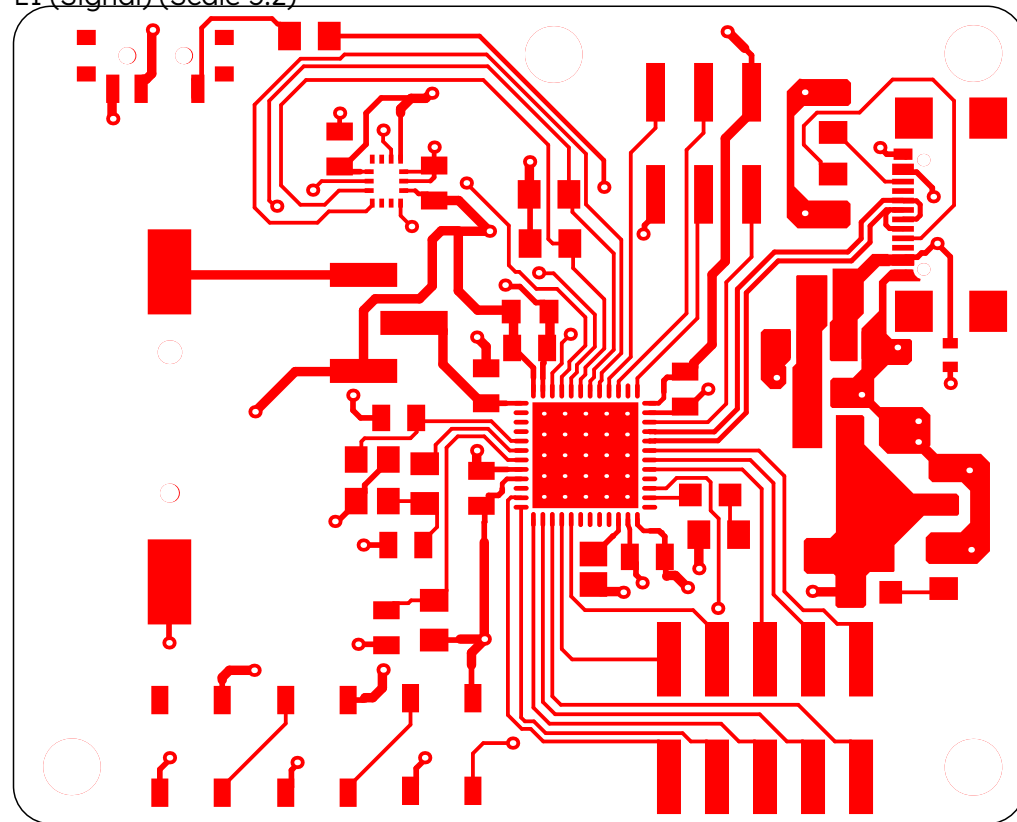
DO

3U

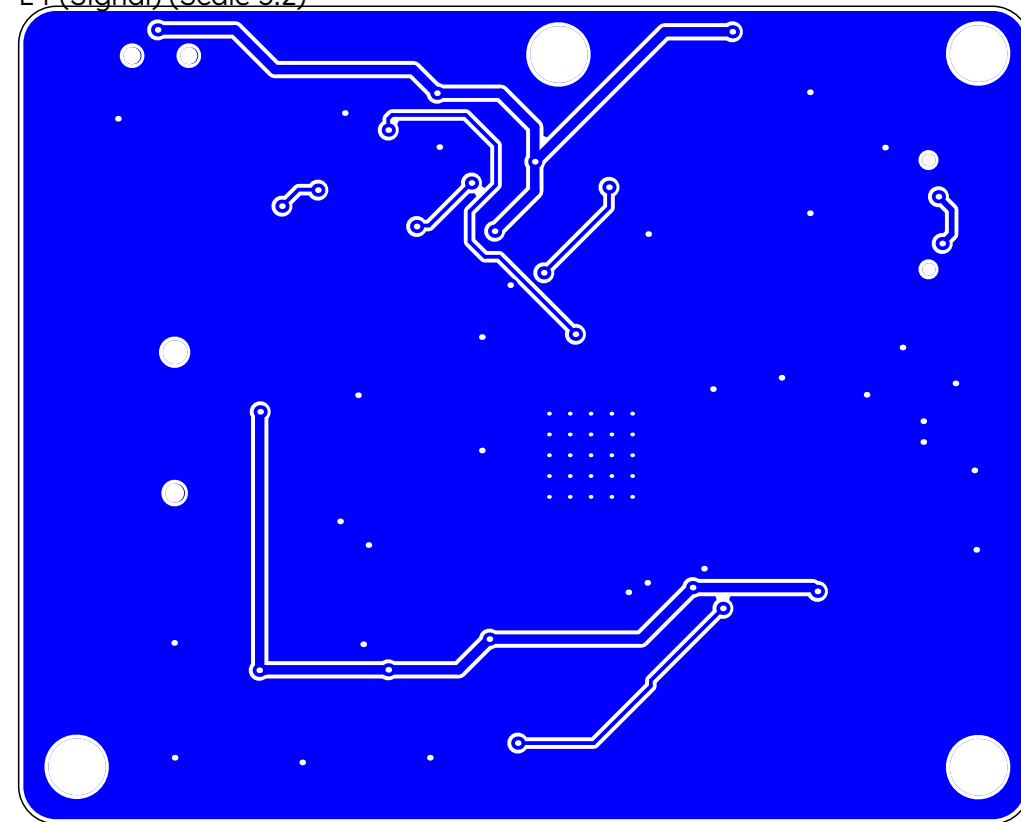
USB

B

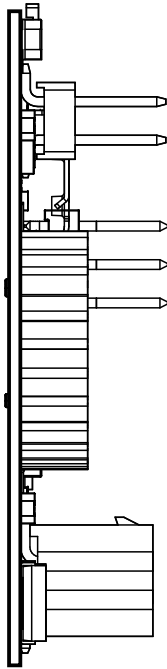
L1 (Signal) (Scale 5:2)



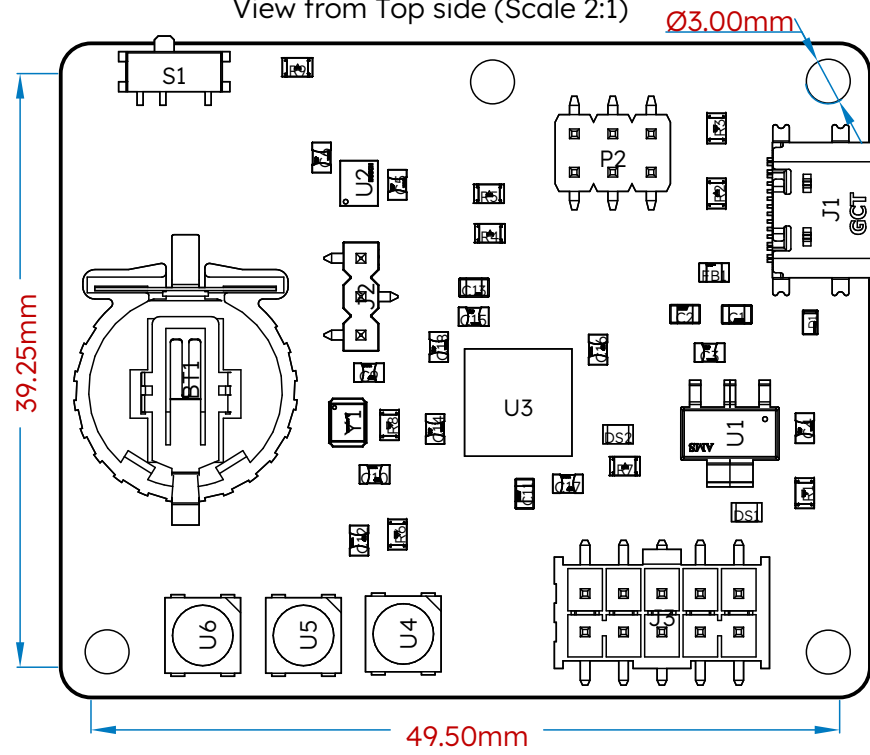
L4 (Signal) (Scale 5:2)



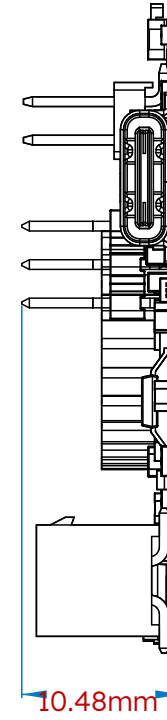
View from Left side (Scale 2:1)



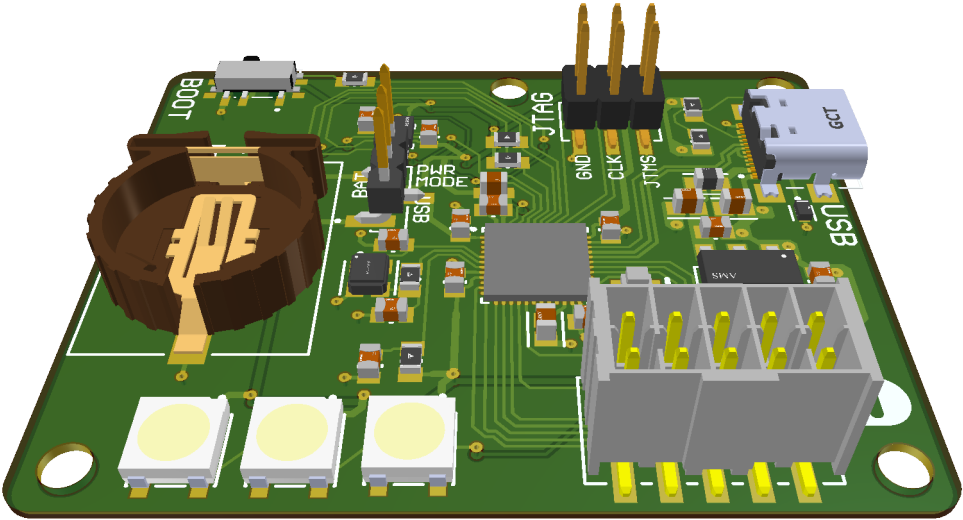
View from Top side (Scale 2:1)



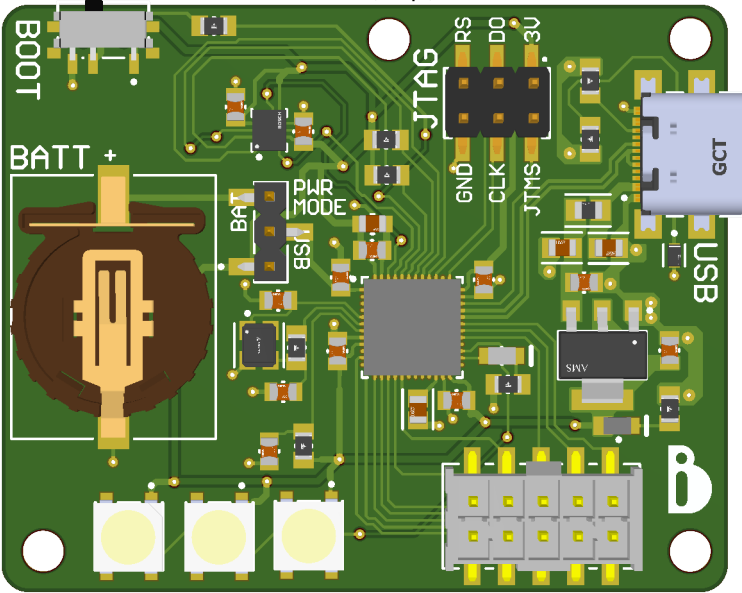
View from Right side (Scale 2:1)



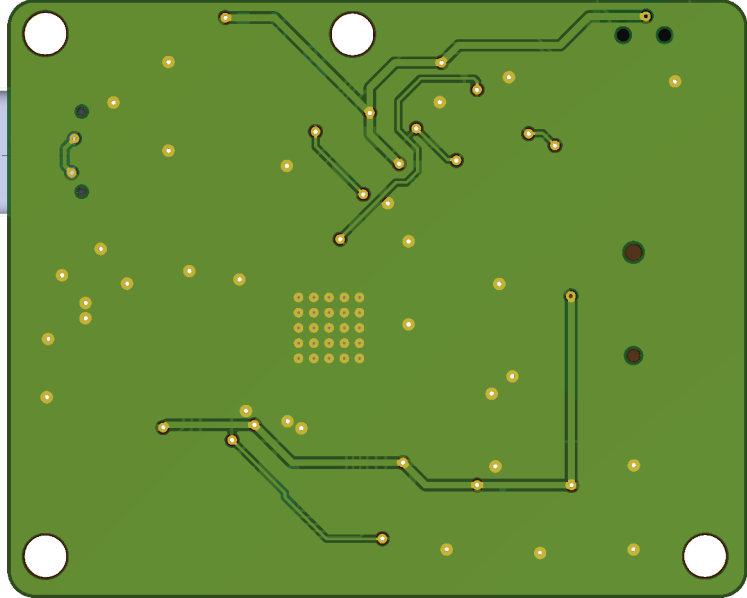
3D Isometric View



3D View (Top)



3D View (Bottom)



Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.03mm	SM-001	Solder Mask	GTS
PbSn	Top Surface Finish	0.02mm		Surface Finish	
CF-004	L1 (Signal)	0.02mm		Signal	GTL
Core		0.66mm	Core-039	Dielectric	
CF-004	L4 (Signal)	0.02mm		Signal	GBL
PbSn	Bottom Surface Finish	0.02mm		Surface Finish	
Surface Material	Bottom Solder	0.03mm	SM-001	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
Total thickness: 0.79mm					

Bill Of Materials

Line #	Designator	Comment	Quantity	Number of Pins	Package	Number of Positions
1	BT1	CR-1220	1			
2	C1, C2, C11	2u2	3	2		
3	C3, C4, C5, C6, C9, C10, C12, C14, C15, C16, C17, C18	22u, 100n, 10p	12		CC0805-0.85	
4	C13	4.7u	1	2		
5	D1	ESDA7P120-1U1M	1		QFN1610	
6	DS1	1K	1			
7	DS2	LTST-C170KRKT	1	2		
8	FB1	120R	1	2		
9	J1	USB4110-GF-A	1		0	
10	J2	5-146128-1	1		HDR3	
11	J3	IPL1-105-02-S-D-K	1			10
12	P2	JTAG CONN	1	6		6
13	R1, R2, R3, R4, R5, R6, R7, R8, R9	1K, 5K1, 2K2, 10K, OR	9			
14	S1	PCM12SMTR	1			
15	U1	AMS1117-3.3	1		AMS1117	
16	U2	BMI160	1			
17	U3	STM32F411CEU6	1			
18	U4, U5, U6	SK6812	3			
19	Y1	24MHz	1	4		