

# Side Channels

**System Security (CM0625, CM0631) 2022-23** Università Ca' Foscari Venezia

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https://matteobusi.github.io/

https://xkcd.com/1938/

## An appetizer [Van Bulck et al., 2018]

https://youtu.be/8ZF6kX6z7pM

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[Van Bulck et al., 2018] Van Bulck et al. "Foreshadow: Extracting the Keys to the Intel SGX Kingdom with Transient Out-of-Order Execution." USENIX Security 2018.

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- Constant-time programs
- Speculative execution
- Speculative leaks
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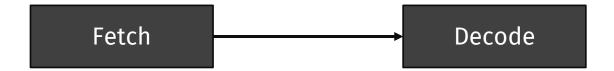
#### What's all this jargon?

We'll spend the next 1.5 hours trying to decode the jargon

Remember how CPUs work?

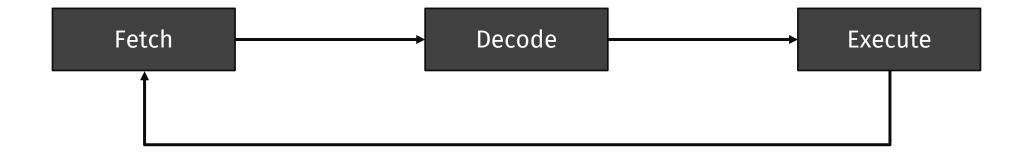
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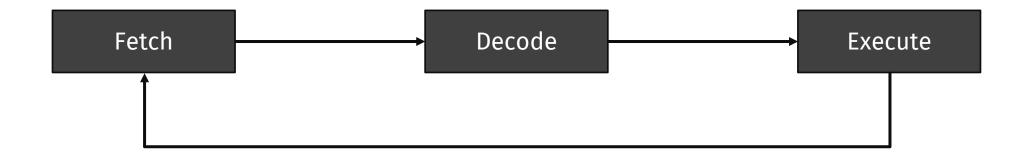








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**Problem:** not very efficient (≥1 cycle per stage)

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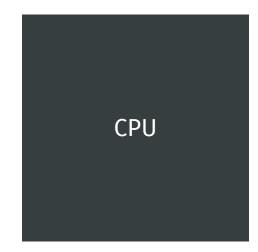
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- First idea: make cycles "shorter", i.e., increase the processor's clock
  - We can reach about 4 GHz
  - **Very good**, but ~2004 we reached the peak
  - Also: power-consumption issues, too much heat, ...
- People started thinking about alternatives!
  - Idea: make the avg case faster
  - Solutions: caches, speculation, multi-core, multi-thread, ...

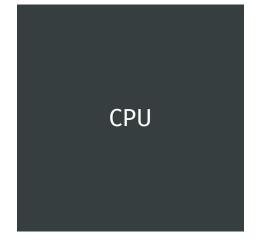
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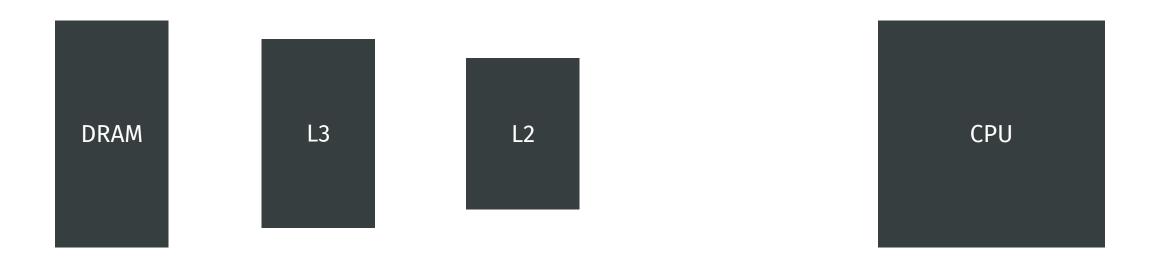




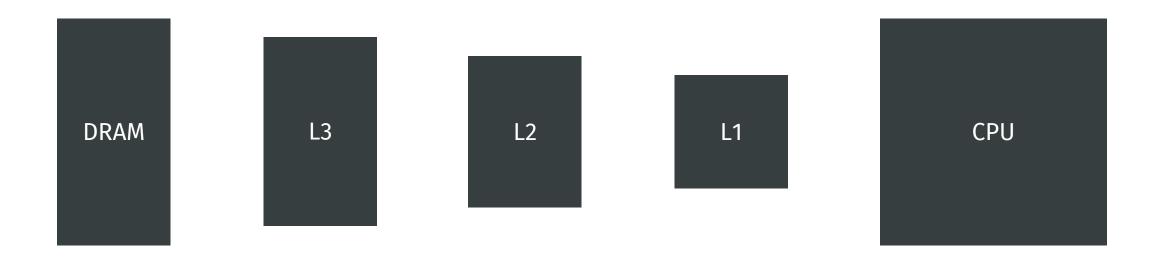
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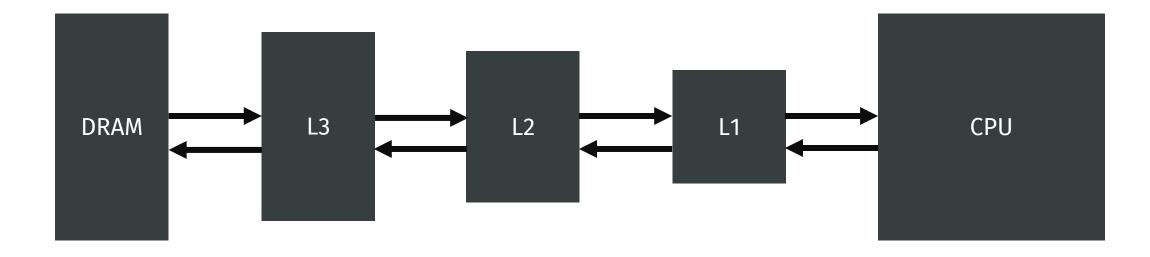
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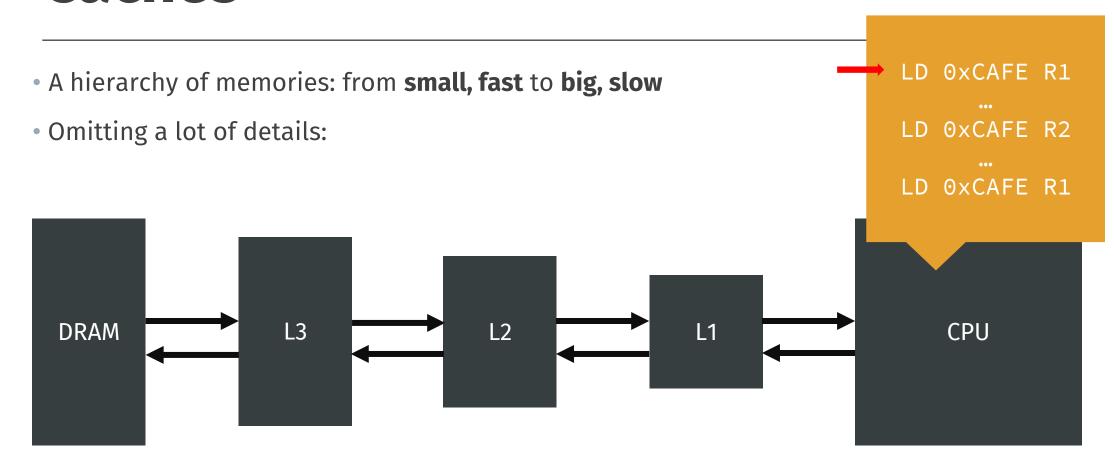


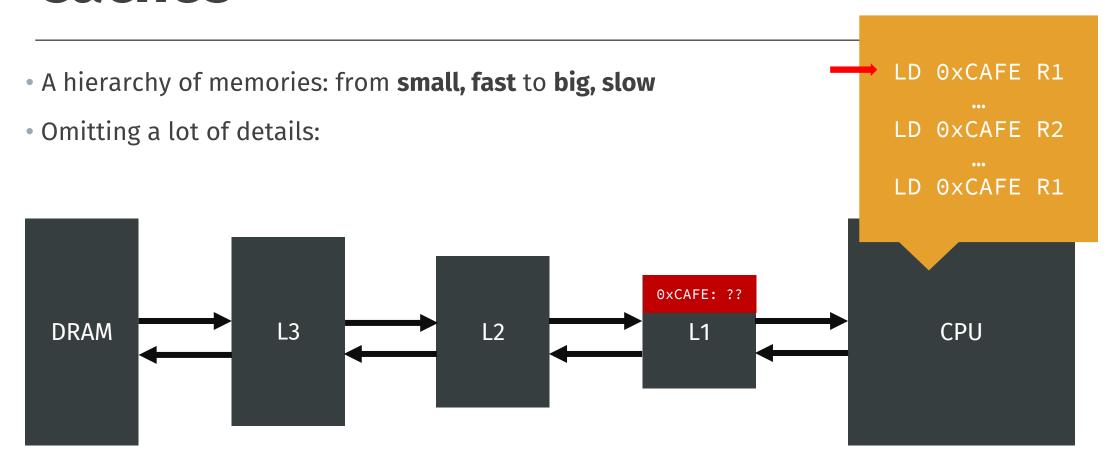
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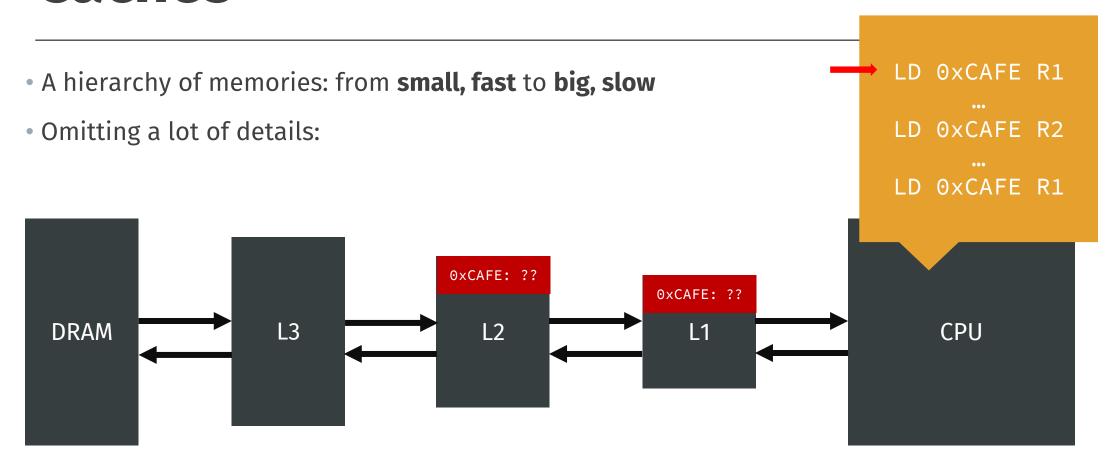


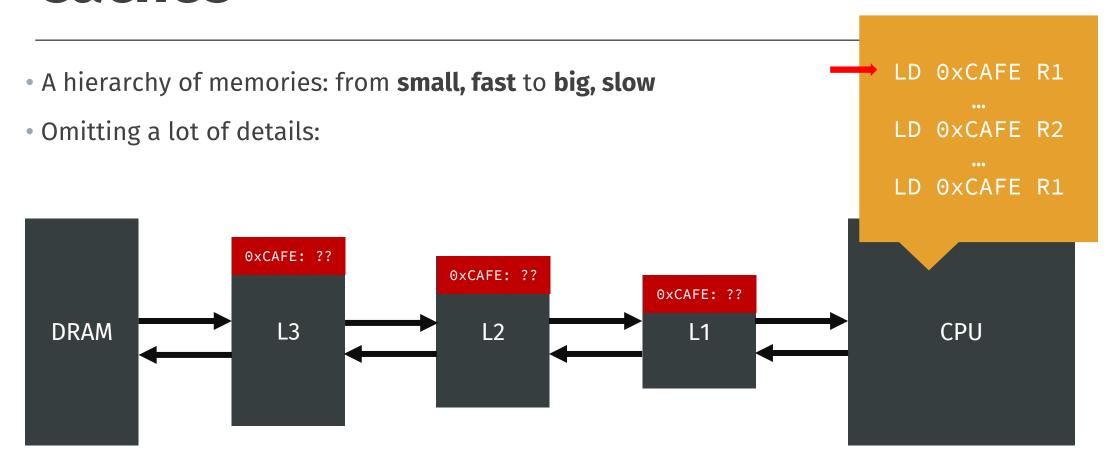
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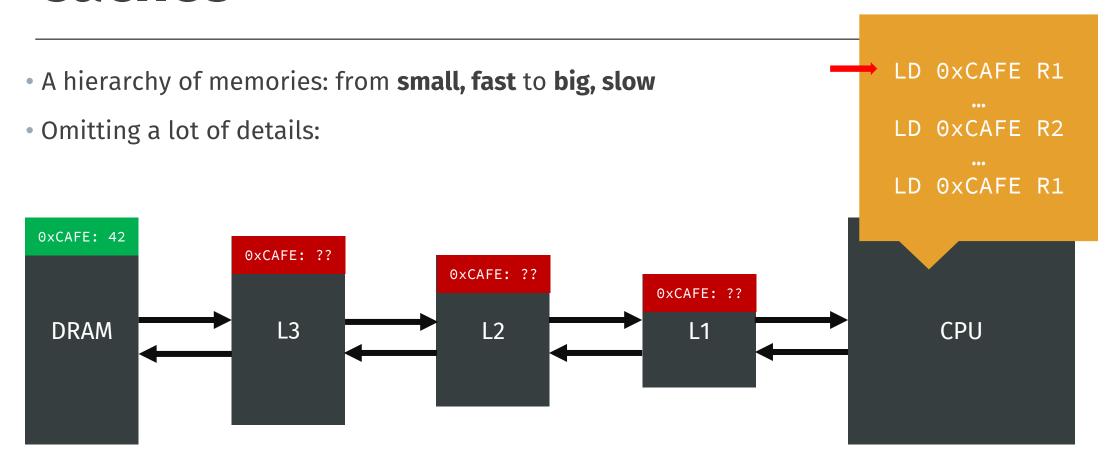


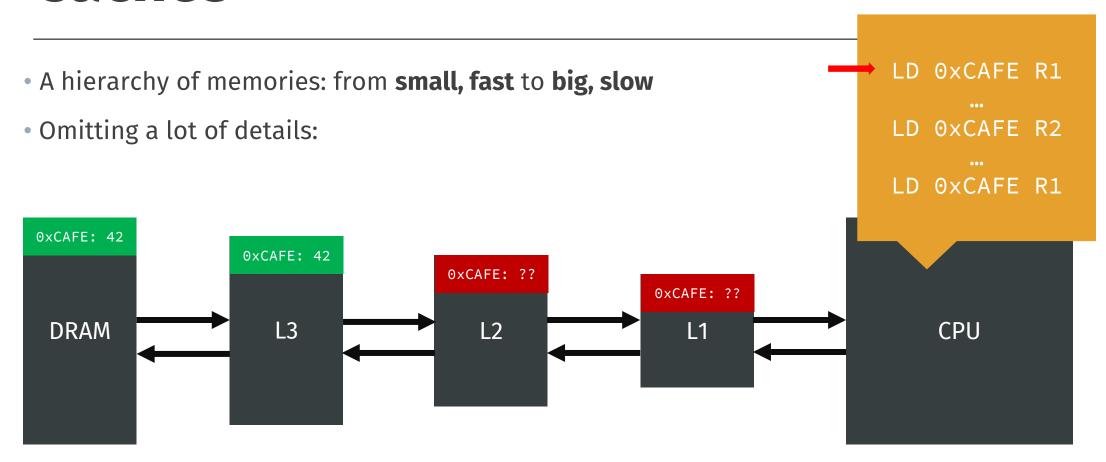


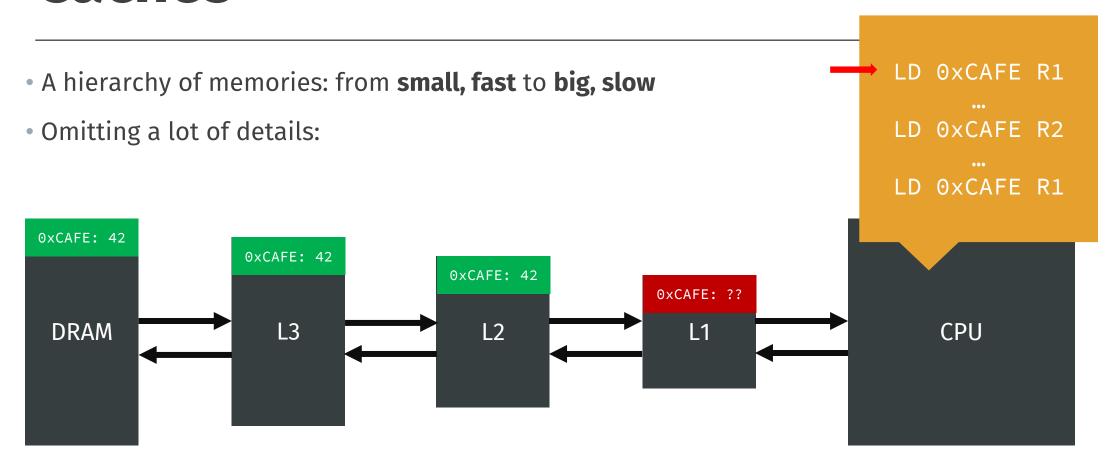


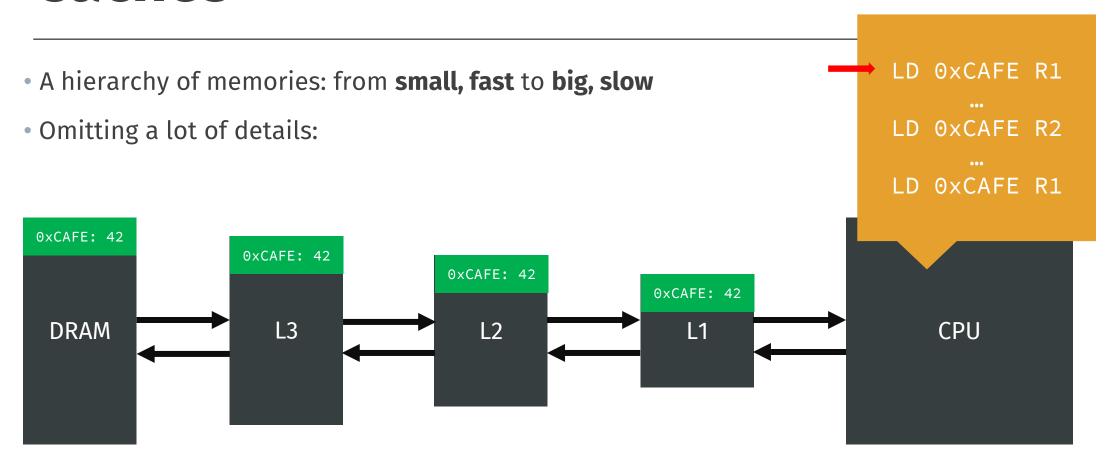


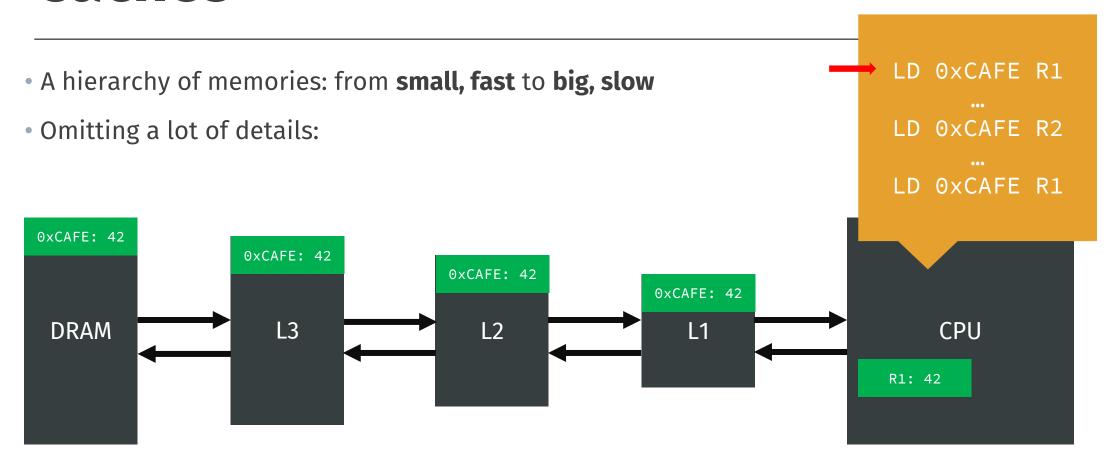


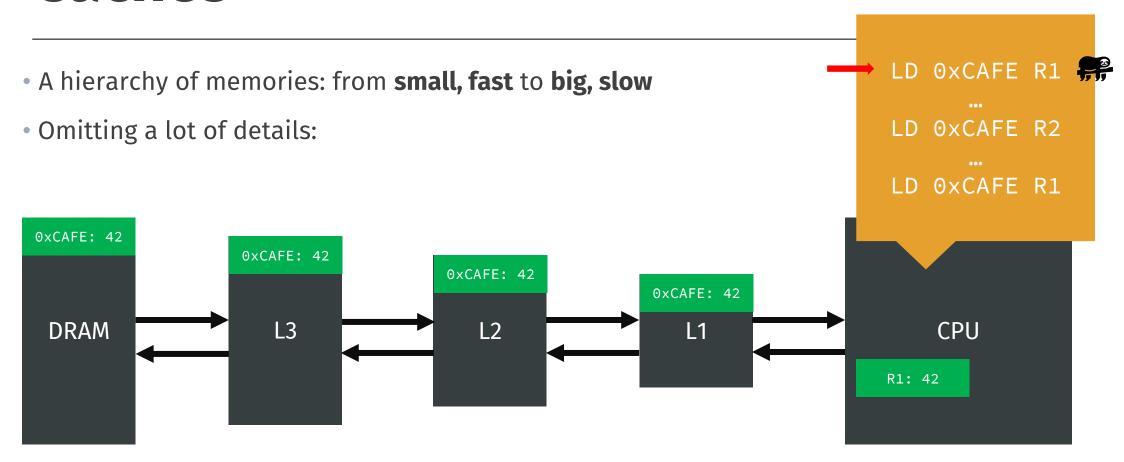


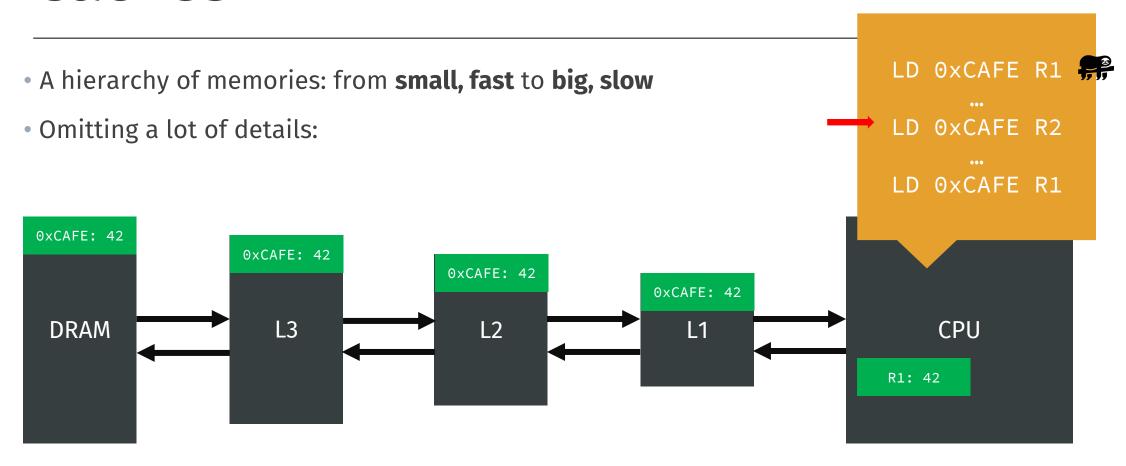


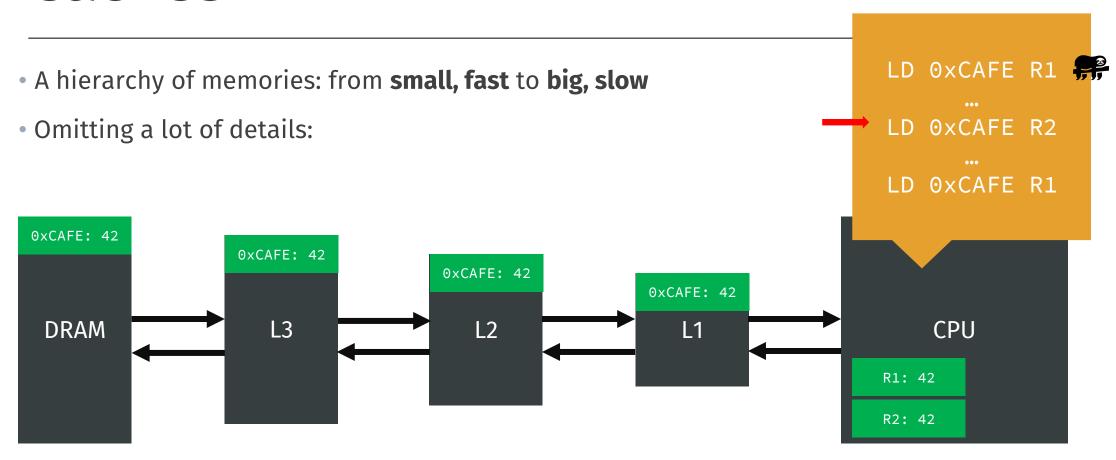


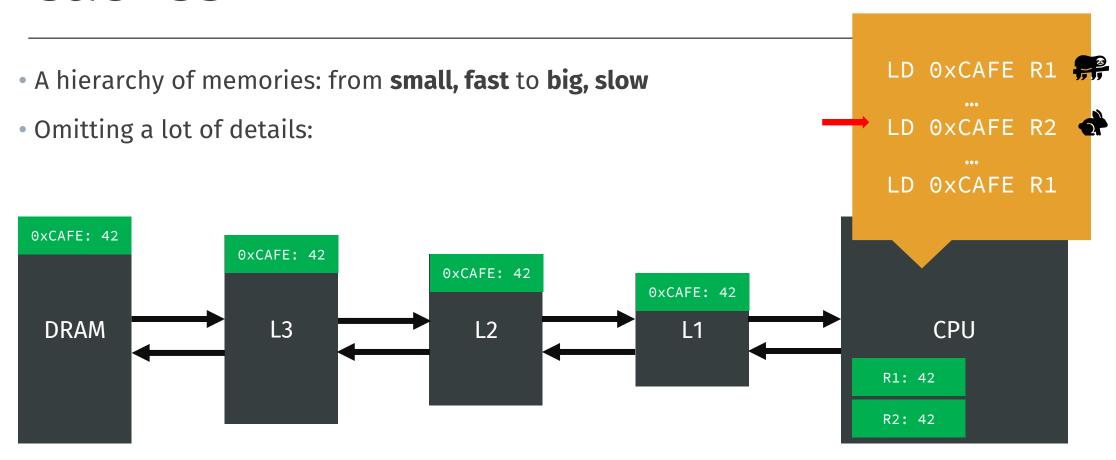


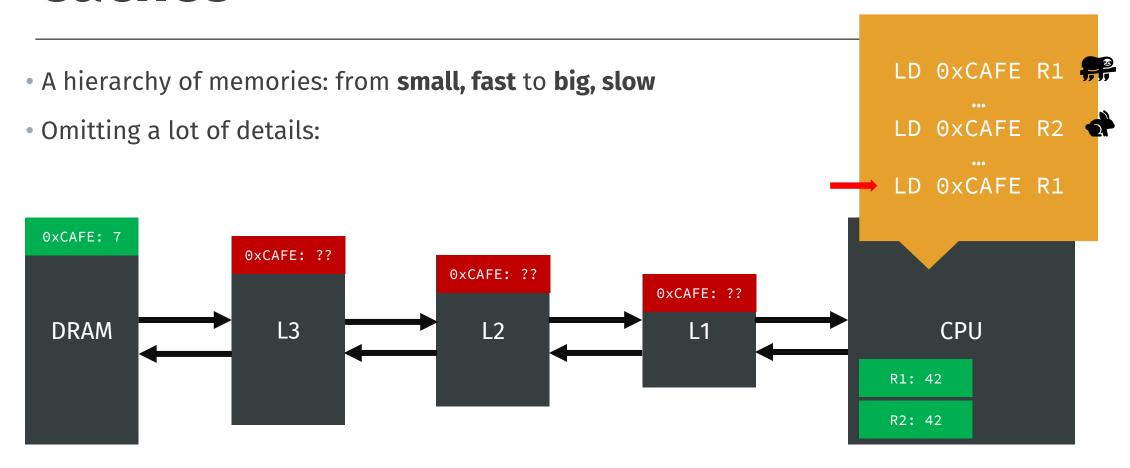


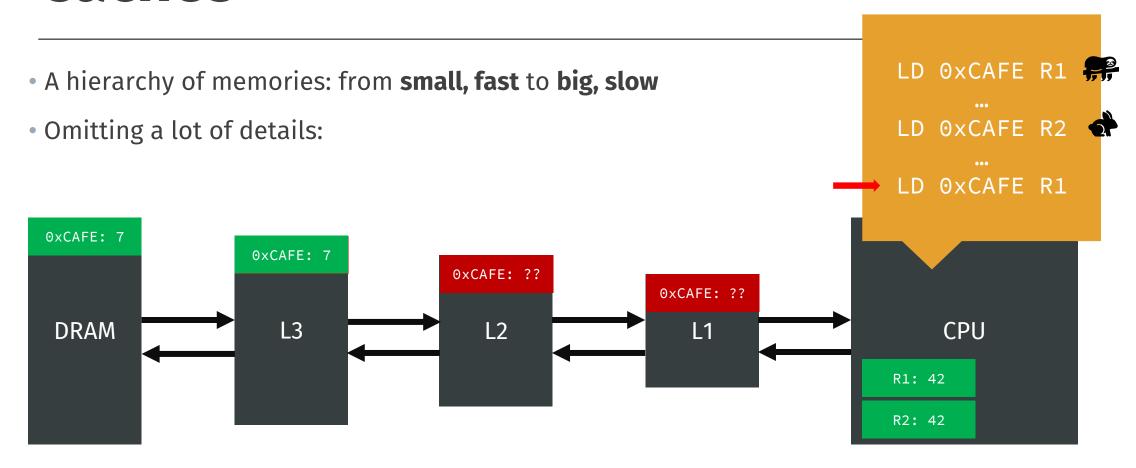


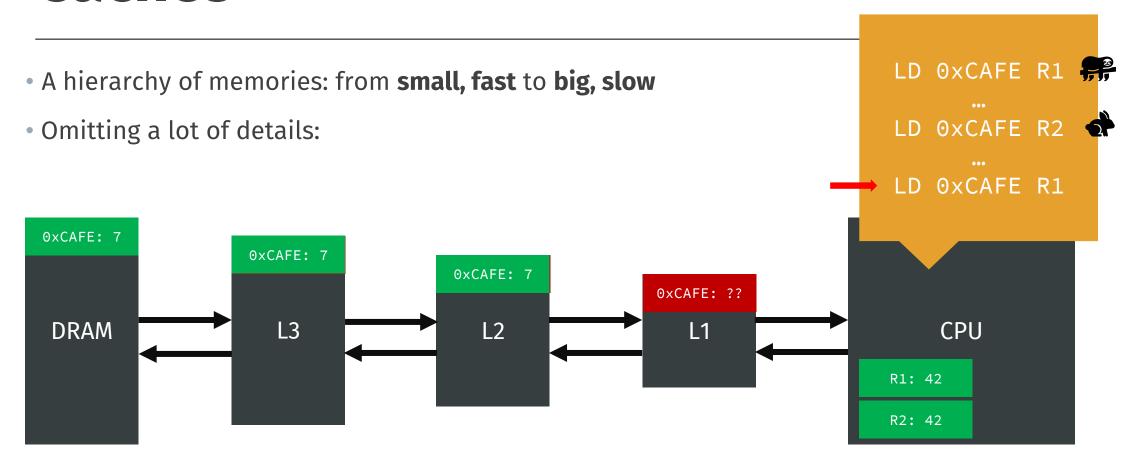


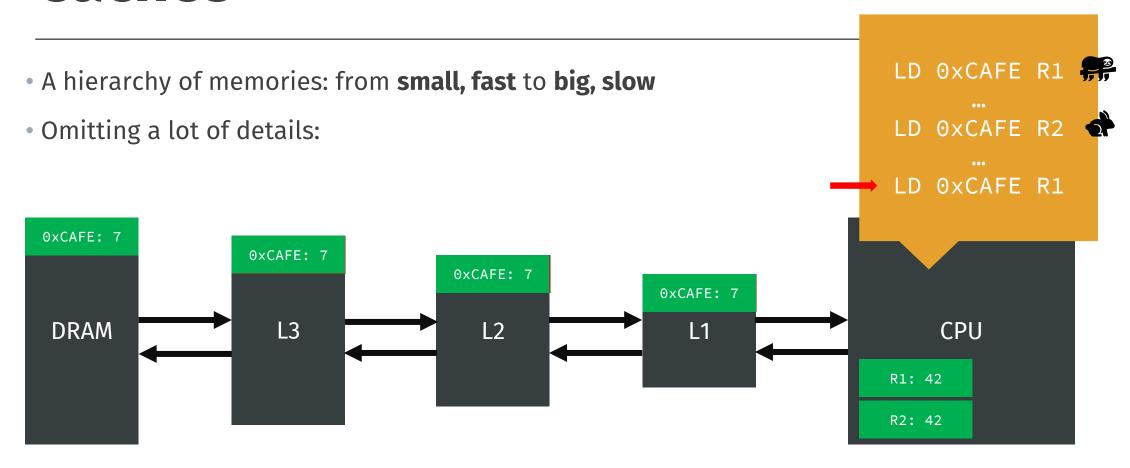


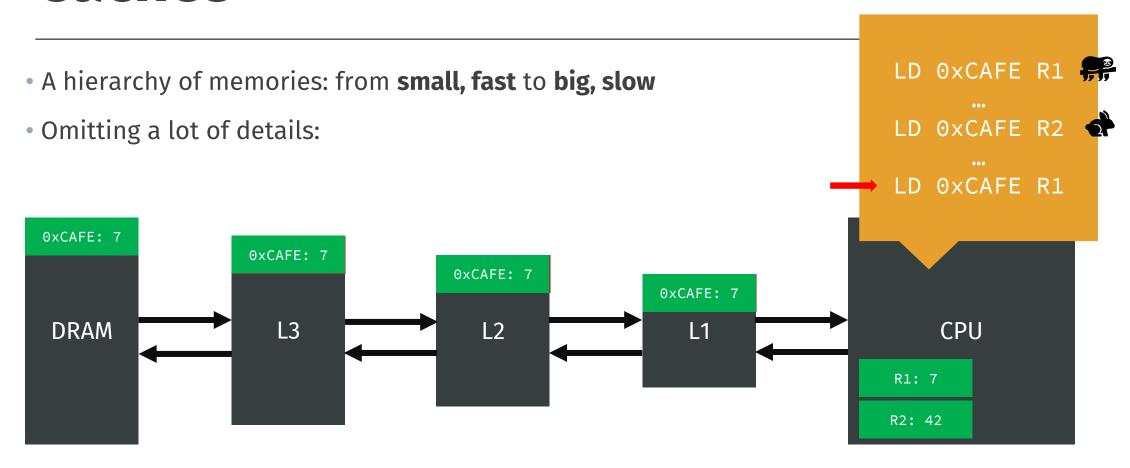


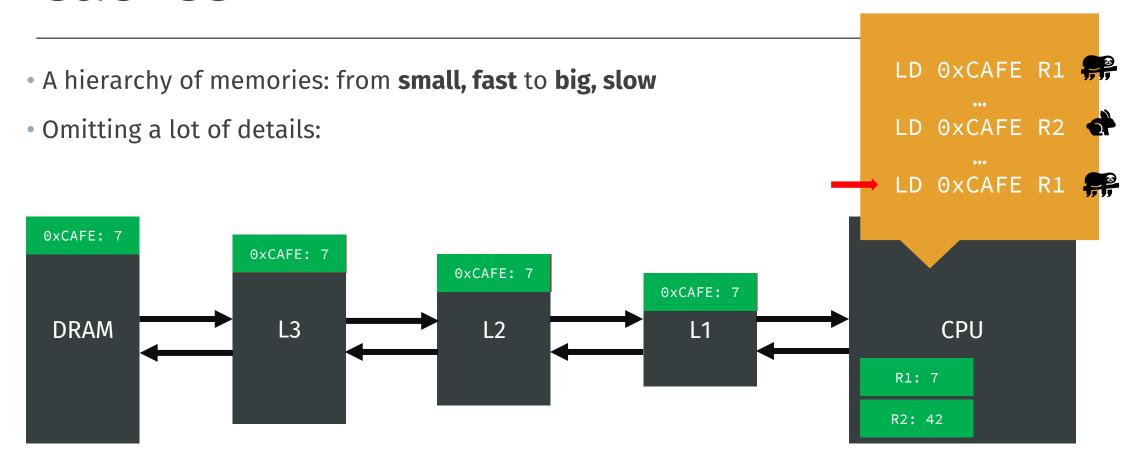












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  - Roughly: should the CPU take the next branch?
  - The CPU trains its branch predictor by observing what happened before
  - Modern branch predictors are complex
    - but for our purposes just one bit telling if we should take the branch!



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  if val >= 0
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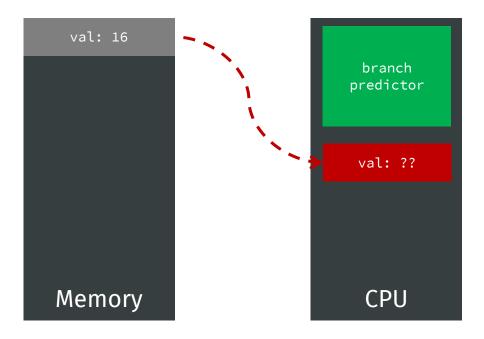




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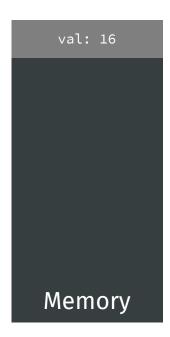








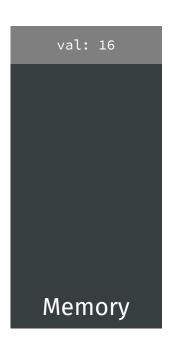
The CPU was right: commit the changes!





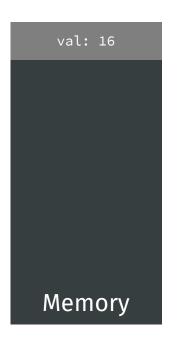
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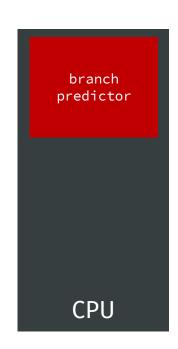
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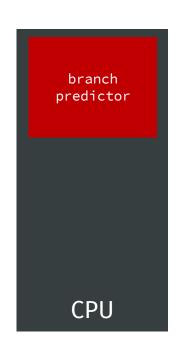
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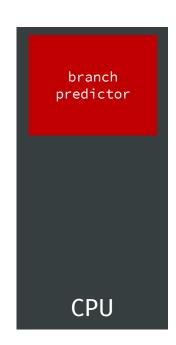




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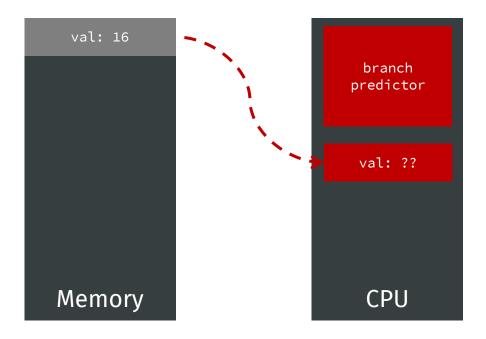
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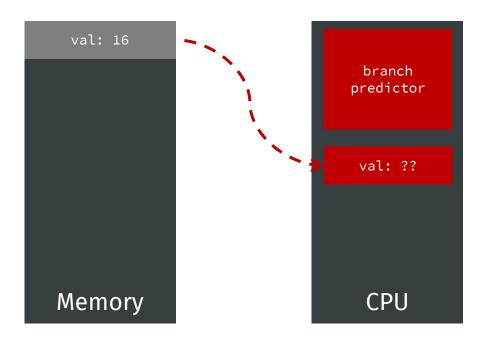
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→ if val >= 0
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→ bar (); rollback!
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#### More precisely:

"A **side channel** is any observable side effect of computation that an attacker could <u>measure</u> and <u>possibly influence</u>." [Lawson, 2009]

# Your first sidechannel attack

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  - Find a line from the cache shared between the attacker and the victim and flush it
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    - Otherwise, the read will be slow

[Yarom&Falkner, 2014] Y. Yarom, K. Falkner. "FLUSH+RELOAD]: A High Resolution, Low Noise, L3 Cache Side-Channel Attack." USENIX Security 2014.

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A[0 \* 512]A[1 \* 512] A[2 \* 512]A[N \* 512  $A[A_sz - 1]$ Memory

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  - 2. The attacker scans A, measuring access time for each A[i \* 512]:
    - for i = N the access will be fast, the secret is leaked!

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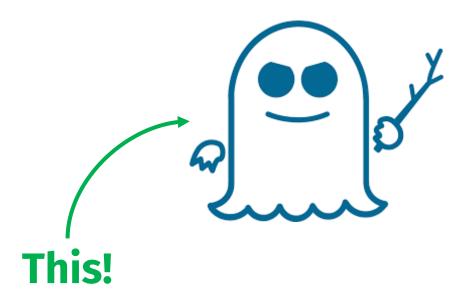


## Mitigating FLUSH+RELOAD

- Detecting **FLUSH+RELOAD**: Anomalous cache hit/misses patterns using HW performance counters
- Mitigating FLUSH+RELOAD:
  - **Software-based:** fix victims avoiding secret-dependent memory accesses; disable page sharing/de-duplication; limit access to high-resolution timers
  - Hardware-based: limit clflush access; make caches non-inclusive

The **Spectre** attack!

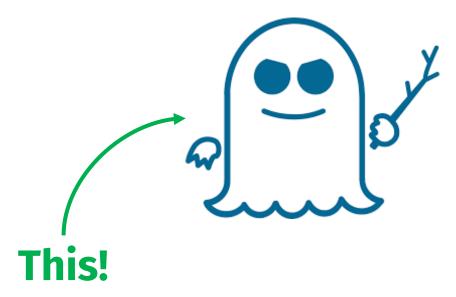
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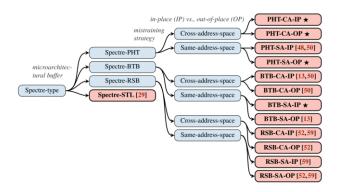




### Spectre [Kocher et al., 2019]

#### **Spectre** is an attack exploiting **speculative execution** to **leak secrets**

- It is part of a recent wave of **micro-architectural attacks**, i.e., attacks using side-channels induced by the micro-architecture of a processor (e.g., cache, timers, virtual memory, ...)
- "Spectre [...] transiently bypasses software-defined security policies (e.g., bounds checking, function call/return abstractions, memory stores) to leak secrets out of the program's intended code/data paths." [Canella et al., 2019] (← bit outdated, but a good survey on Spectre!)
- Many variants, here an updated version <a href="https://transient.fail/">https://transient.fail/</a>



## Spectre v1/v1.1 (special-cases of PHT)

#### We focus on Spectre v1 and v1.1

- Also called Spectre-PHT: the attacker mistrains the branch predictor by poisoning the Pattern History Table
- How? For example
  - The attacker:
    - 1. Looks for a piece of "vulnerable code" (code gadget) including a condition (next slide)
    - 2. Runs that code multiple times with an input s.t. the condition always holds (so training the branch predictor to take the "true" branch)
    - 3. Then, runs the code with a specially-crafted input making the condition false: now the CPU mis-speculates and executes the "true" branch with wrong data (!!!)
    - 4. Finally, it looks for information left behind after the CPU discovered it mis-speculated and rolled-back the computation (e.g., contents of caches)

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y = B[A[x] * 512];</pre>
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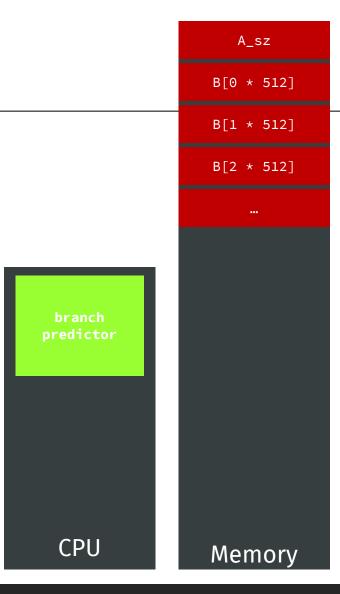
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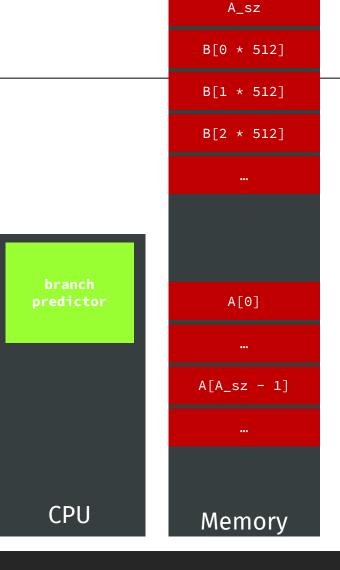
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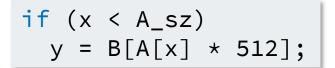
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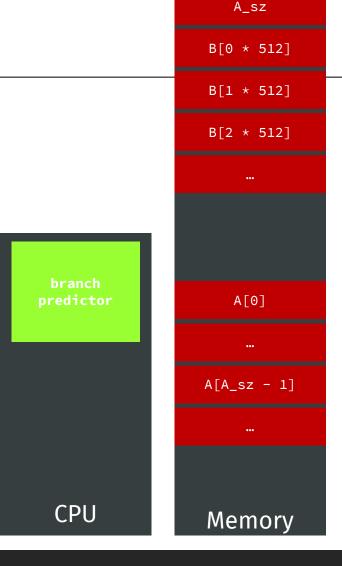


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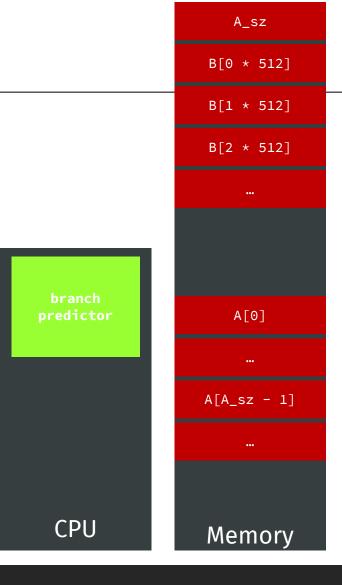
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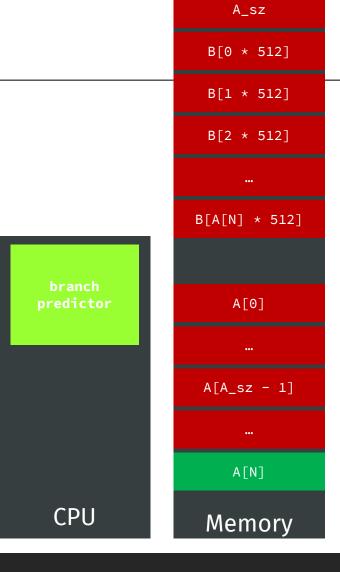
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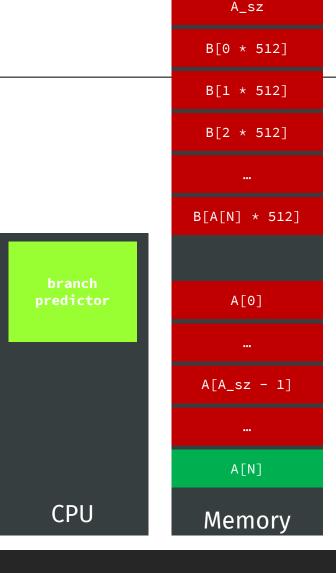
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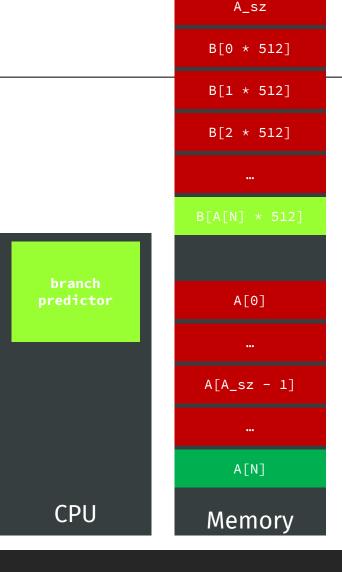
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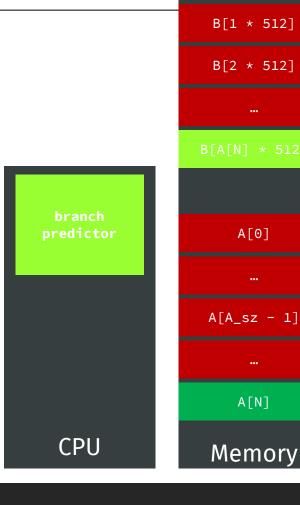


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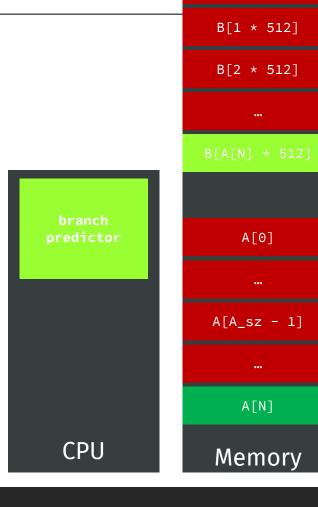


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 $A_sz$ B[0 \* 512] B[1 \* 512]B[2 \* 512]A[0]  $A[A_sz - 1]$ A[N] Memory

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- In pseudo-C:

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if (x < A_sz) {
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- It works (mostly:)
- Probably nothing else!

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- To make this a bit better one could use static analysis to decide where fences should go
  - E.g., Microsoft MSVC does that by detecting known problematic patterns or Blade tool

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- It may be more efficient to introduce an **artificial** data dependency between the condition of a jump and the pointer
- Simplifying, for Spectre v1 (assuming "\_ ? \_ : \_" to be implemented w/o branching, e.g., using a cmov)

```
uint mask = ALL_ONES;
if (cond) {
  mask = !cond ? ALL_ZEROES : mask;
  // ...
  y = B[(A[x] * 512) \& mask];
else {
  mask = cond ? ALL_ZEROES : mask;
  /* ... */
```

# Mitigating Spectre: SLH | // ... | y = B[(A[x] \* 512) & mask];

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- It works (with some changes also for other Spectre variants) }
- More efficient than fences
- No need of static analysis code (but still could help)

#### The Bad:

- Still slow (mask must be known when accessing to B, also when speculating!)
- Must be carefully implemented
- Still requires re-compilation

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# Mitigating Spectre: other ideas

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- Make secrets non reachable:
  - Just like **Chrome** and **Firefox**: isolate secrets in different processes
- Reduce the bandwidth of side-channels:
  - e.g., via shadow micro-arch state that can be discarded, less accurate timers, adding noise, ...

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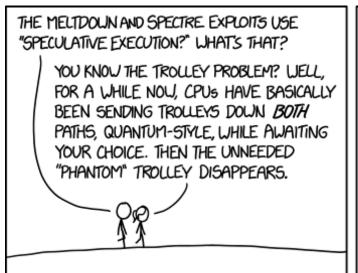
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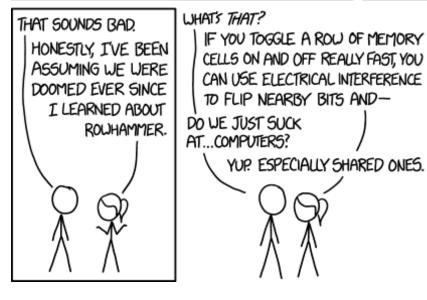
#### Is Spectre fixed?

Only if you are willing to re-compile/re-design your system and make it slow 😉

# The End









https://xkcd.com/1938/