

Assignment

Day 3

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1. Executive Summary

This report discusses each of the following topics:

- 1- The differences between Von Neumann and Harvard architectures.
- 2- The differences between RISC and CISC machines.
- 3- The differences between AHB and APB buses.

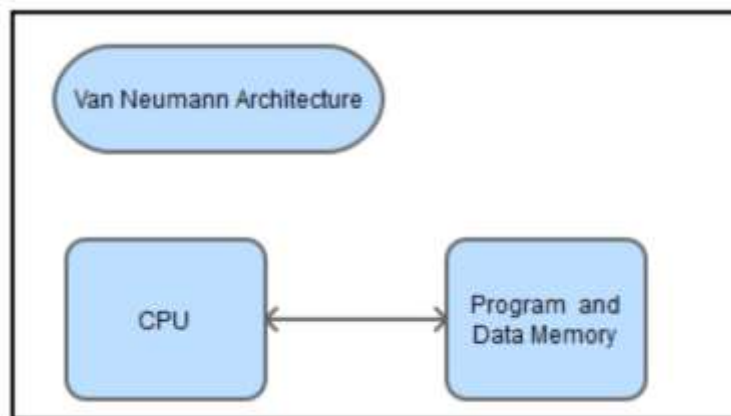
2. Von Neumann vs Harvard Arch.

The architecture of any micro-controller or a micro-computer mainly refers to the overall arrangement of the constituent CPU (it happens with respect to the ROM and RAM). Here, Harvard and Von Neumann architecture serve as the two major ways using which the microcontroller gets its CPU arrangement with the ROM and RAM.

2.1. Von Neumann Architecture

Von Neumann's primary advancement was referred to as "conditional control transfer", which had allowed a program sequence to be interrupted and then reinitiated at any point, furthermore, this advancement had allowed data to be stored with instructions in the same memory unit.

The von Neumann architecture describes a design model for a stored program digital computer that incorporates only one single processing unit and one single separate storage structure, which will hold both instructions and data.



2.1.1. Von Neumann Advantages

- The control unit retrieves instruction and data in the same way from one memory unit. This simplifies the development and design of the control unit.
- The above advantage would also mean that data from memory and from devices are accessed the same way. Therefore increasing efficiency.
- An advantageous characteristic is that programmers have control of memory organization.

2.1.2. Von Neumann Disadvantages

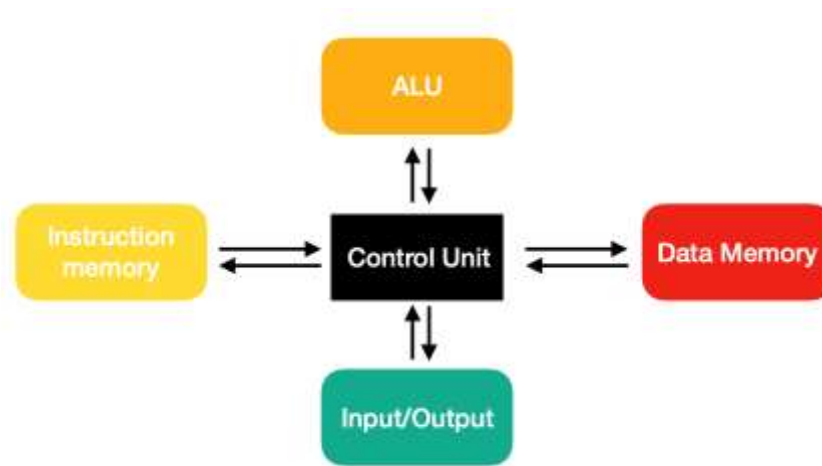
- Parallel executions of programs are not allowed due to serial instruction processing.

- Only one “bus” can be accessed at a time. This results in the CPU being idle (as it’s faster than a data bus) This is considered to be the von Neumann Bottleneck.
- Although both instructions and data being stored in the same place can be viewed as an advantage as a whole. This can however result in re-writing over it, which results in data loss, due to an error in a program.

2.2. Harvard Architecture

Harvard architecture is named after the “Harvard Mark I” relay-based computer, which was an IBM computer in the University of Harvard.

Harvard architecture is a type of architecture, which stores the data and instructions separately, therefore splitting the memory unit.



The CPU in a Harvard architecture system is enabled to fetch data and instructions simultaneously, due to the architecture having separate buses for data transfers and instruction fetches.

2.2.1. Harvard Advantages

- Due to instructions and data being transferred in different buses, this means there is a smaller chance of data corruption.
- Instructions and data can be accessed the same way.
- Harvard architecture offers a high performance, as this architecture allows a simultaneous flow of data and instructions. These are kept in a separate memory and travel via separate buses.
- There is a greater memory bandwidth that is more predictable, due to the architecture having separate memory for instructions and data.

2.2.2. Harvard Disadvantages

- The memory dedicated to each (data and instructions) must be balanced by the manufacturer. Because if there is free memory data memory, it cannot be used for instructions and vice versa.
- However, this advantage (to the left) results in a more complex architecture, as it requires two buses. This means it takes more time to manufacture and it makes these systems more expensive.
- This architecture, however, despite the high performance, is very complex, especially for main board manufacturers to implement.
- Though as mentioned above, to achieve the advantage on the left, Harvard architecture requires a control unit for two buses. Which increases complexity and makes development more difficult. All of which increase the price of the system.

2.3. Facts

- 2.3.1. The von Neumann Architecture was a large advancement from the program-controlled computers, which were used in the 1940's. Such computer were programmed by setting the inserting patch leads and switches to route data and control signals between different functional sets.
- 2.3.2. The CPU in a Harvard architecture system is enabled to fetch data and instructions simultaneously, due to the architecture having separate buses for data transfers and instruction fetches.

3. RISC vs CISC Machines

Both RISC and CISC architectures have been developed largely as a breakthrough to cover the semantic gap. The semantic gap, is the gap that is present between machine language and high-level language.

Therefore the main objective of creating these two architectures is to improve the efficiency of software development, and by doing so, there have been several programming languages that have been developed as a result, such as Ada, C++, C, and Java etc.

3.1. What are RISC processors

Reduced Instruction Set Computer (RISC), is a type of computer architecture that operates on a small, highly optimized set of instructions, instead of a more specialized set of instructions, which can be found in other types of architectures. This architecture means that the computer microprocessor will have fewer cycles per instruction.

A RISC chip doesn't require many transistors, which makes them less costly to design and produce. One of RISCs main characteristics is that the instruction set contains relatively simple and basic instructions from which more complex instructions can be produced.

3.2. What are CISC processors

CISC, which stands for "Complex Instruction Set Computer", is a computer architecture where single instructions can execute several low-level operations, for instance, "load from memory an arithmetic operation, and a memory store). CISC processors are also capable of executing multi-step operations or addressing modes with single instructions.

In CISC processors, every single instruction has several low-level operations. Yes, this makes CISC instructions short, but complex.

3.3. Comparison between RISC and CISC processors

	RISC	CISC
Performance	Average the same.	
	<ul style="list-style-type: none"> - RISC is faster in decoding. - RISC is not supported with complex instructions so there may be more instructions to make the same operation. 	<ul style="list-style-type: none"> - CISC is slower in decoding. - RISC is not supported with complex instructions so there may be more instructions to make the same operation.
Cost	Average the same.	
	<ul style="list-style-type: none"> - RISC compiler is more expensive to handle the simple instructions. 	<ul style="list-style-type: none"> - CISC ALU is more expensive to handle more instructions.

Comparison between RISC and CISC processors

Size	Average the same.	
	<ul style="list-style-type: none">- RISC ALU is smaller because of lower number of instruction set.- Decoder is bigger because it is hardwired decoder.	<ul style="list-style-type: none">- CISC ALU is bigger because of bigger number of instruction set.- Decoder is smaller because it is microprogrammed decoder.
Power Consumption	Average the same. Only one circuit is on at the same time.	

So a reduced Instruction Set Computer (RISC), can be considered as an evolution of the alternative to Complex Instruction Set Computing (CISC). With RISC, in simple terms, its function is to have simple instructions that do less but execute very quickly to provide better performance.

4. AHP and APB Buses

AHB (Advanced High-performance Bus) and APB (Advanced Peripheral Bus) are two bus protocols that are extensively used in the design of complex digital systems.

The key difference between AHB and APB is their speed and intended usage. AHB is designed for high-performance applications requiring fast data transmission rates and low-latency communication, whereas APB is designed for slower peripherals not requiring high-speed data transport.

4.1. AHB Interface

AHB is an ARM-designed high-performance bus protocol for connecting high-speed peripherals and memory in a system-on-a-chip (SoC) design. The AHB is a pipelined bus with separate address and data phases that allows high-speed data transmission between peripherals.

4.2. APB Interface

APB (Advanced Peripheral Bus) is an ARM-designed low-power, low-cost bus protocol for connecting low-speed peripherals in a system-on-a-chip (SoC) design. The APB is a simple bus with a single clock edge protocol, making it simple to implement and lowering total system complexity.

4.3. Comparison between AHB and APB interfaces

Characteristics	AHB	APB
Speed	High	High
Clock Rate	100 MHz to 1 GHz	100 MHz to 1 GHz
Latency	AHB latency is low.	AHB latency is low.
Transfer Size	The AHB transfer size is up to 16 beats.	The AHB transfer size is up to 16 beats.
Modes of Transfer	single, incremental, and fixed burst	single, incremental, and fixed burst
Power Consumption	High	High
Number of Pins	Many	Many
Complexity of Signal	AHB has a complex signal interface.	AHB has a complex signal interface.

5. References

- 5.1. [https://eng.libretexts.org/Bookshelves/Electrical_Engineering/Electronics/Implementing_a_One_Address_CPU_in_Logisim_\(Kann\)/01%3A_Introduction/1.03%3A_Von_Neumann_and_Harvard_Architectures](https://eng.libretexts.org/Bookshelves/Electrical_Engineering/Electronics/Implementing_a_One_Address_CPU_in_Logisim_(Kann)/01%3A_Introduction/1.03%3A_Von_Neumann_and_Harvard_Architectures)
- 5.2. <https://teachcomputerscience.com/von-neumann-harvard-architecture/>
- 5.3. <https://teachcomputerscience.com/risc-and-cisc-processors/>
- 5.4. <https://www.tutorialspoint.com/difference-between-ahb-and-apb>