

University of Engineering and Technology,Taxila

Department of Computer Engineering



Assignment

For the Course of DSD

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Section: Omega

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Course Instructor:Dr.Abdul rehman aslam

Date: 05-02-24.

Course Title: DSD

Questions/Answer

1. Design the following basic gates using 2-to-1 multiplexers only. (40 Marks)

a. Inverter

Truth table:

21-CP-26 M. Ibrahim

Q No 1
Design following basic gates 2x1
MUX only?
a) Inverter.

Truth table:- Not gate

A	OUT	Inverted	$S=0$ $OUT=1$
0	1	0	$S=1$ $OUT=0$

Truth table 2x1

S	A	B	Out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Circuit diagram :

Truth table :- Not gate

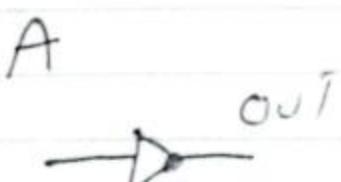
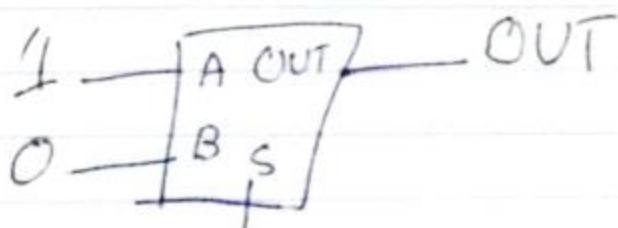
A OUT
0 1
1 0

Inverted

$$\begin{array}{l} S=0 \\ OUT=1 \end{array}$$

NOT Gate

$A = \text{Select}$



Truth table 2x1

S	A	B	out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Code:

ISF Project Navigator (P.28xd) - G:\semster 6\DSD LAB\ASSIGNMENTS\A01_21 CP_26\A01_21 CP_26.xise - [A01_21CP26_Q1Av1]

The screenshot shows a software interface for Verilog simulation. The top menu bar includes File, Edit, View, Project, Source, Process, Tools, Window, Layout, and Help. Below the menu is a toolbar with various icons for file operations like Open, Save, and Run. A left sidebar titled 'Files' lists multiple Verilog files under a 'Simulation' category, each named 'A01...' and ending with 'Veri... All'. The main window displays the Verilog source code for a module named 'A01_21CP26_Q1A'. The code defines a module with inputs Y, D0, D1, and S, and outputs Y. It uses an assign statement to set Y based on S. Inside the module, there is a 'mux' block with its own parameters and connections to the module's inputs.

```
20 //////////////////////////////////////////////////////////////////
21 module mux(Y,D0,D1,S);
22   output wire Y;
23   input wire D0;
24   input wire D1;
25   input wire S;
26   assign Y=(S==0)?D0:D1;
27 endmodule
28
29 module A01_21CP26_Q1A(Y,A);
30   input wire A;
31   output wire Y;
32   wire D0=1'b0;
33   wire D1=1'b1;
34   wire S;
35   |
36   assign S=A^1'b1;
37
38 mux m1(
39   .Y(Y),
40   .D0(D0),
41   .D1(D1),
42   .S(S));
43 endmodule
44
```

```
'timescale 1ns / 1ps
```

// Company:

```

// Engineer:
//
// Create Date: 13:43:56 01/27/2024
// Design Name:
// Module Name: A01_21CP26_Q1A
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
///////////////////////////////
module mux(Y,D0,D1,S);
output wire Y;
input wire D0;
input wire D1;
input wire S;
assign Y=(S==0)?D0:D1;
endmodule

module A01_21CP26_Q1A(Y,A);
input wire A;
output wire Y;
wire D0=1'b0;
wire D1=1'b1;
wire S;

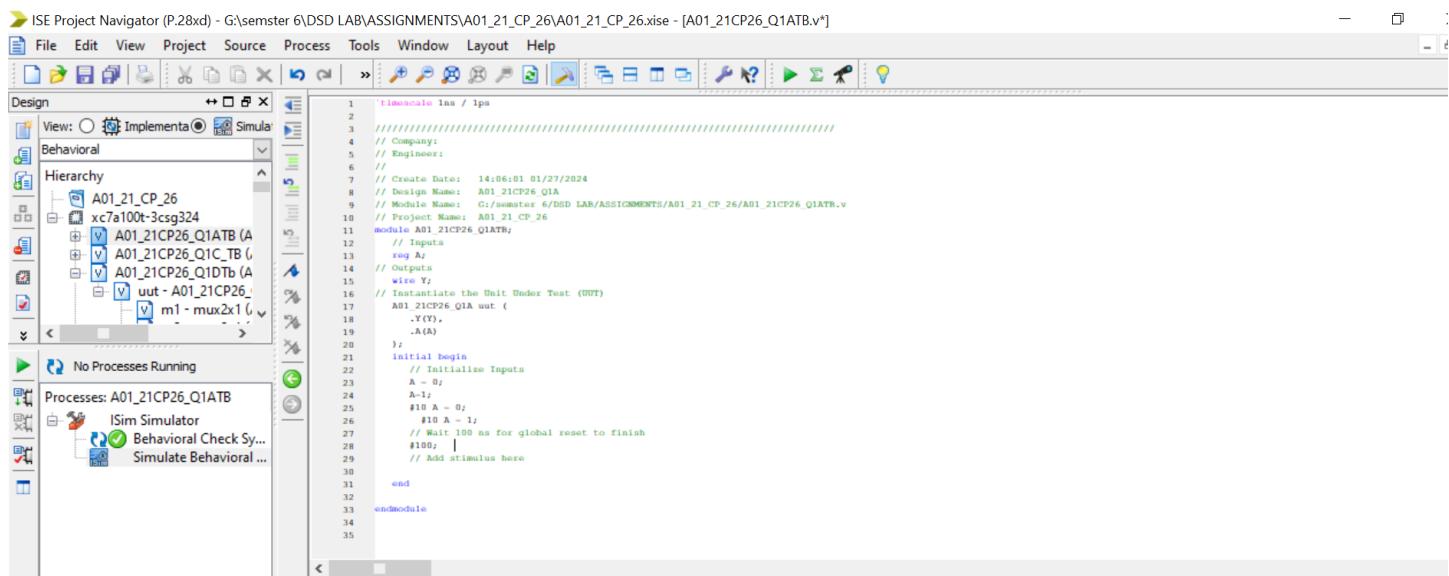
assign S=A^1'b1;

mux m1(
.Y(Y),
.D0(D0),
.D1(D1),
.S(S));

```

endmodule

TestBench:



`timescale 1ns / 1ps

|||||

// Company:

// Engineer:

11

// Create Date: 14:06:01 01/27/2024

// Design Name: A01_21CP26_Q1A

// Module Name: G:/semster 6/DSD LAB/ASSIGNMENTS/A01_21_CP_26/A01_21CP26_Q1ATB.v

// Project Name: A01_21_CP_26

```
module A01_21CP26_Q1ATB;
```

// Inputs

S

wire Y;

Create the Unit Under Test

'26_Q1

.Y(Y),

);

in

// Init

$$A = 0$$

A=1;

#10 A = 0;

```

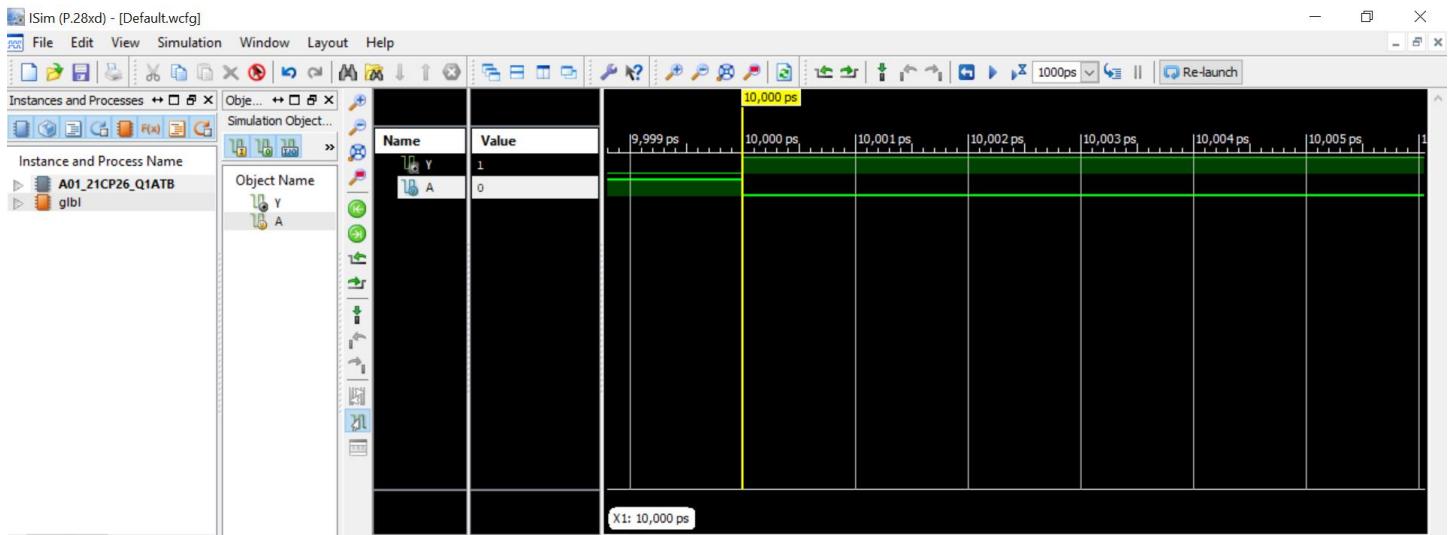
#10 A = 1;
// Wait 100 ns for global reset to finish
#100;
// Add stimulus here

end

endmodule

```

Simulation:

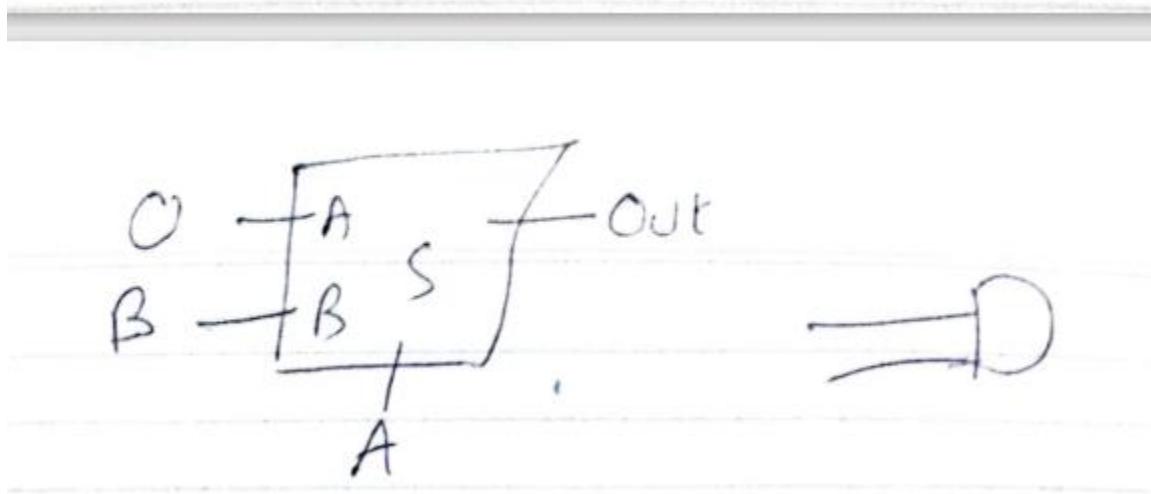


b. 2-input and gate

Truth table:

Truth table And gate			
A	B	Out	
0	0	0	Out = 0
0	1	0	when A = 0
1	0	0	Out = B
1	1	1	when A = 1

Circuit diagram :



Code:

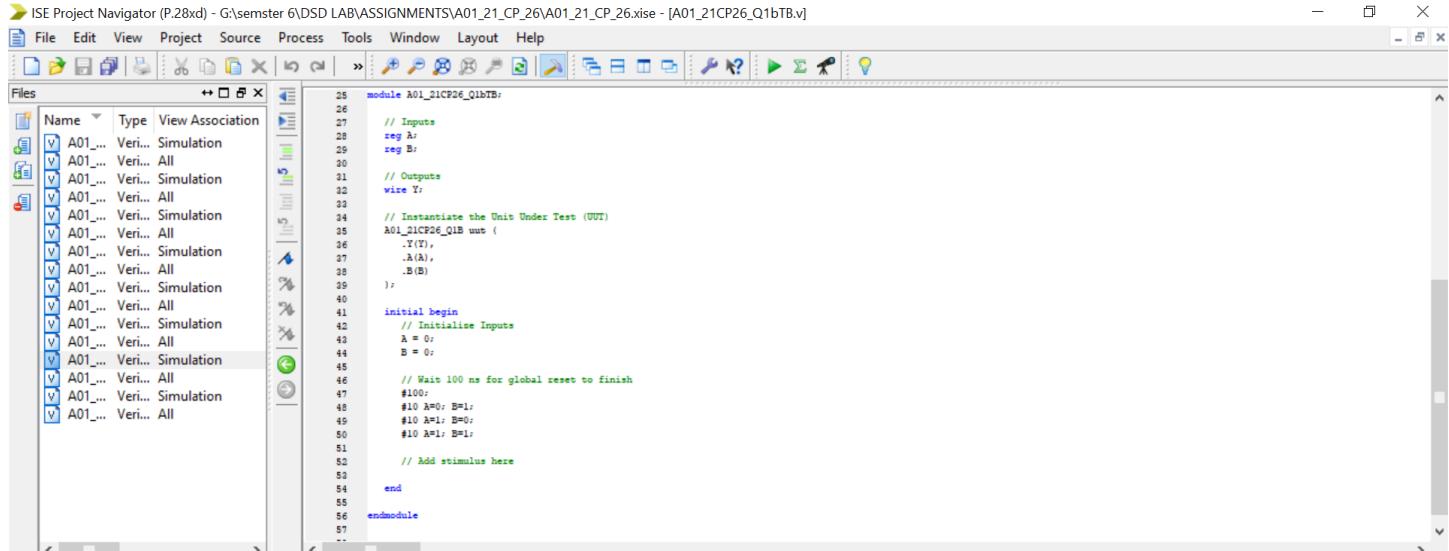
The screenshot shows the ISE Project Navigator interface. The code editor displays the following Verilog HDL code for a MUX module:

```
13 // Dependencies:
14 // Revision:
15 // Revision 0.01 - File Created
16 // Additional Comments:
17 ///////////////////////////////////////////////////////////////////
18 module A01_21CP26_Q1B(Y,A,B
19 );
20   input wire A,B;
21   output wire Y;
22   wire D0=1'b0;
23   wire D1=B;
24
25   mux m2(
26     .Y(Y),
27     .D0(D0),
28     .D1(D1),
29     .S(A)
30   );
31   endmodule
32
33
34
35
36
37
```

```
'timescale 1ns / 1ps
/////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 14:22:04 01/27/2024
// Design Name:
// Module Name: A01_21CP26_Q1B
// Project Name:
// Target Devices:
// Tool versions:
// Description:
```

```
//  
// Dependencies:  
//  
// Revision:  
// Revision 0.01 - File Created  
// Additional Comments:  
//  
////////////////////////////////////////////////////////////////  
module A01_21CP26_Q1B(Y,A,B  
);  
input wire A,B;  
output wire Y;  
wire D0=1'b0;  
wire D1=B;  
  
mux m2(  
    .Y(Y),  
    .D0(D0),  
    .D1(D1),  
    .S(A)  
);  
endmodule
```

TestBench:



`timescale 1ns / 1ps

// Company:

```
// Engineer:  
//  
// Create Date: 14:27:45 01/27/2024  
// Design Name: A01_21CP26_Q1B  
// Module Name: G:/semster 6/DSD LAB/ASSIGNMENTS/A01_21_CP_26/A01_21CP26_Q1bTB.v  
// Project Name: A01_21_CP_26  
// Target Device:  
// Tool versions:  
// Description:  
//  
// Verilog Test Fixture created by ISE for module: A01_21CP26_Q1B  
//  
// Dependencies:  
//  
// Revision:  
// Revision 0.01 - File Created  
// Additional Comments:  
//  
||||||||||||||||||||||||||||||||||||||||||||||||||||||||
```

```
module A01_21CP26_Q1bTB;
```

```
    // Inputs  
    reg A;  
    reg B;  
  
    // Outputs  
    wire Y;  
  
    // Instantiate the Unit Under Test (UUT)  
    A01_21CP26_Q1B uut (  
        .Y(Y),  
        .A(A),  
        .B(B)  
    );
```

```
initial begin  
    // Initialize Inputs  
    A = 0;
```

```

B = 0;

// Wait 100 ns for global reset to finish

#100;

#10 A=0; B=1;
#10 A=1; B=0;
#10 A=1; B=1;

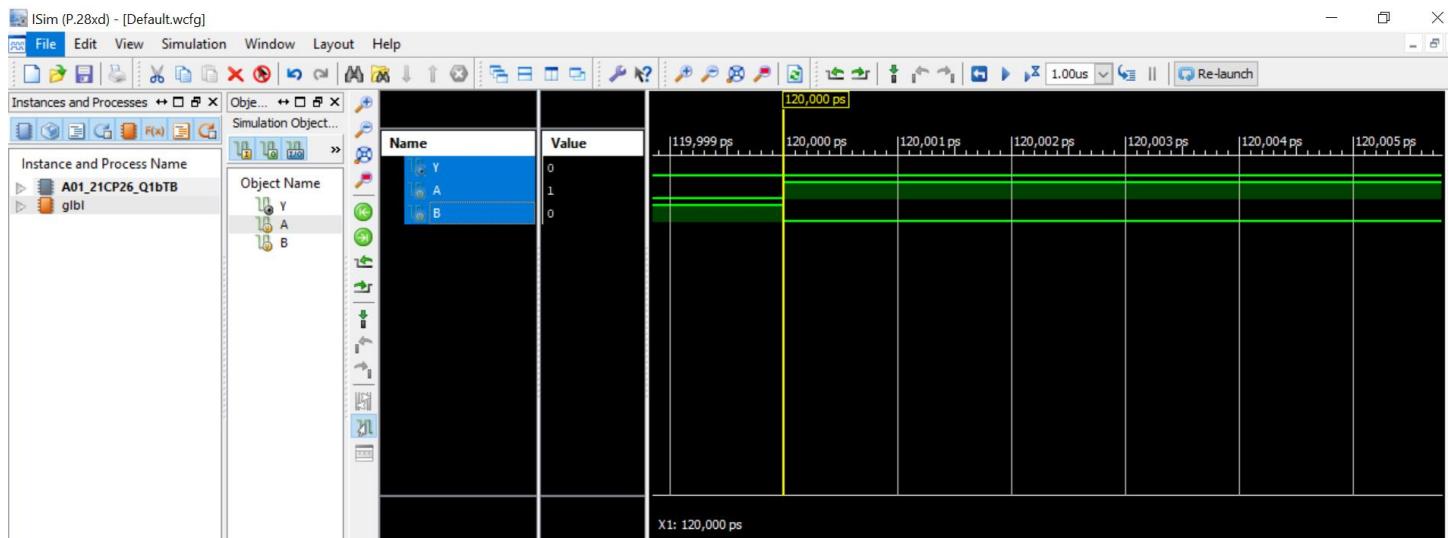
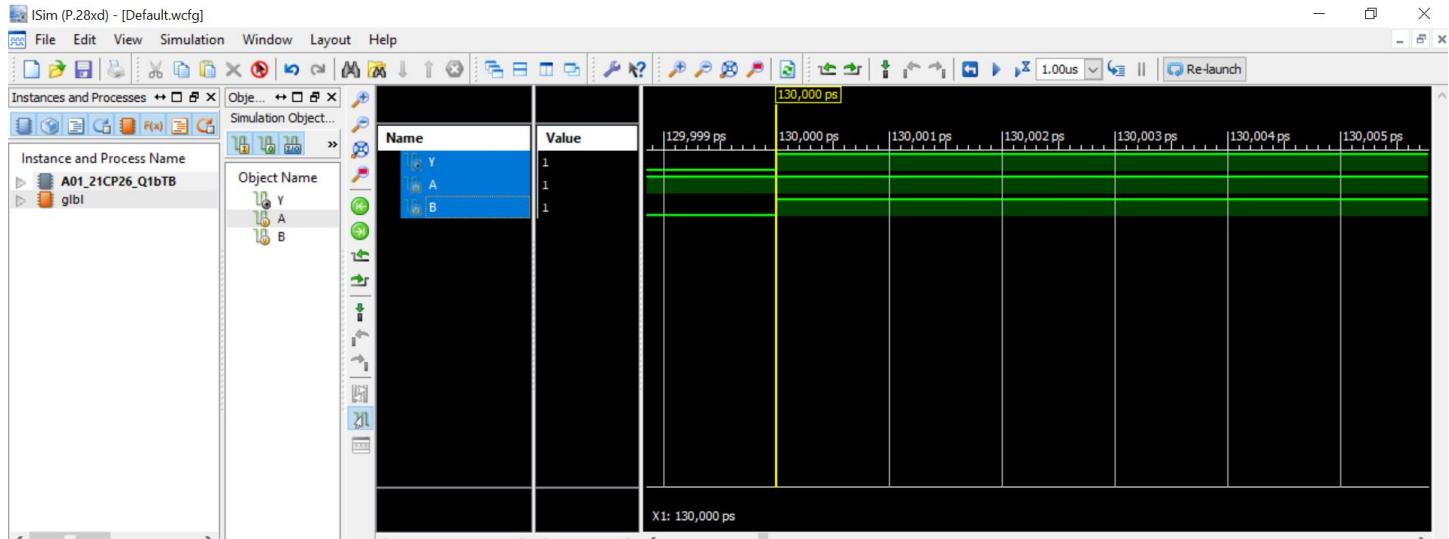
// Add stimulus here

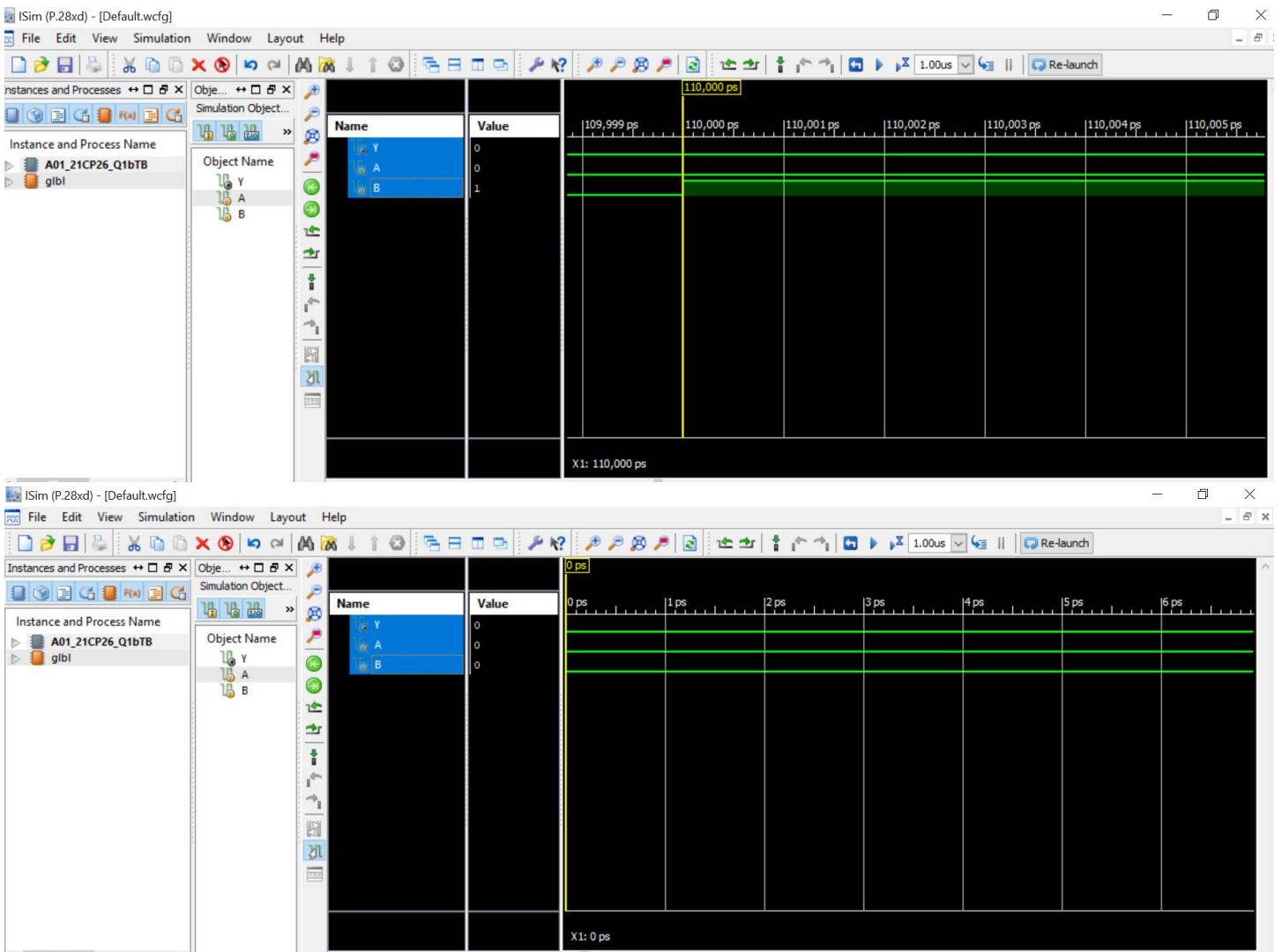
end

endmodule

```

Simulation:





c. 2-input or gate

Truth table:

Truth table

A	B	OUT	
0	0	0	$OUT = B$
0	1	1	when $A = 0$
1	0	1	$OUT = 1$
1	1	1	when $A = 1$

Circuit diagram :

2-input OR gate

Truth table

A	B	OUT
---	---	-----

0	0	0
---	---	---

0	1	1
---	---	---

1	0	1
---	---	---

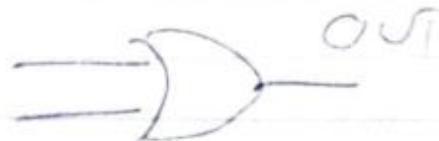
1	1	1
---	---	---

OUT = B

when A = 0

OUT = 1

when A = 1



Code:

```
11 // Tool versions:  
12 // Description:  
13 //  
14 // Dependencies:  
15 //  
16 // Revision:  
17 // Revision 0.01 - File Created  
18 // Additional Comments:  
19 //  
20 ///////////////////////////////////////////////////////////////////  
21 module A01_21CP26_Q1C(Y,A,B);  
22     input wire A,B;  
23     output wire Y;  
24     wire D0=B;  
25     wire D1=1;  
26  
27     mux m3(  
28         .Y(Y),  
29         .D0(D0),  
30         .D1(D1),  
31         .S(A)  
32     );  
33 endmodule  
34
```

'timescale 1ns / 1ps

//

// Company:

// Engineer:

//

// Create Date: 14:33:45 01/27/2024

// Design Name:

// Module Name: A01_21CP26_Q1C

// Project Name:

// Target Devices:

// Tool versions:

// Description:

11

11

11

11

11 Revision 6

11

.....

Module A01_Z1CP26_Q1C(Y,A,B);

Input wire A,B;

output wire Y;

wire D0=B;

wire D1=1;

mux m3(

$\cdot Y(Y),$

.D0(D0),

.D1(D1),

.S(A)

);

endmodule

TestBench:

ISE Project Navigator (P.28xd) - G:\semster 6\DS^D LAB\ASSIGNMENTS\A01_21_CP_26\A01_21_CP_26.xise - [A01_21CP26_Q1C_TB.v]

```

25 module A01_21CP26_Q1C_TB;
26
27 reg A, B;
28 wire Y;
29
30 // Instantiate the Unit Under Test (UUT)
31 A01_21CP26_Q1C uut (
32   .A(A),
33   .B(B),
34   .Y(Y)
35 );
36
37 initial begin
38
39   A = 0;
40   B = 0;
41   #10;
42
43   A = 0;
44   B = 1;
45   #10;
46
47   A = 1;
48   B = 0;
49   #10;
50   A = 1;
51   B = 1;
52   #10;
53
54 end
55
56 endmodule
57

```

'timescale 1ns / 1ps

//////////

// Company:

// Engineer:

//

// Create Date: 14:38:03 01/27/2024

// Design Name: A01_21CP26_Q1C

// Module Name: G:/semster 6/DS^D LAB/ASSIGNMENTS/A01_21_CP_26/A01_21CP26_Q1C_TB.v

// Project Name: A01_21_CP_26

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: A01_21CP26_Q1C

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////

module A01_21CP26_Q1C_TB;

```

reg A, B;
wire Y;

// Instantiate the Unit Under Test (UUT)
A01_21CP26_Q1C uut (
    .A(A),
    .B(B),
    .Y(Y)
);

initial begin

    A = 0;
    B = 0;
    #10;

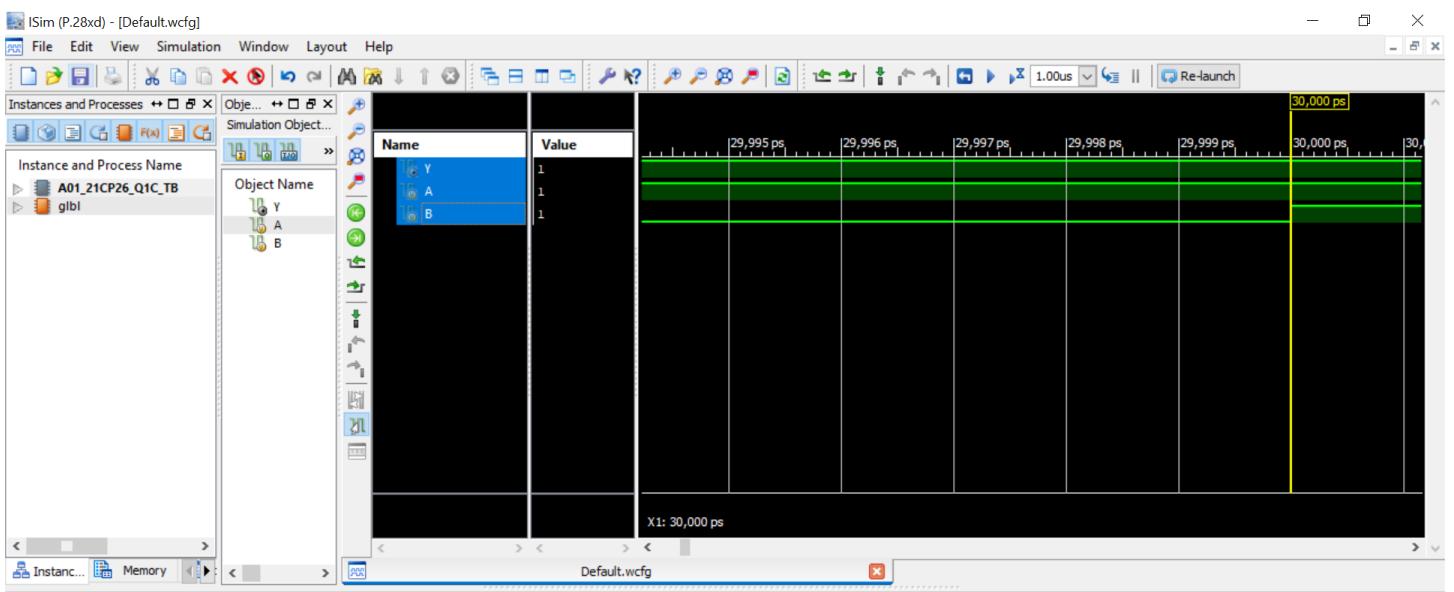
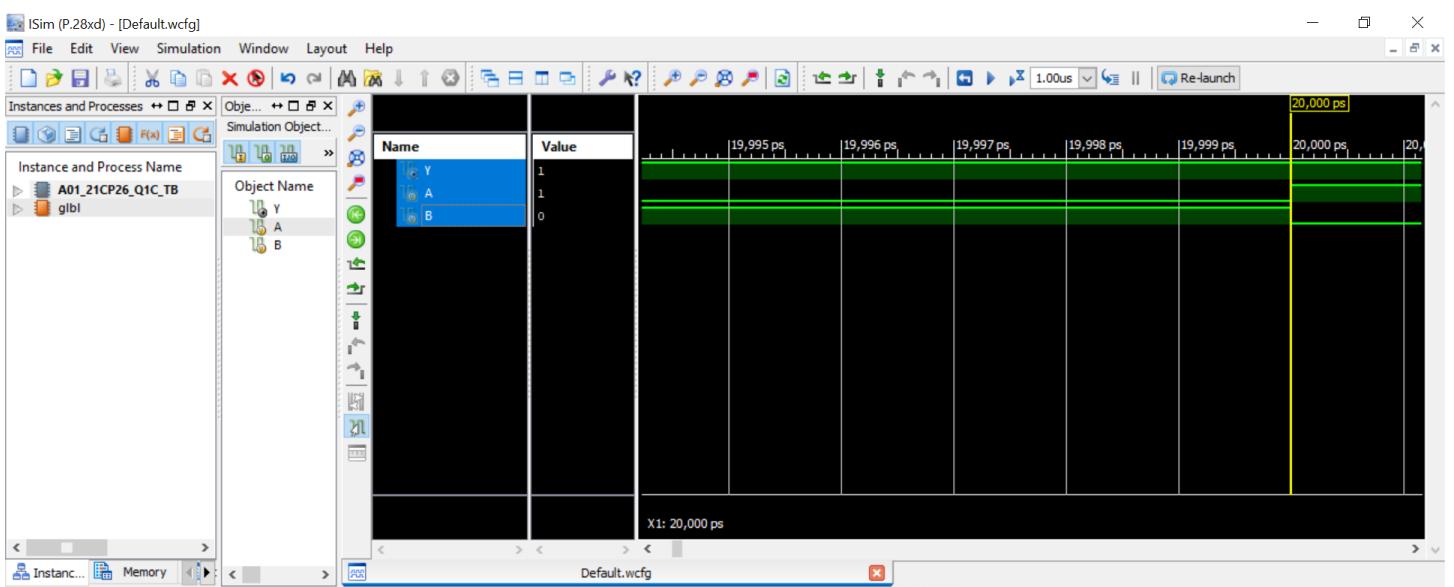
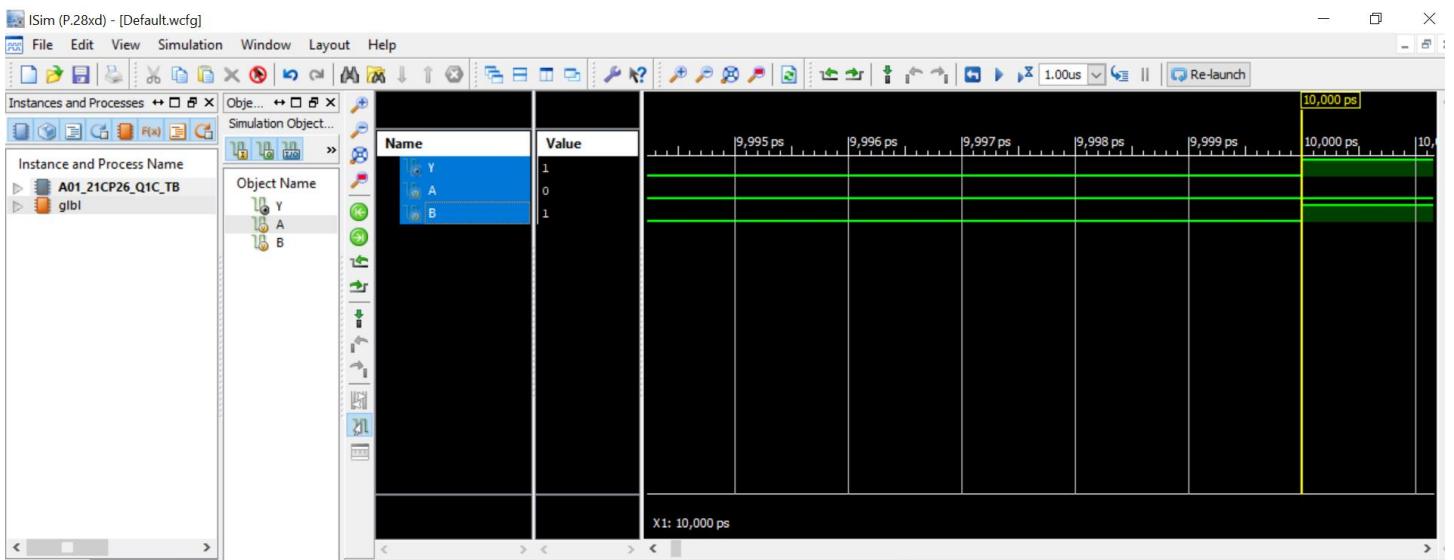
    A = 0;
    B = 1;
    #10;

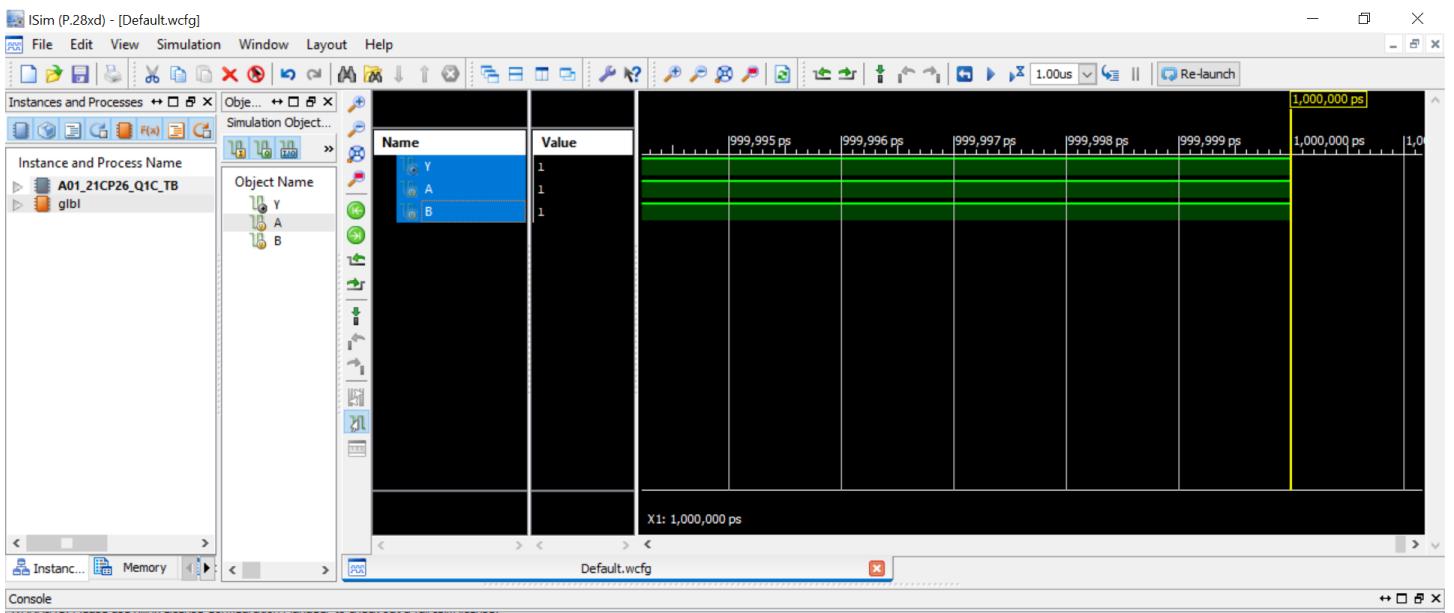
    A = 1;
    B = 0;
    #10;
    A = 1;
    B = 1;
    #10;
end

endmodule

```

Simulation:





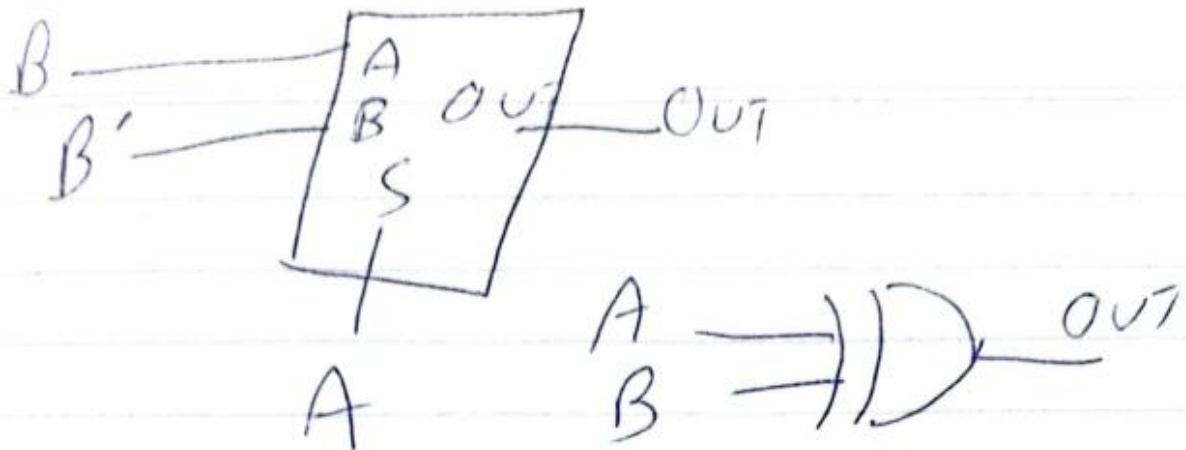
d. 2-input xor gate

Truth table:

2 -input xor gate

A	B	OUT		OUT = B
0	0	0]	when $A=0$
0	1	1]	$OUT = B'$
1	0	1]	when $A=1$

Circuit diagram :



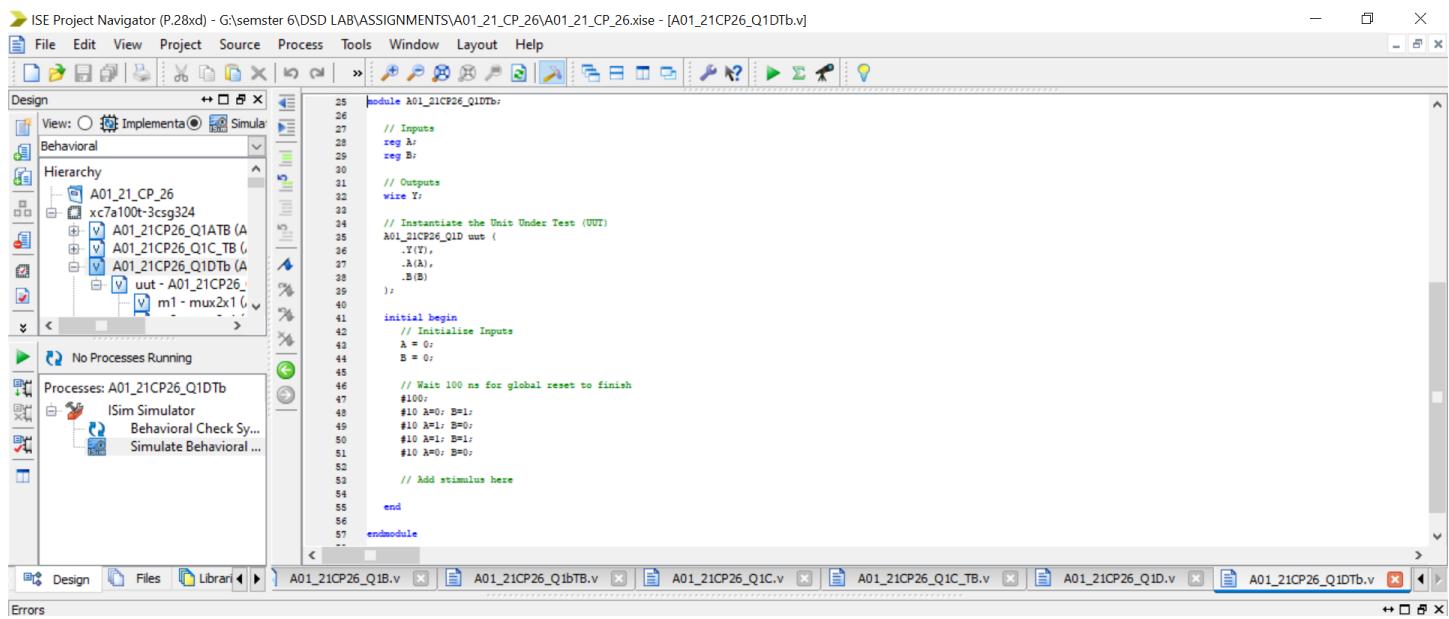
Code:

```
`timescale 1ns / 1ps

//////////////////////////////  
// Company:  
// Engineer:  
//  
// Create Date: 00:20:38 02/03/2024  
// Design Name:  
// Module Name: A01_21CP26_Q1D  
// Project Name:  
// Target Devices:  
// Tool versions:  
// Description:
```

```
//  
// Dependencies:  
//  
// Revision:  
// Revision 0.01 - File Created  
// Additional Comments:  
//  
////////////////////////////////////////////////////////////////  
module A01_21CP26_Q1D(output Y,input A,B  
);  
  
assign q=1;  
assign w=0;  
wire w1;  
mux2x1 m1(.Y(w1), .A(q),.B(w),.S(B));  
  
mux2x1 m2(.Y(Y), .A(B),.B(w1),.S(A));  
  
endmodule  
  
module mux2x1(  
output Y,input A,B,S);  
  
assign Y=(S==0)?A:B;  
  
endmodule
```

TestBench:



```
'timescale 1ns / 1ps
```

|||||

// Company:

// Engineer:

11

// Create Date: 00:26:00 02/03/2024

// Design Name: A01_21CP26_Q1D

// Module Name: G:/semster 6/DSD

// Project Name: A01 21 CP 26

// Target Device:

// Tool versions:

// Description:

11

11

“*It’s a good day to be alive.*”

11

// Revision.

// Revision 0.01 - File Created

// Additional Comments:

11

|||||

module A01_21CP26_Q1DTb;

```

// Inputs
reg A;
reg B;

// Outputs
wire Y;

// Instantiate the Unit Under Test (UUT)
A01_21CP26_Q1D uut (
    .Y(Y),
    .A(A),
    .B(B)
);

initial begin
    // Initialize Inputs
    A = 0;
    B = 0;

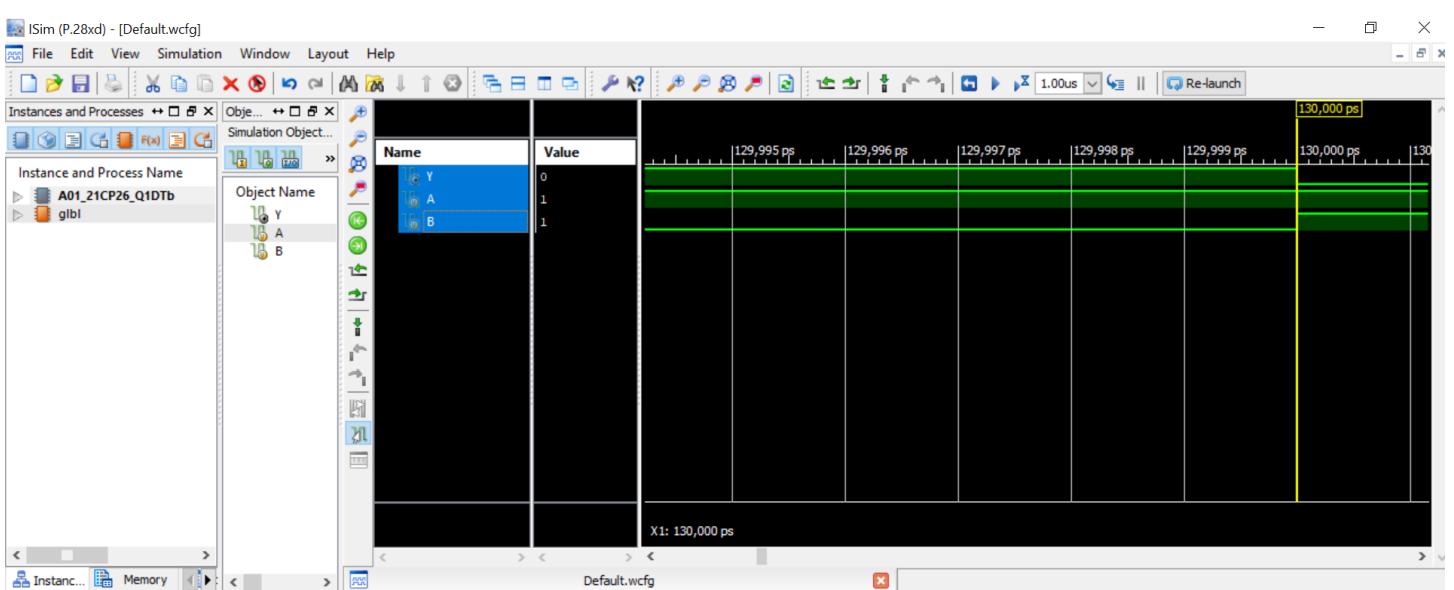
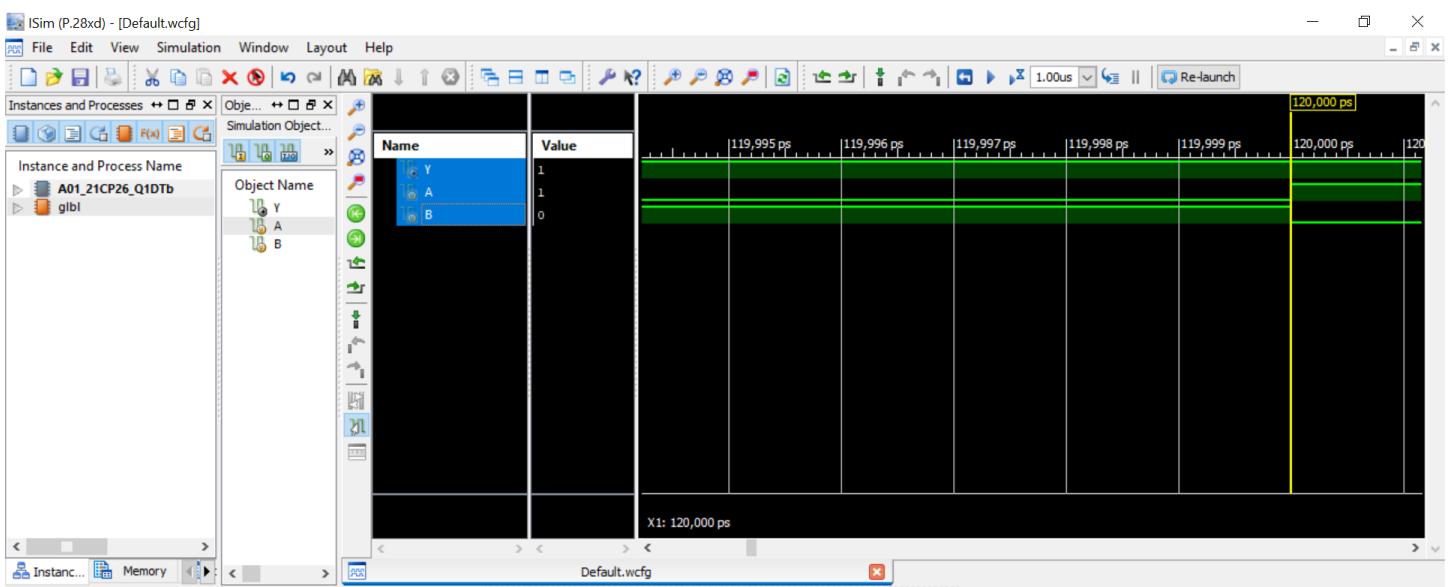
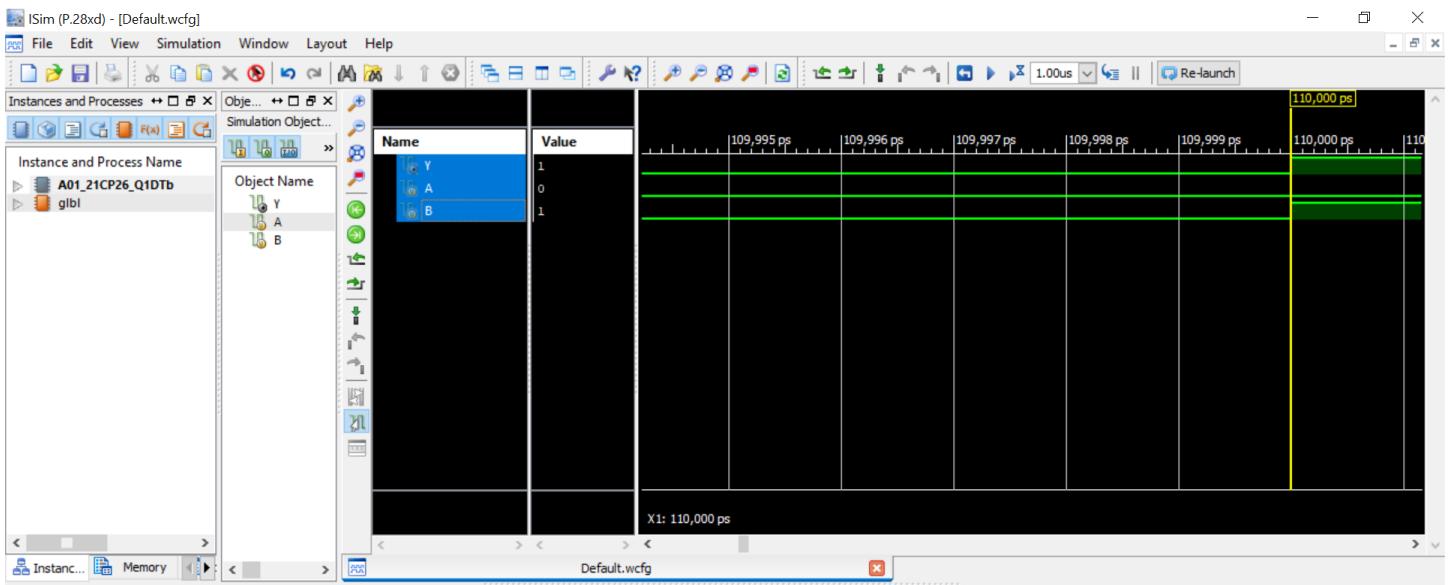
    // Wait 100 ns for global reset to finish
    #100;
    #10 A=0; B=1;
    #10 A=1; B=0;
    #10 A=1; B=1;
    #10 A=0; B=0;

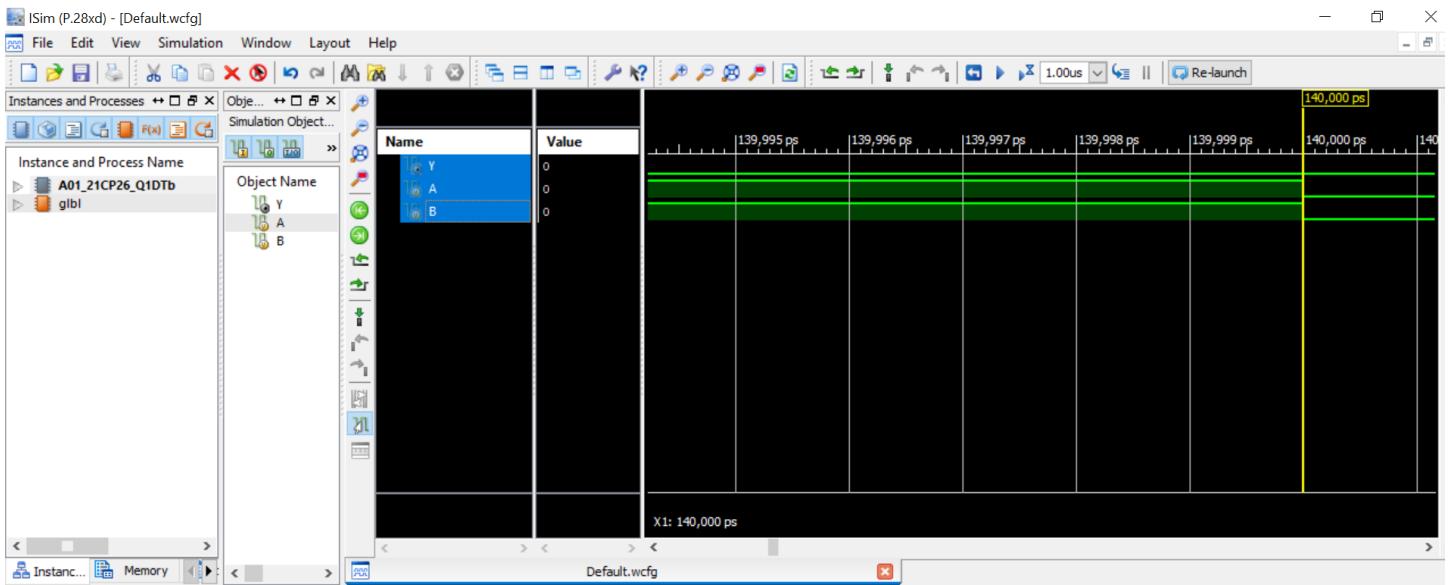
    // Add stimulus here
end

endmodule

```

Simulation:





e. 2-input xnor gate

Truth table:

2 - input XNOR

A	B	OUT	
0	0	1	{
0	1	0	{
1	0	0	{
1	1	1	}

OUT = \bar{B}'
when $\bar{A} = \bar{C}$

OUT = B
when $A = 1$

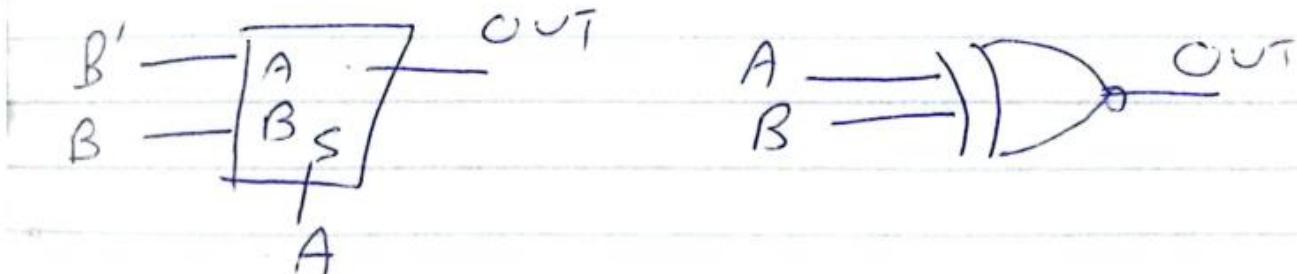
Circuit diagram :

2 - input XNOR

A	B	OUT	
0	0	1	{
0	1	0	}
1	0	0	{
1	1	1	}

OUT = \bar{B}'
when $\bar{A} = 0$

OUT = B
when $\bar{A} = 1$



Code:

`timescale 1ns / 1ps

// Company:

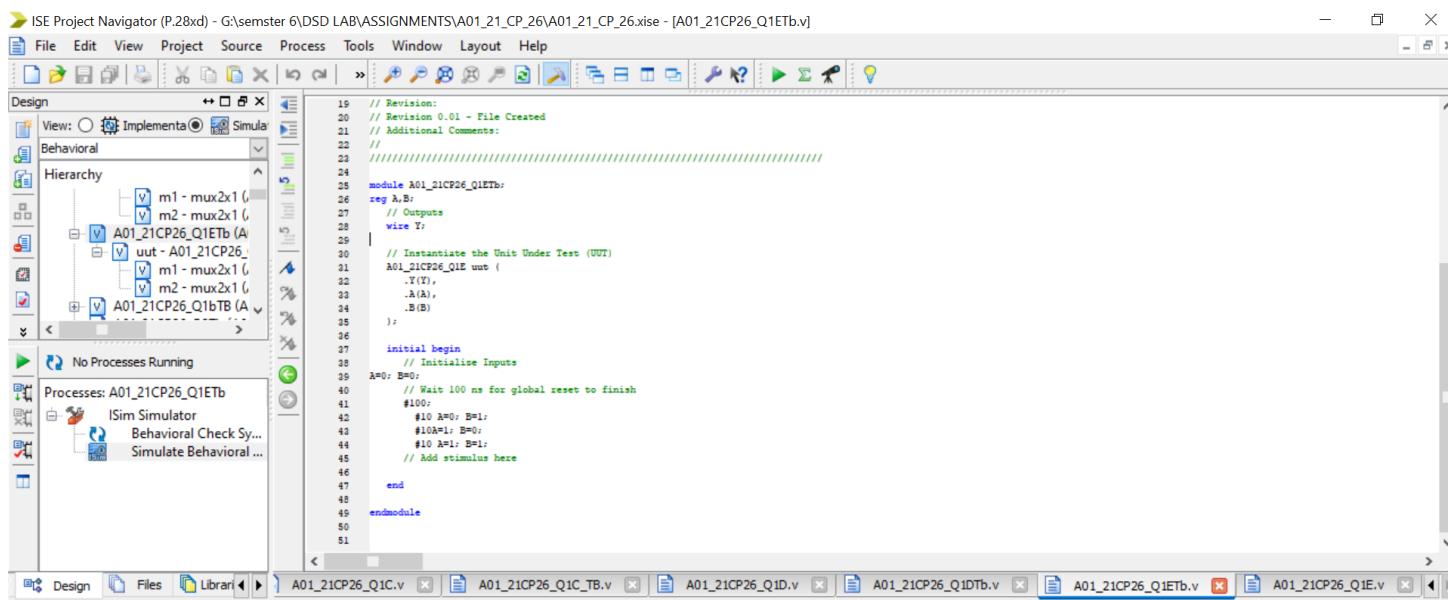
// Engineer:

11

// Create Date: 00:32:26 02/03/2024

```
// Design Name:  
// Module Name: A01_21CP26_Q1E  
// Project Name:  
// Target Devices:  
// Tool versions:  
// Description:  
//  
// Dependencies:  
//  
// Revision:  
// Revision 0.01 - File Created  
// Additional Comments:  
//  
//////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////  
module A01_21CP26_Q1E(output Y,input A,B);  
  
assign q=1;  
assign w=0;  
wire w1;  
mux2x1 m1(.Y(w1), .A(q),.B(w),.S(B));  
  
mux2x1 m2(.Y(Y), .A(w1),.B(B),.S(A));  
  
endmodule  
  
module mux2x1(  
output Y,input A,B,S);  
  
assign Y=(S==0)?A:B;  
  
endmodule
```

TestBench:



`timescale 1ns / 1ps

// Company:

// Engineer:

11

// Create Date: 00:34:13 02/03/2024

// Design Name: A01_21CP26_Q1E

// Module Name: G:/semster 6/DSD LAB/ASSIGNMENTS/A01_21_CP_26/A01_21CP26_Q1ETb.v

// Project Name: A01_21_CP_26

// Target Device:

// Tool versions:

// Description:

11

// Verilog Test Fixture created by ISE for module: A01_21CP26_Q1E

11

// Dependencies:

11

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

11

```
module A01_21CP26_Q1ETb;  
  
reg A,B;
```

```

// Outputs
wire Y;

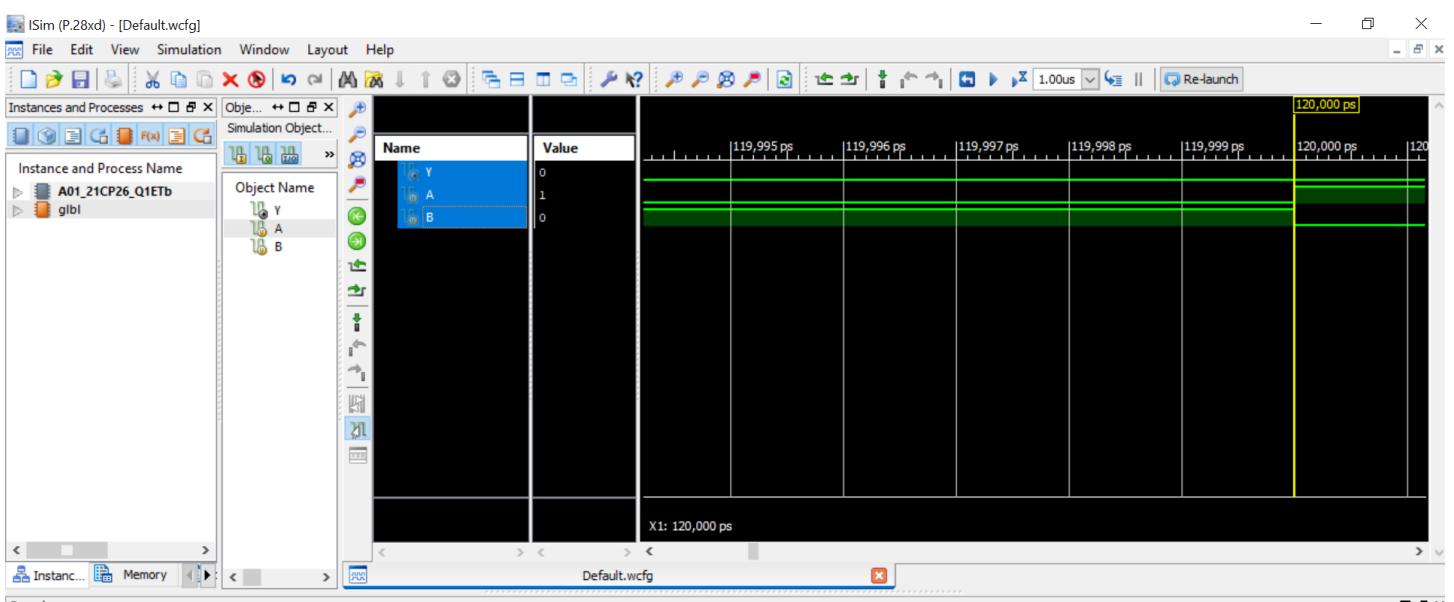
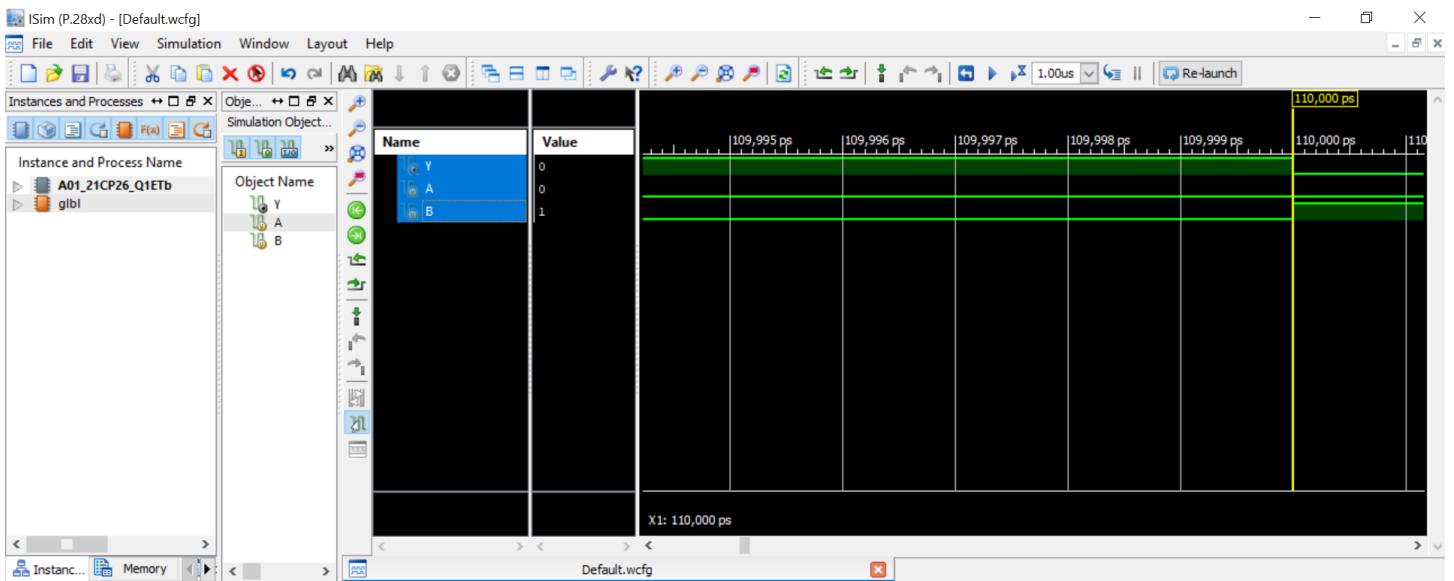
// Instantiate the Unit Under Test (UUT)
A01_21CP26_Q1E uut (
    .Y(Y),
    .A(A),
    .B(B)
);

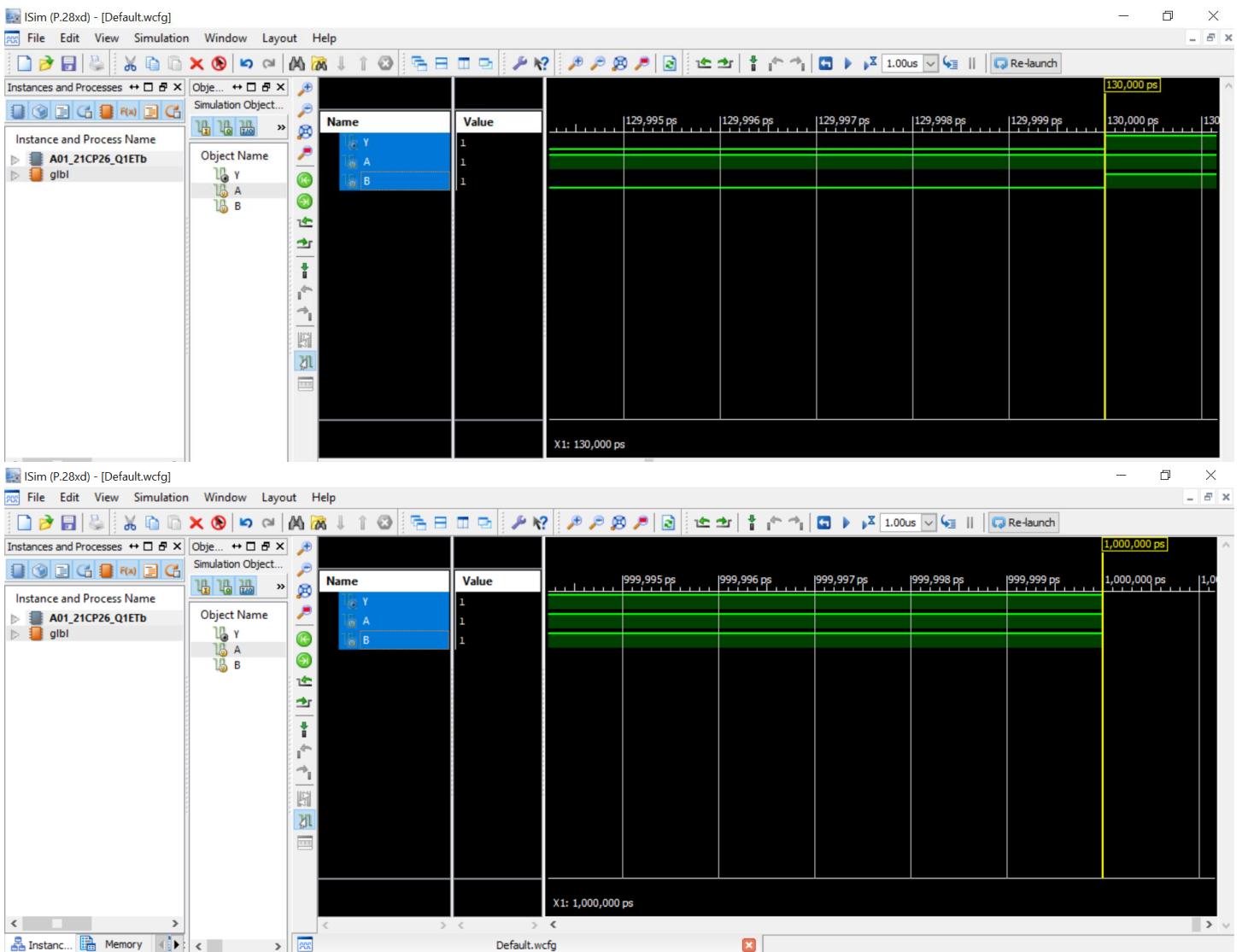
initial begin
    // Initialize Inputs
    A=0; B=0;
    // Wait 100 ns for global reset to finish
    #100;
    #10 A=0; B=1;
    #10A=1; B=0;
    #10 A=1; B=1;
    // Add stimulus here
end

endmodule

```

Simulation:





2. Design a 16-to-1 Multiplexer using 2-to-1 Multiplexer only. (20 Marks)

Truth table:

	Inputs				Outputs
	S_0	S_1	S_2	S_3	Y
1	0	0	0	0	A_0
2	0	0	0	1	A_1
3	0	0	1	0	A_2
4	0	0	1	1	A_3
5	0	1	0	0	A_4
6	0	1	0	1	A_5
7	0	1	1	0	A_6
8	0	1	1	1	A_7
9	1	0	0	0	A_8
10	1	0	0	1	A_9
11	1	0	1	0	A_{10}
12	1	0	1	1	A_{11}
13	1	1	0	0	A_{12}
14	1	1	0	1	A_{13}
15	1	1	1	0	A_{14}
16	1	1	1	1	A_{15}

Circuit diagram :

$$Y = A_0 \bar{S}_0 \bar{S}_1 \bar{S}_2 \bar{S}_3 + A_1 \bar{S}_0 \bar{S}_1 \bar{S}_2 S_3$$

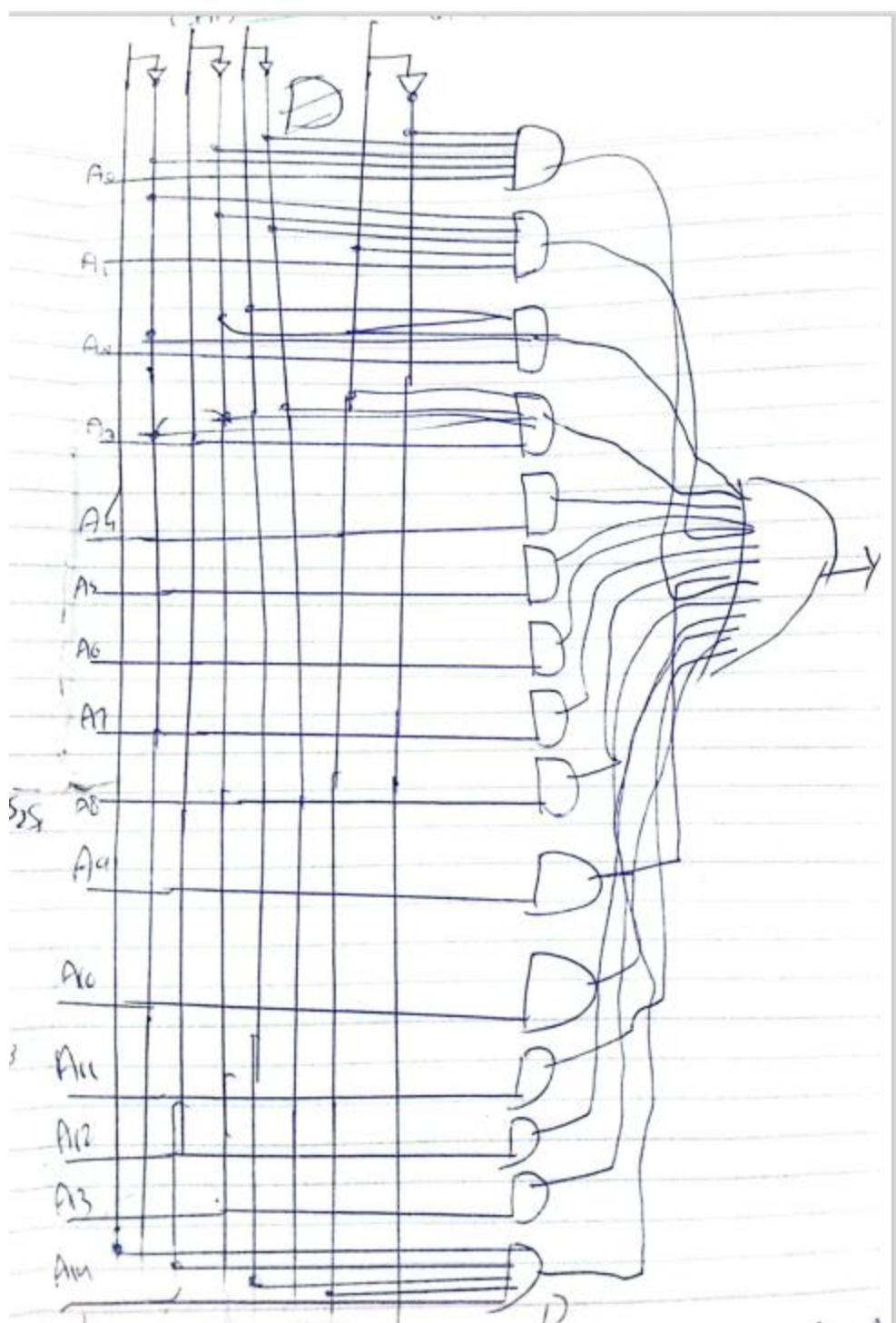
$$+ A_2 \bar{S}_0 \bar{S}_1 S_2 \bar{S}_3 + A_3 \bar{S}_0 \bar{S}_1 S_2 \bar{S}_3 + A_4 \bar{S}_0 S_1 \bar{S}_2 \bar{S}_3$$

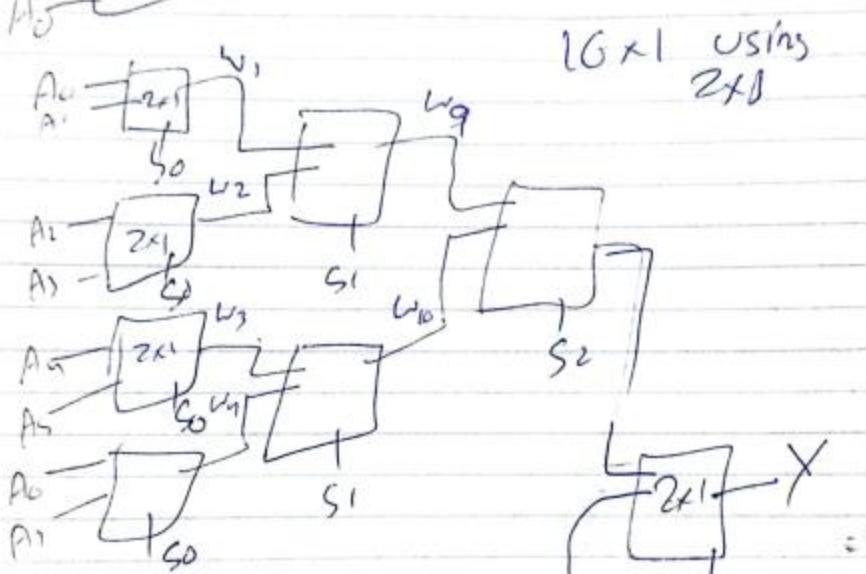
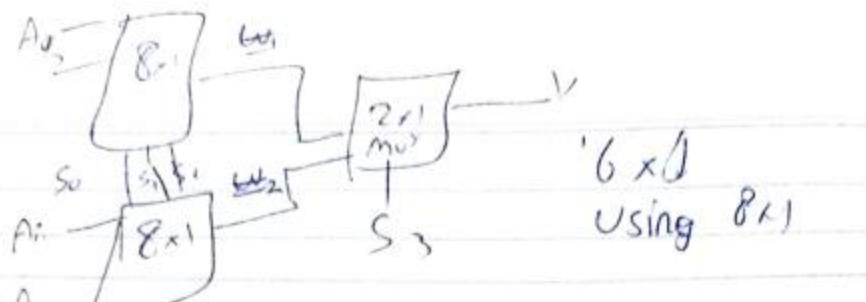
$$+ A_5 \bar{S}_0 S_1 \bar{S}_2 S_3 + A_6 \bar{S}_0 S_1 S_2 \bar{S}_3 + A_7 \bar{S}_0 S_1 S_2 S_3$$

~~$$+ A_8 \bar{S}_0 \bar{S}_1 \bar{S}_2 \bar{S}_3 + A_9 \bar{S}_0 \bar{S}_1 S_2 \bar{S}_3 + A_{10} \bar{S}_0 S_1 \bar{S}_2 \bar{S}_3$$~~

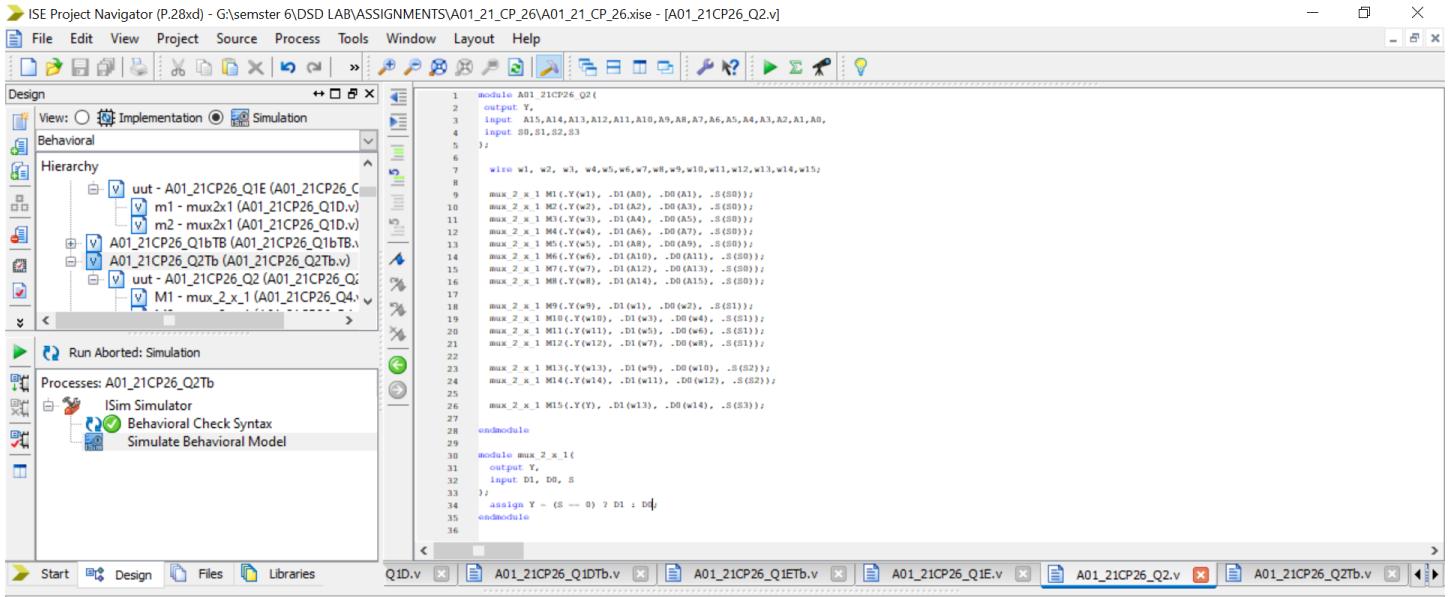
$$+ A_{11} \bar{S}_0 \bar{S}_1 S_2 S_3 + A_{12} \bar{S}_0 S_1 \bar{S}_2 \bar{S}_3 + A_{13} \bar{S}_0 S_1 \bar{S}_2 S_3$$

$$+ A_{14} \bar{S}_0 S_1 S_2 S_3 + A_{15} \bar{S}_0 S_1 S_2 S_3$$





Code:



```
module A01_21CP26_Q2(
    output Y,
    input A15,A14,A13,A12,A11,A10,A9,A8,A7,A6,A5,A4,A3,A2,A1,A0,
    input S0,S1,S2,S3
);
```

```
wire w1, w2, w3, w4,w5,w6,w7,w8,w9,w10,w11,w12,w13,w14,w15;
```

```
mux_2_x_1 M1(.Y(w1), .D1(A0), .D0(A1), .S(S0));
```

```
mux_2_x_1 M2(.Y(w2), .D1(A2), .D0(A3), .S(S0));
```

```
mux_2_x_1 M3(.Y(w3), .D1(A4), .D0(A5), .S(S0));
```

```
mux_2_x_1 M4(.Y(w4), .D1(A6), .D0(A7), .S(S0));
```

```
mux_2_x_1 M5(.Y(w5), .D1(A8), .D0(A9), .S(S0));
```

```
mux_2_x_1 M6(.Y(w6), .D1(A10), .D0(A11), .S(S0));
```

```
mux_2_x_1 M7(.Y(w7), .D1(A12), .D0(A13), .S(S0));
```

```
mux_2_x_1 M8(.Y(w8), .D1(A14), .D0(A15), .S(S0));
```

```
mux_2_x_1 M9(.Y(w9), .D1(w1), .D0(w2), .S(S1));
```

```
mux_2_x_1 M10(.Y(w10), .D1(w3), .D0(w4), .S(S1));
```

```
mux_2_x_1 M11(.Y(w11), .D1(w5), .D0(w6), .S(S1));
```

```
mux_2_x_1 M12(.Y(w12), .D1(w7), .D0(w8), .S(S1));
```

```
mux_2_x_1 M13(.Y(w13), .D1(w9), .D0(w10), .S(S2));
```

```
mux_2_x_1 M14(.Y(w14), .D1(w11), .D0(w12), .S(S2));
```

```
mux_2_x_1 M15(.Y(Y), .D1(w13), .D0(w14), .S(S3));
```

```
endmodule
```

```
module mux_2_x_1(
```

```
    output Y,
```

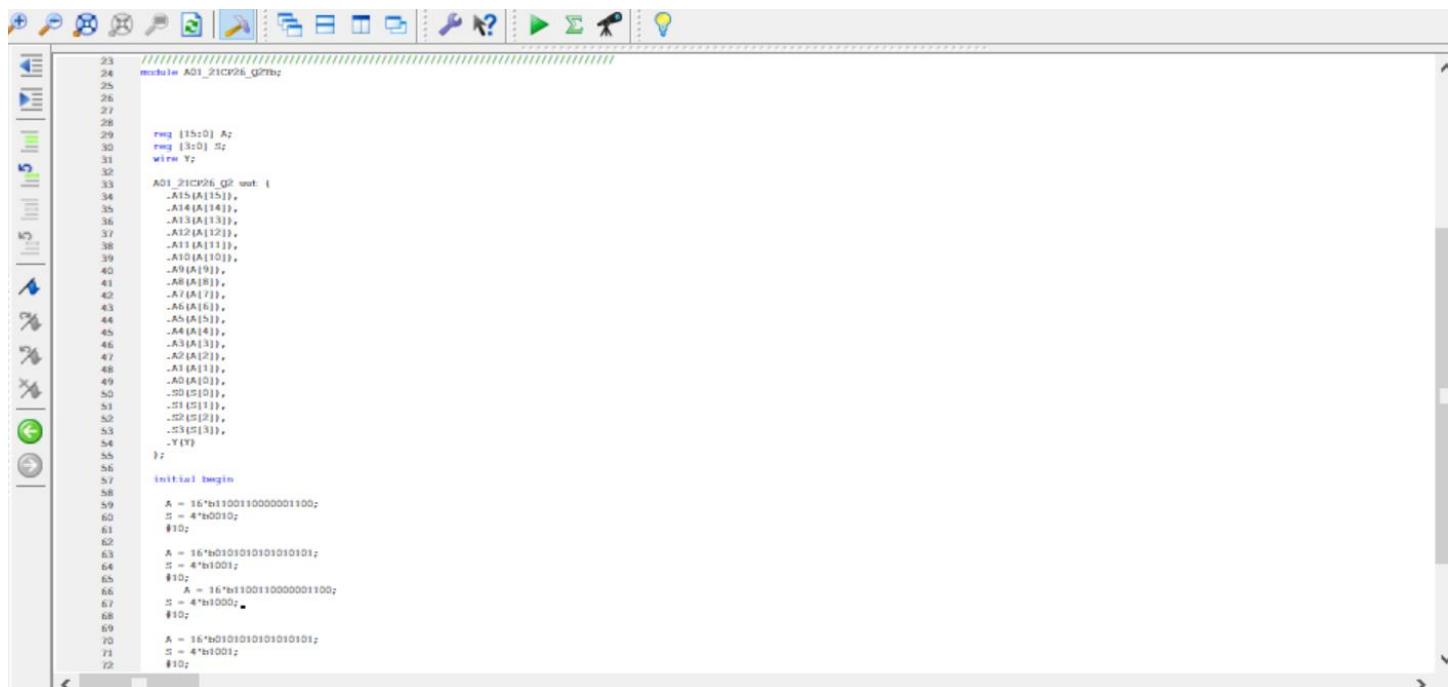
```
    input D1, D0, S
```

```
);
```

```
    assign Y = (S == 0) ? D1 : D0;
```

```
endmodule
```

TestBench:



```
23 module A01_21CP26_Q2tb;
24
25
26
27
28
29     reg [15:0] A2;
30     reg [3:0] S2;
31     wire Y2;
32
33     A01_21CP26_Q2 uut (
34         .A15(A[15]),
35         .A14(A[14]),
36         .A13(A[13]),
37         .A12(A[12]),
38         .A11(A[11]),
39         .A10(A[10]),
40         .A9(A[9]),
41         .A8(A[8]),
42         .A7(A[7]),
43         .A6(A[6]),
44         .A5(A[5]),
45         .A4(A[4]),
46         .A3(A[3]),
47         .A2(A[2]),
48         .A1(A[1]),
49         .A0(A[0]),
50         .SD(S[0]),
51         .SD(S[1]),
52         .SD(S[2]),
53         .SD(S[3]),
54         .Y(Y)
55     );
56
57     initial begin
58
59         A = 16'b1100110000001100;
60         S = 4'b0010;
61         #10;
62
63         A = 16'b0101010101010101;
64         S = 4'b1001;
65         #10;
66         A = 16'b1100110000001100;
67         S = 4'b1000;
68         #10;
69
70         A = 16'b0101010101010101;
71         S = 4'b1001;
72         #10;
73
74     end
75
76 endmodule
```

```
`timescale 1ns / 1ps
```

```
//////////
```

```
// Company:
```

```
// Engineer:
```

```
//
```

```
// Create Date: 15:26:55 01/28/2024
```

```
// Design Name: A01_21CP26_Q2
```

```
// Module Name: G:/semster 6/DSD LAB/ASSIGNMENTS/A01_21_CP_26/A01_21CP26_Q2Tb.v
```

```
// Project Name: A01_21_CP_26
```

```
// Target Device:
```

```
// Tool versions:
```

```
// Description:
```

```
//
```

```
// Verilog Test Fixture created by ISE for module: A01_21CP26_Q2
```

```
//
```

```
// Dependencies:
```

```
//
```

```
// Revision:
```

```
// Revision 0.01 - File Created
```

```
// Additional Comments
```

```
///////////////////////////////
```

```
module A01_21CP26_Q2Tb;
```

```
reg [15:0] A;
```

```
reg [3:0] S;
```

```
wire Y;
```

```
A01_21CP26_Q2 uut (
```

```
.A15(A[15]),
```

```
.A14(A[14]),
```

```
.A13(A[13]),
```

```
.A12(A[12]),
```

```
.A11(A[11]),
```

```
.A10(A[10]),
```

```
.A9(A[9]),
```

```
.A8(A[8]),
```

```
.A7(A[7]),
```

```
.A6(A[6]),
```

```
.A5(A[5]),
```

```
.A4(A[4]),
```

```
.A3(A[3]),
```

```
.A2(A[2]),
```

```
.A1(A[1]),
```

```
.A0(A[0]),
```

```
.S0(S[0]),
```

```
.S1(S[1]),
```

```
.S2(S[2]),
```

```
.S3(S[3]),
```

```
.Y(Y)  
);
```

```
initial begin
```

```
A = 16'b1100110000001100;
```

```
S = 4'b0010;
```

```
#10;
```

```
A = 16'b0101010101010101;
```

```
S = 4'b1001;
```

```
#10;
```

```
A = 16'b1100110000001100;
```

```
S = 4'b1000;
```

```
#10;
```

```
A = 16'b0101010101010101;
```

```
S = 4'b1001;
```

```
#10;
```

```
A = 16'b1100110000001100;
```

```
S = 4'b0110;
```

```
#10;
```

```
A = 16'b0101010101010101;
```

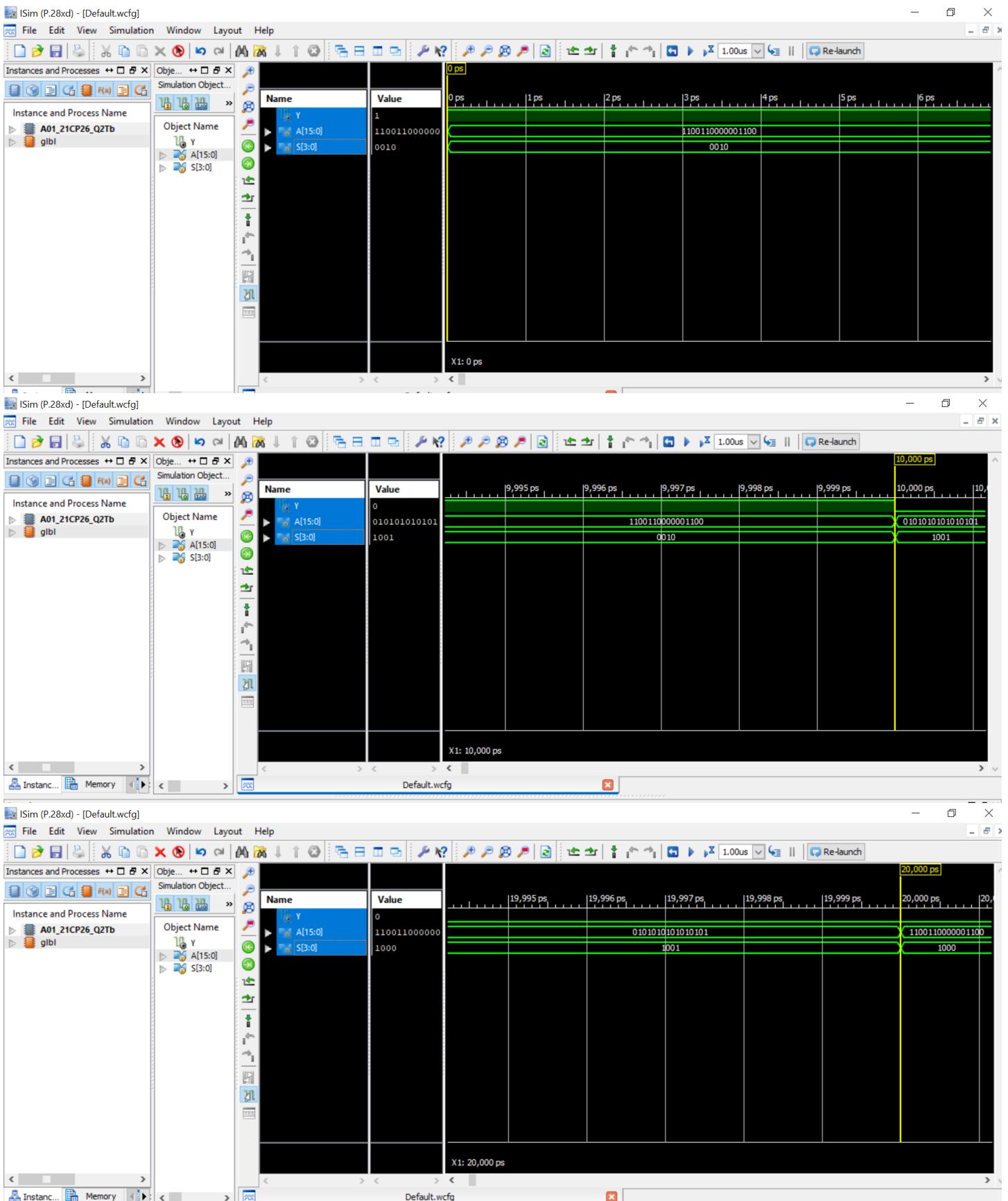
```
S = 4'b1111;
```

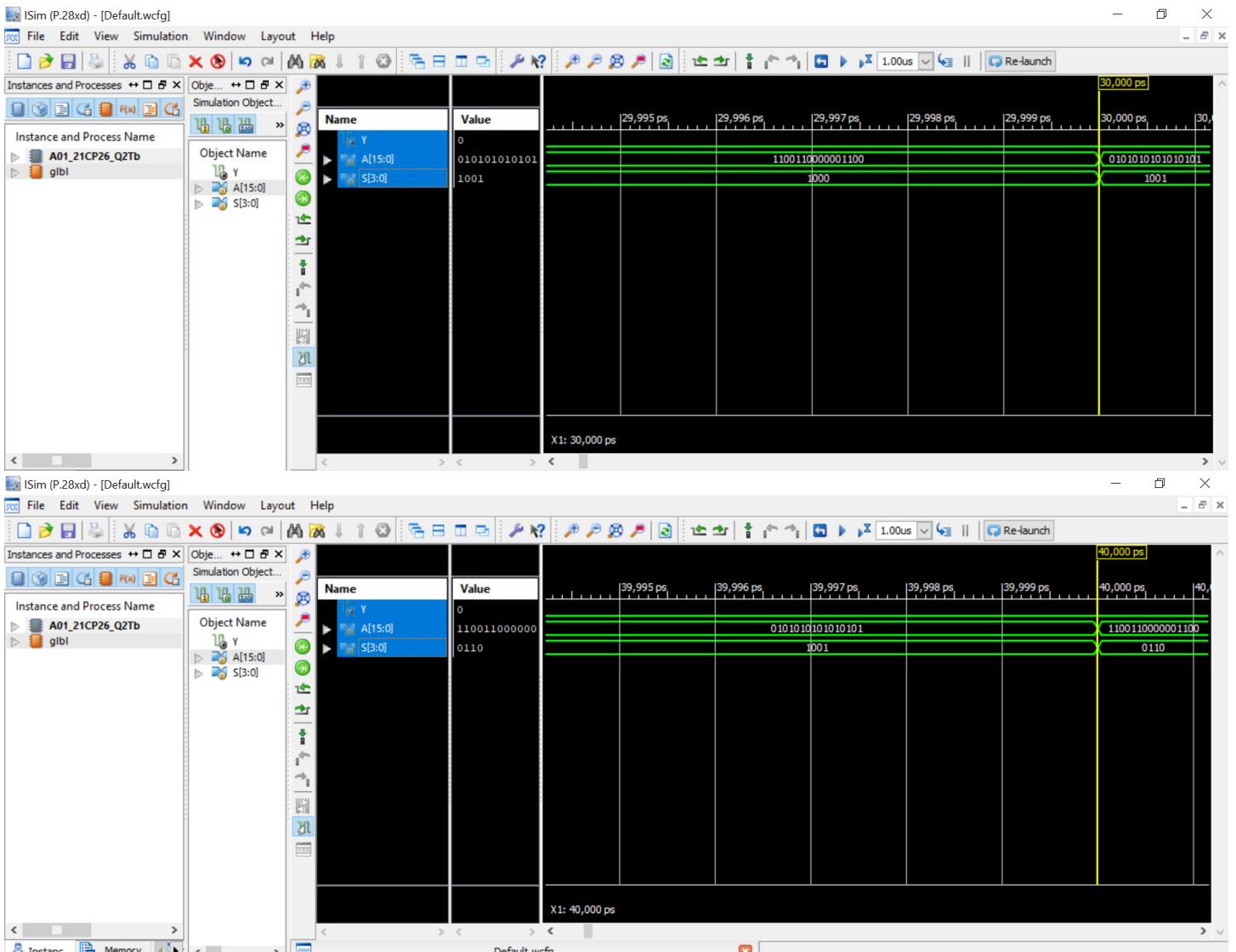
```
#10;
```

```
end
```

```
endmodule
```

Simulation:





3. Design a 3-bit comparator using multiplexer only. The input of the circuit is two 3-bit numbers. The circuit has three binary outputs E, L, and G which become high when A==B, A > B respectively. (20 Marks)

Truth table:

Task 3
3-bit comparator

Truth Table

A_0	A_1	A_2	B_0	B_1	B_2	G	L	E	$A > B$	$A < B$	$A = B$
0	0	0	0	0	0	0	0	1	0	1	0
0	0	0	0	0	1	0	1	0	0	1	0
0	0	0	0	1	0	0	1	0	0	0	1
0	0	0	0	1	1	0	1	0	0	1	0
0	0	0	1	0	0	0	1	0	1	0	0
0	0	0	1	0	1	0	1	0	0	1	0
0	0	0	1	1	0	0	1	0	0	1	0
0	0	0	1	1	1	0	1	0	0	1	0
0	0	1	0	0	0	1	0	0	1	0	0
0	0	1	0	0	1	0	0	1	0	1	0
0	0	1	0	1	0	0	1	0	0	1	0
0	0	1	0	1	1	0	1	0	0	1	0
0	0	1	1	0	0	0	1	0	1	0	0
0	0	1	1	0	1	0	1	0	0	1	0
0	0	1	1	1	0	0	1	0	0	1	0
0	1	0	0	0	0	1	0	0	1	0	0
0	1	0	0	0	1	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	1	0	0
0	1	0	0	1	1	0	0	1	1	0	0
0	1	0	1	0	0	0	0	1	1	1	0
0	1	0	1	0	1	0	0	1	1	1	0
0	1	0	1	1	0	0	0	1	1	1	0
0	1	0	1	1	1	0	0	1	1	1	0
0	1	1	0	0	0	0	0	1	1	1	1
0	1	1	0	0	1	0	0	1	1	1	1
0	1	1	0	1	0	0	0	1	1	1	1
0	1	1	0	1	1	0	0	1	1	1	1
0	1	1	1	0	0	0	0	1	1	1	1
0	1	1	1	0	1	0	0	1	1	1	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	0	1	0	0	1	1	1	1
1	0	0	0	1	0	0	0	1	1	1	1
1	0	0	0	1	1	0	0	1	1	1	1
1	0	0	1	0	0	0	0	1	1	1	1
1	0	0	1	0	1	0	0	1	1	1	1
1	0	0	1	1	0	0	0	1	1	1	1
1	0	0	1	1	1	0	0	1	1	1	1
1	0	1	0	0	0	0	0	1	1	1	1
1	0	1	0	0	1	0	0	1	1	1	1
1	0	1	0	1	0	0	0	1	1	1	1
1	0	1	0	1	1	0	0	1	1	1	1
1	0	1	1	0	0	0	0	1	1	1	1
1	0	1	1	0	1	0	0	1	1	1	1
1	0	1	1	1	0	0	0	1	1	1	1
1	1	0	0	0	0	0	0	1	1	1	1
1	1	0	0	0	1	0	0	1	1	1	1
1	1	0	0	1	0	0	0	1	1	1	1
1	1	0	0	1	1	0	0	1	1	1	1
1	1	0	1	0	0	0	0	1	1	1	1
1	1	0	1	0	1	0	0	1	1	1	1
1	1	0	1	1	0	0	0	1	1	1	1
1	1	0	1	1	1	0	0	1	1	1	1
1	1	1	0	0	0	0	0	1	1	1	1
1	1	1	0	0	1	0	0	1	1	1	1
1	1	1	0	1	0	0	0	1	1	1	1
1	1	1	0	1	1	0	0	1	1	1	1
1	1	1	1	0	0	0	0	1	1	1	1
1	1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	1	1	1	1

Circuit diagram :

E
 $A=B$

$$\begin{array}{cccccc} A_2 & & A_1 & & A_0 & \\ \parallel & \times & \parallel & \times & \parallel & \\ B_2 & & B_1 & & B_0 & \end{array} \Rightarrow A \cdot \bar{B}$$

$$A_2 \Rightarrow \frac{A_2 -}{A_2 B_2 + A_2 \bar{B}_2} \quad \text{X No R} \\ \quad \quad \quad A_2 \oplus B_2 \quad \quad \quad : ID$$

$$A_1 \Rightarrow A_1 \oplus B_1 \quad A_0 = B_0$$

$$A_0 \Rightarrow A_0 \oplus B_0$$

$$E = (A_1 \oplus B_1) \cdot (A_2 \oplus B_2) \cdot (A_0 \oplus B_0)$$

G $A \geq B$
3 case

(1) ~~$A_2 = B_2, A_1 = B_1, A_0 > B_0$~~
 ~~$(A_2 \oplus B_2) \cdot (A_1 \oplus B_1) \cdot (A_0 \cdot \bar{B}_0)$~~
 ~~$A_2 = 1 \quad B_2 = 0$~~

1) $A_2 > B_2 \quad \underline{A_2 = 1 \quad B_2 = 0}$
 $A_2 \cdot \bar{B}_2$

b) $A_2 = B_2, A_1 \supset B_1$

$$(A_2 \odot B_2) \cdot (A_1, \bar{B}_1)$$

c) $A_2 = B_2, A_1 = B_2, A_0 \supset B_0$

$$(A_2 \odot B_2) \cdot (A_1 \odot B_1) \cdot (A_0 \cdot \bar{B})$$

$L \quad A \subset B$

a) $A_2 \subset B_2, A_2 \supseteq B_2 \equiv$

$$\bar{A}_2 \cdot B_2$$

b) $A_2 = B_2, A_1 \subset B_1$

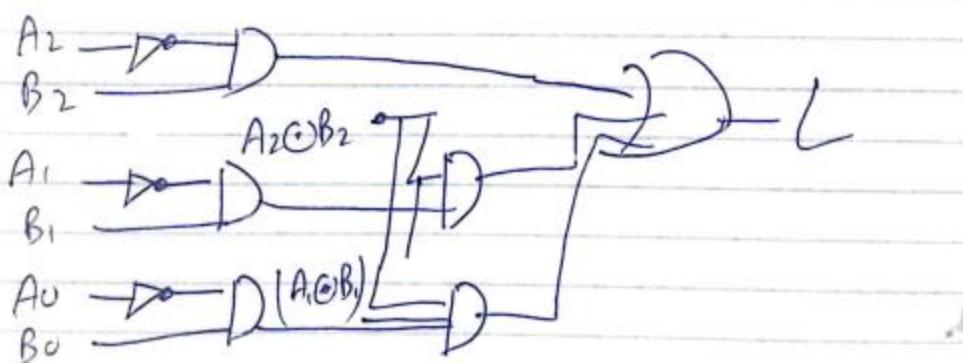
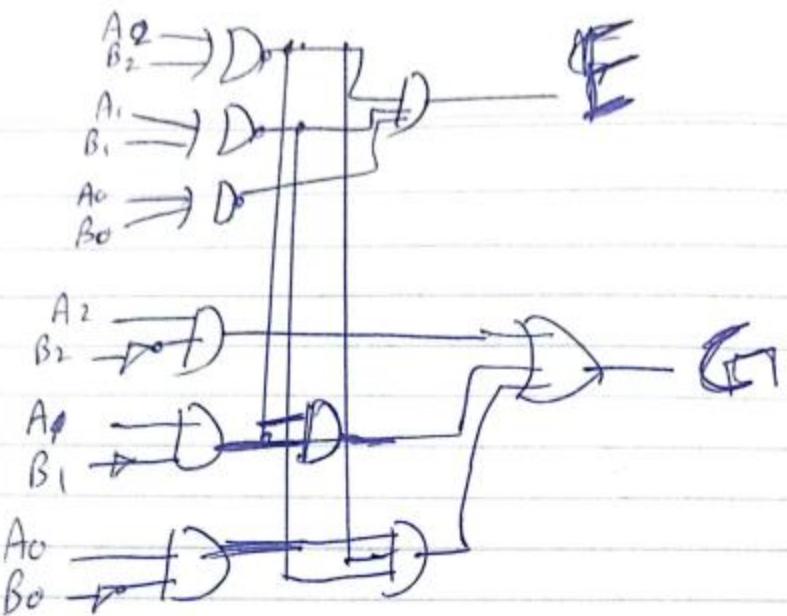
$$(A_2 \odot B_2) \cdot \bar{A}_1, B_1$$

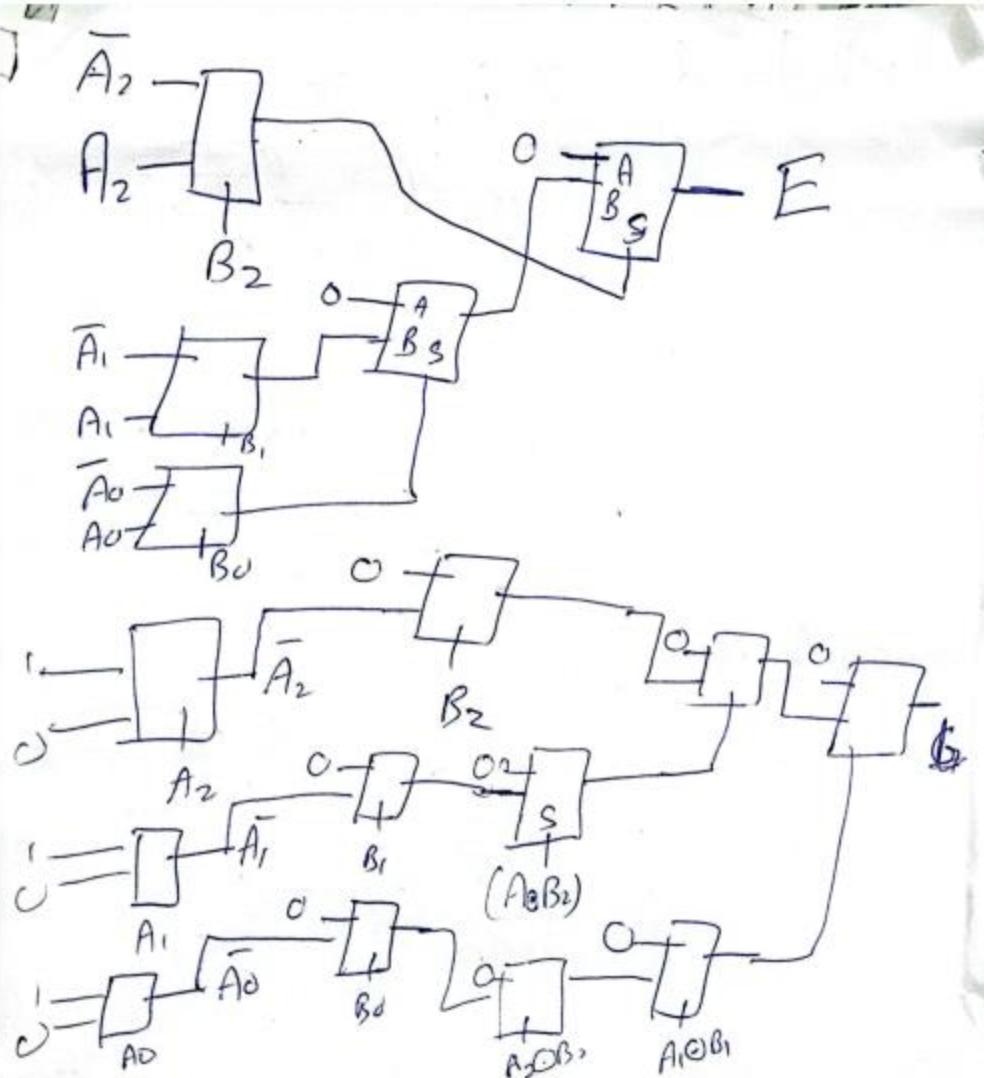
c) $A_2 = B_2, A_1 = B_1, A_1 \subset B_1$

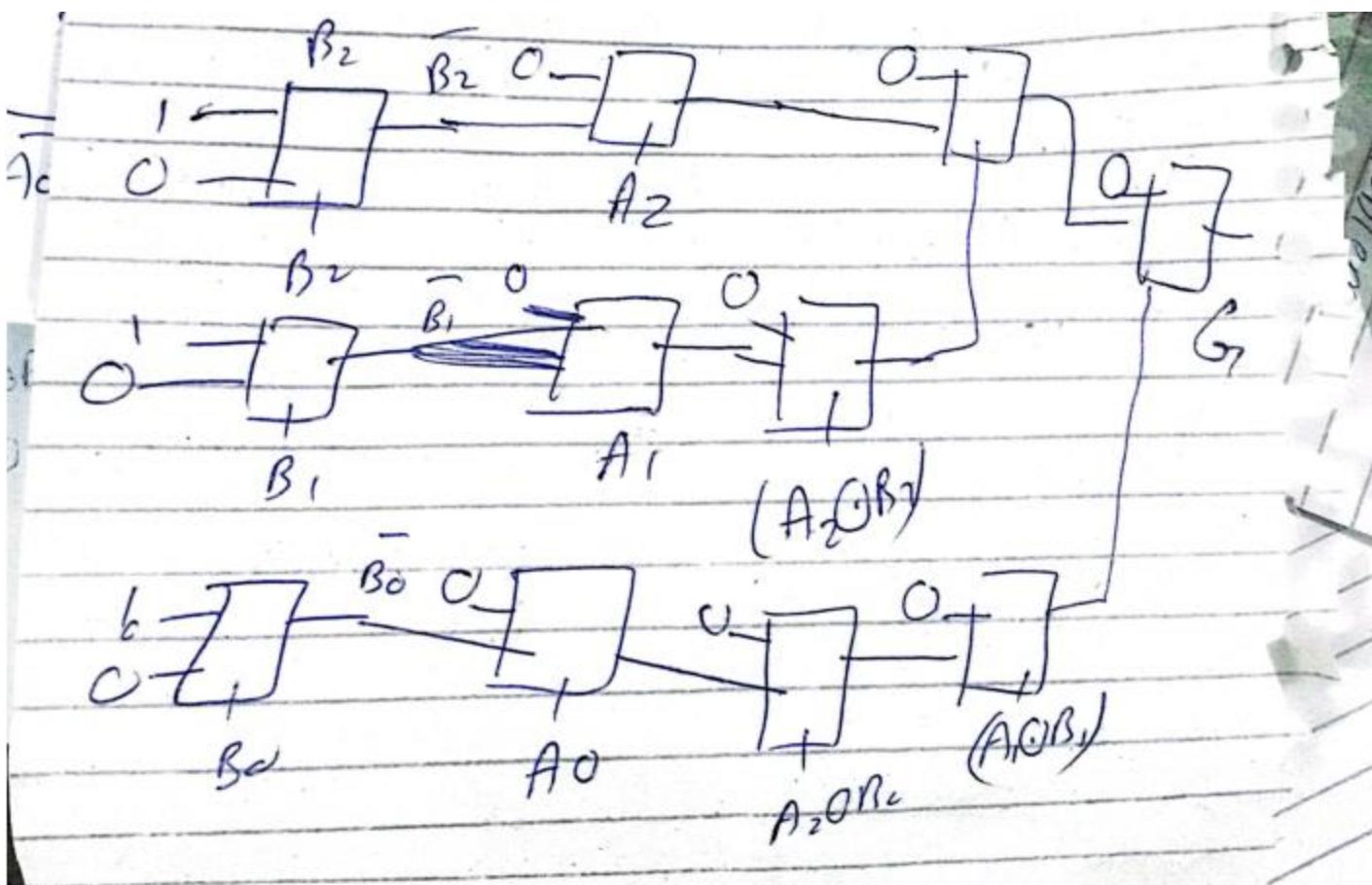
$$(A_2 \odot B_2) \cdot (A_1 \odot B_1) \cdot \bar{A}_1, B_1$$

$$L = \bar{A}_2 \cdot B_2 + (A_2 \odot B_2) \cdot \bar{A}_1, B_1$$

$$\textcircled{2} + (A_2 \odot B_2) \cdot (A_1 \odot B_1) \cdot \bar{A}_1, B_1$$







Code:

ISE Project Navigator (P.28xd) - G:\semester 6\DS_D LAB\ASSIGNMENTS\A01_21_CP_26\A01_21_CP_26.xise - [A01_21CP26_Q3.v]

File Edit View Project Source Process Tools Window Layout Help

Files

```
21 module A01_21CP26_Q3(output G,L,E,
22   input [2:0] A,[2:0] B
23   );
24   XNOR x1(
25     .Y(w1), .A(A[0]), .B(B[0]));
26   XNOR x2(
27     .Y(w2), .A(A[1]), .B(B[1]));
28   XNOR x3(
29     .Y(w3), .A(A[2]), .B(B[2]));
30   And_3 A1(
31     .Y(E), .A(w1), .B(w2), .C(w3));
32   AND A2(.Y(w4), .A(A[2]), .B(B[2]));
33   AND A3(.Y(w5), .A(A[1]), .B(B[1]));
34   AND A4(.Y(w6), .A(A[0]), .B(B[0]));
35   AND A5(.Y(w7), .A(w1), .B(w4));
36   AND A6(.Y(w8), .A(w2), .B(w5));
37   And_3 A7(.Y(G), .A(w7), .B(w6), .C(w8));
38   AND A8(.Y(w9), .A(A[2]), .B(B[2]));
39   AND A9(.Y(w10), .A(A[1]), .B(B[1]));
40   AND A10(.Y(w11), .A(A[0]), .B(B[0]));
41   AND A88(.Y(w11), .A(w1), .B(w10));
42   AND A88(.Y(w10), .A(w2), .B(w11));
43   AND b88(.Y(w12), .A(w3), .B(w11));
44
45   OR_3 A888(
46     .Y(L), .A(w9), .B(w12));
47
48 endmodule
```

Design Files Library

A01_21CP26_Q1ETb.v A01_21CP26_Q1E.v A01_21CP26_Q2.v A01_21CP26_Q2Tb.v A01_21CP26_Q3Tb.v A01_21CP26_Q3.v

ISE Project Navigator (P.28xd) - G:\semester 6\DS_D LAB\ASSIGNMENTS\A01_21_CP_26\A01_21_CP_26.xise - [A01_21CP26_Q3.v]

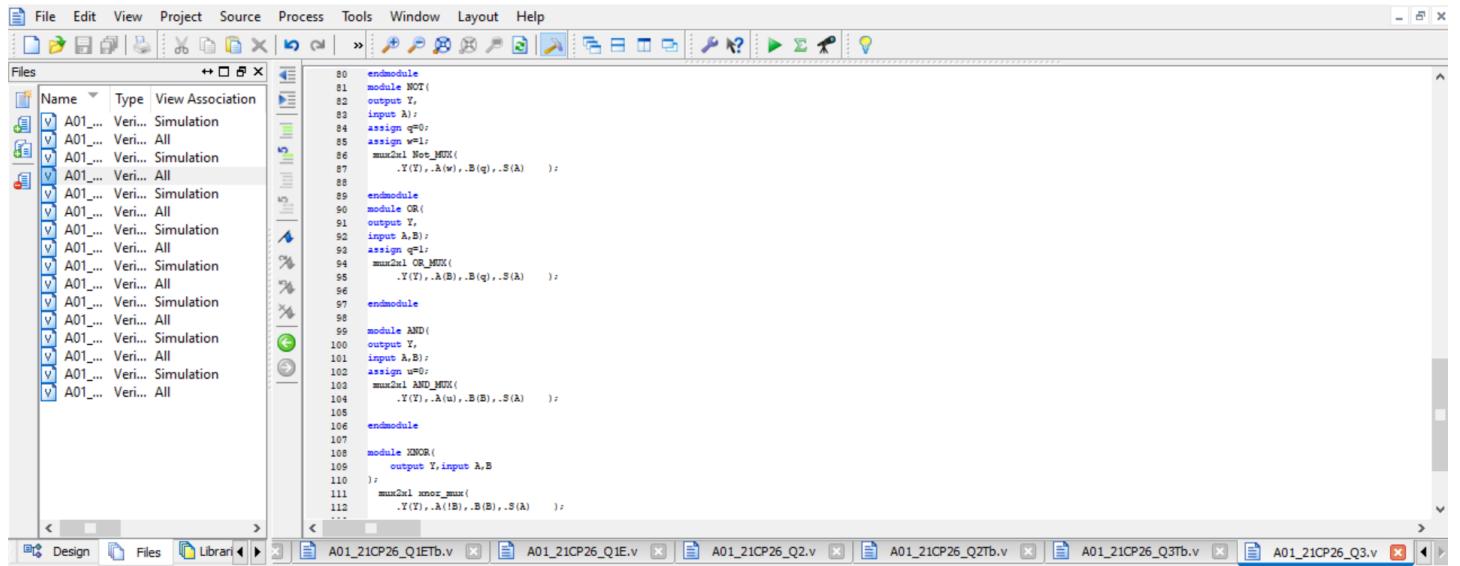
File Edit View Project Source Process Tools Window Layout Help

Files

```
53 module OR_3(
54   output Y,
55   input A,B,C);
56   assign q=0;
57   assign w=1;
58   wire w1;
59   mux21 OR0_MUX(
60     .Y(w1), .A(C), .B(1), .S(B));
61   mux21 OR1_MUX(
62     .Y(Y), .A(w1), .B(1), .S(A));
63
64
65
66
67 endmodule
68 module And_3(
69   output Y,
70   input A,B,C);
71   assign q=0;
72   assign w=1;
73   wire w1;
74   mux21 AND0_MUX(
75     .Y(w1), .A(q), .B(C), .S(B));
76   mux21 AND1_MUX(
77     .Y(Y), .A(q), .B(w1), .S(A));
78
79
80 endmodule
81 module NOT(
82   output Y,
83   input A);
84   assign q=0;
85   assign w=1;
```

Design Files Library

A01_21CP26_Q1ETb.v A01_21CP26_Q1E.v A01_21CP26_Q2.v A01_21CP26_Q2Tb.v A01_21CP26_Q3Tb.v A01_21CP26_Q3.v



```

107
108 module XNOR(
109   output Y, input A,B
110 );
111   mux2xl xnor_mux(
112     .Y(Y), .A(!B), .B(B), .S(A)    );
113
114 endmodule
115 module mux2xl(
116   output Y,
117   input A,B,S;
118   assign Y=(S==0)?A:B;
119 endmodule
120

```

'timescale 1ns / 1ps

//

// Company:

// Engineer:

//

// Create Date: 23:19:59 02/02/2024

// Design Name:

// Module Name: A01_21CP26_Q3

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

```
//////////
```

```
module A01_21CP26_Q3(output G,L,E,
```

```
input [2:0] A,[2:0] B
```

```
);
```

```
XNOR x1(
```

```
.Y(w1), .A(A[0]),.B(B[0]));
```

```
XNOR x2(
```

```
.Y(w2), .A(A[1]),.B(B[1]));
```

```
XNOR x3(
```

```
.Y(w3), .A(A[2]),.B(B[2]));
```

```
And_3 A1(
```

```
.Y(E),.A(w1),.B(w2),.C(w3));
```

```
AND A2(.Y(w4),.A(A[2]),.B(!B[2]));
```

```
AND A3(.Y(w5),.A(A[1]),.B(!B[1]));
```

```
AND A4(.Y(w6),.A(A[0]),.B(!B[0]));
```

```
AND A5(.Y(w7),.A(w1),.B(w4));
```

```
AND A6(.Y(w8),.A(w2),.B(w6));
```

```
And_3 A7(.Y(G),.A(w7),.B(w5),.C(w8));
```

```
AND A88(.Y(w9),.A(!A[2]),.B(B[2]));
```

```
AND A98(.Y(w10),.A(!A[1]),.B(B[1]));
```

```
AND A108(.Y(w11),.A(!A[0]),.B(B[0]));
```

```
AND A888(.Y(w11),.A(w1),.B(w10));
```

```
AND b88(.Y(w12),.A(w2),.B(w11));
```

```
OR_3 A9888(
```

```
.Y(L),.A(w9),.B(w11),.C(w12));
```

```
endmodule
```

```
module OR_3(
```

```
output Y,
```

```
input A,B,C);
```

```
assign q=0;
```

```
assign w=1;
```

```

wire w1;

mux2x1 OR0_MUX(
    .Y(w1),.A(C),.B(1),.S(B)  );
mux2x1 OR1_MUX(
    .Y(Y),.A(w1),.B(1),.S(A)  );

endmodule

module And_3(
    output Y,
    input A,B,C);
    assign q=0;
    assign w=1;
    wire w1;
    mux2x1 AND0_MUX(
        .Y(w1),.A(q),.B(C),.S(B)  );
    mux2x1 AND1_MUX(
        .Y(Y),.A(q),.B(w1),.S(A)  );

endmodule

module NOT(
    output Y,
    input A);
    assign q=0;
    assign w=1;
    mux2x1 Not_MUX(
        .Y(Y),.A(w),.B(q),.S(A)  );

endmodule

module OR(
    output Y,
    input A,B);
    assign q=1;
    mux2x1 OR_MUX(
        .Y(Y),.A(B),.B(q),.S(A)  );

endmodule

```

```
module AND(
    output Y,
    input A,B);
    assign u=0;
    mux2x1 AND_MUX(
        .Y(Y),.A(u),.B(B),.S(A) );
```

endmodule

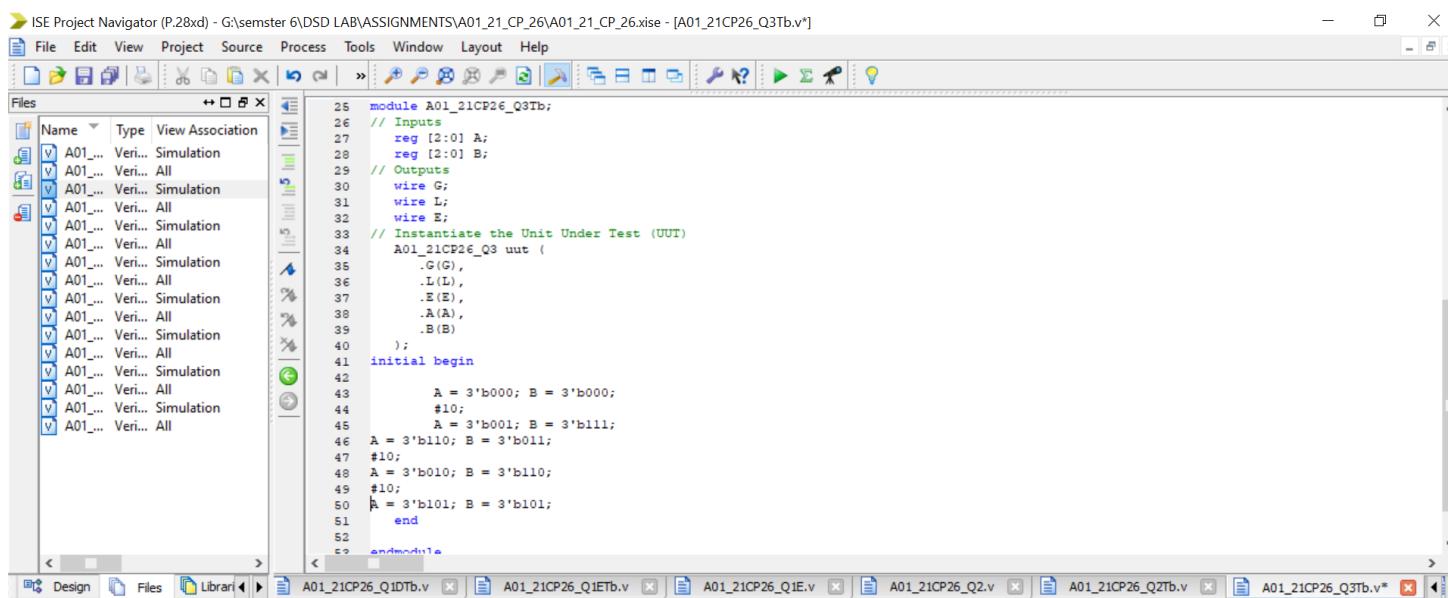
module XNOR(

```
    output Y,input A,B  
);  
  
mux2x1 xnor_mux(  
    .Y(Y),.A(!B),.B(B),.S
```

endmodule

```
module mux2x1(  
    output Y,  
    input A,B,S);  
  
    assign Y=(S==0)?A:B;  
  
endmodule
```

TestBench:



`timescale 1ns / 1ns

```
// Company:  
// Engineer:  
//  
// Create Date: 00:12:08 02/03/2024  
// Design Name: A01_21CP26_Q3  
// Module Name: G:/semster 6/DSD LAB/ASSIGNMENTS/A01_21_CP_26/A01_21CP26_Q3Tb.v  
// Project Name: A01_21_CP_26  
// Target Device:  
// Tool versions:  
// Description:  
//  
// Verilog Test Fixture created by ISE for module: A01_21CP26_Q3  
//  
// Dependencies:  
//  
// Revision:  
// Revision 0.01 - File Created  
// Additional Comments:  
//  
||||||||||||||||||||||||||||||||||||||||||||||||
```

```
module A01_21CP26_Q3Tb;  
// Inputs  
    reg [2:0] A;  
    reg [2:0] B;  
// Outputs  
    wire G;  
    wire L;  
    wire E;  
// Instantiate the Unit Under Test (UUT)  
A01_21CP26_Q3 uut (  
    .G(G),  
    .L(L),  
    .E(E),  
    .A(A),  
    .B(B)  
);  
initial begin
```

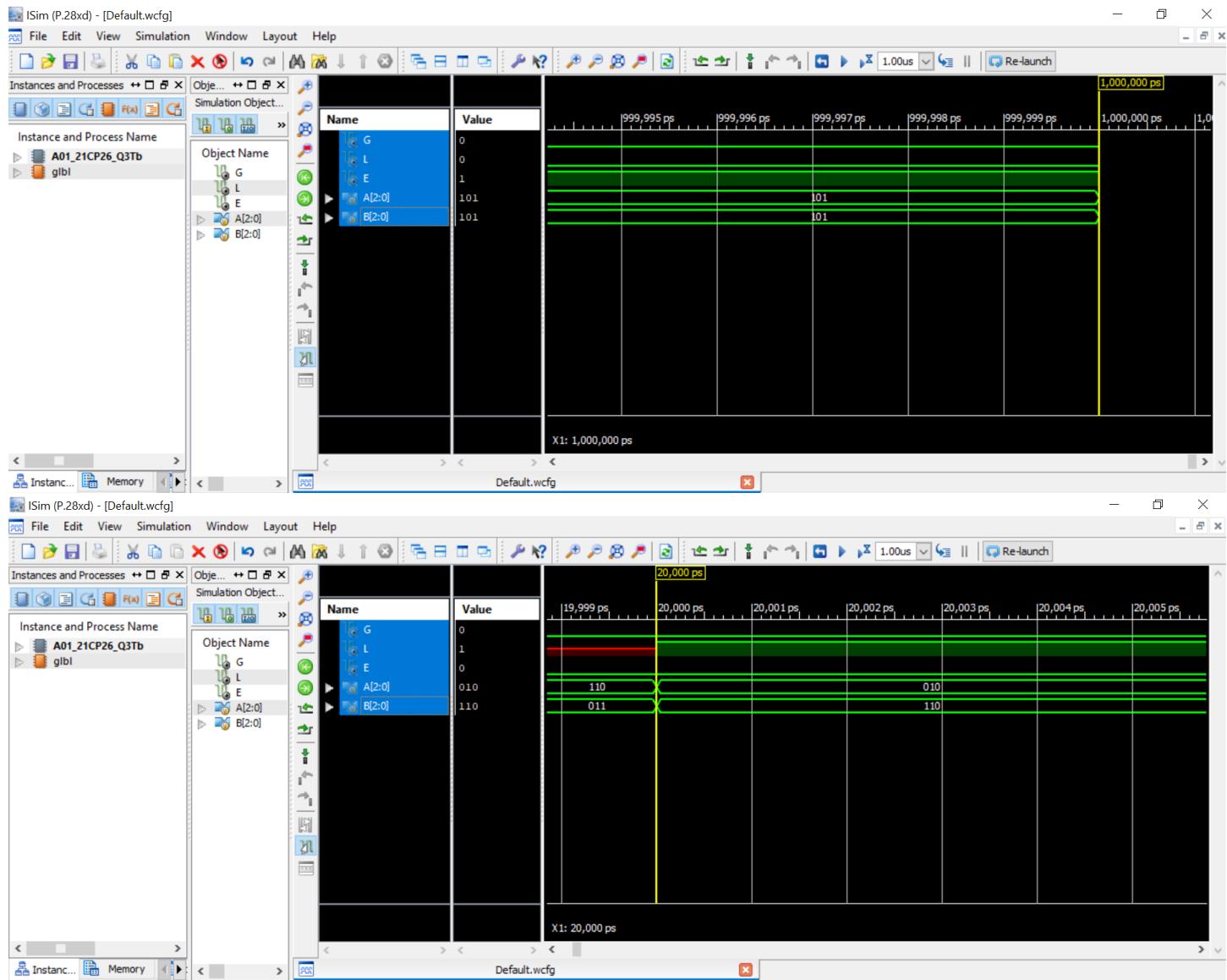
```

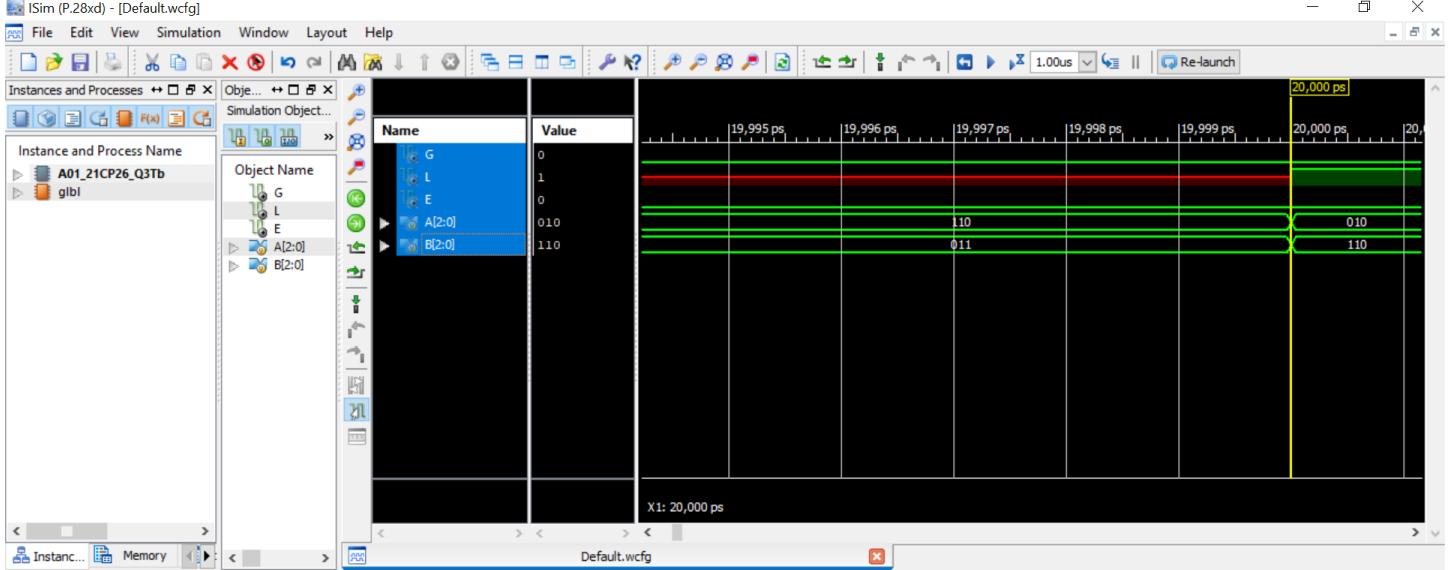
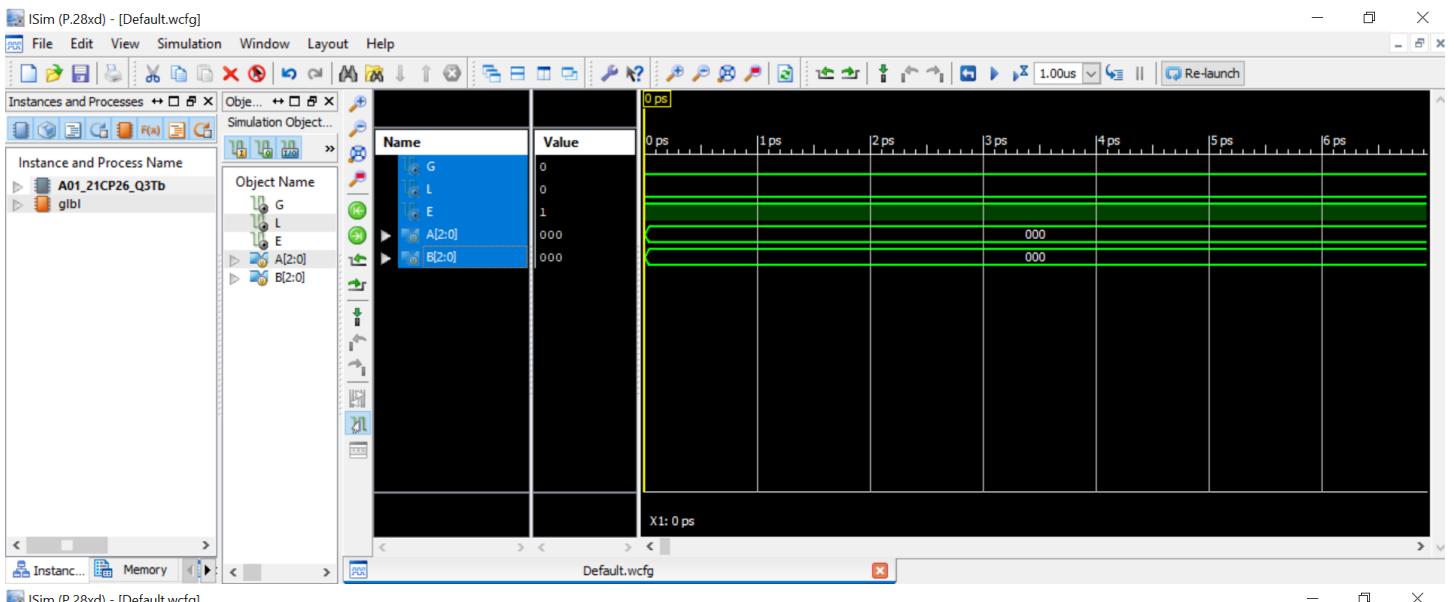
A = 3'b000; B = 3'b000;
#10;
A = 3'b001; B = 3'b111;
A = 3'b110; B = 3'b011;
#10;
A = 3'b010; B = 3'b110;
#10;
A = 3'b101; B = 3'b101;
end

```

```
endmodule
```

Simulation:





4. Design 8 bit even parity detector using multiplexer only. The input of the circuit is a 4-bit number. The circuit provides a binary output E which becomes high for the even parity. (20 Marks)

Truth table:

C-Nay Even Parity

A	B	C	D	P?
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

		∞	0^1	11	10
		CD			
	AB	00	00	11	10
		01		11	10
		10		11	10

$$P = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}D$$

$$+ \bar{A}BC\bar{D} + A\bar{B}\bar{C}\bar{D} + ABCD$$

$$+ A\bar{B}\bar{C}D + A\bar{B}C\bar{D}$$

$$X \oplus Y = X\bar{Y} + \bar{X}Y$$

$$X \odot Y = X\bar{Y} + \bar{X}Y$$

$$X \odot Y = \overline{X \oplus Y}$$

W
L
S.

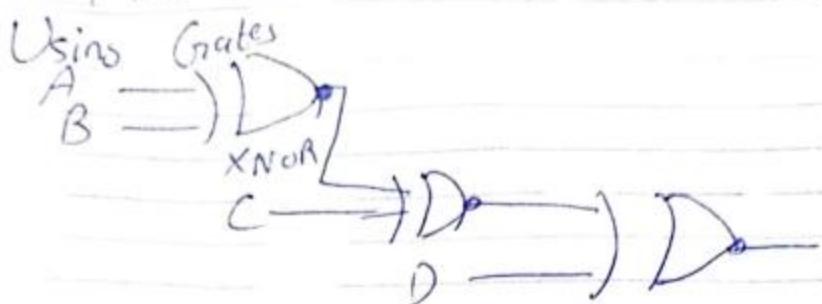
Circuit diagram :

$$\begin{aligned}
&= \bar{A}\bar{B}(\bar{C}\bar{D} + CD) + \bar{A}B(\bar{C}D + C\bar{D}) \\
&\quad + AB(\bar{C}\bar{D} + CD) + A\bar{B}(C\bar{D} + \bar{C}\bar{D}) \\
&= \bar{A}\bar{B}(C \oplus D) + \bar{A}B(C \oplus D) \\
&\quad + AB(C \odot D) + A\bar{B}(C \oplus D) \\
&= (C \odot D)(\bar{A}\bar{B} + AB) + (C \oplus D)(\bar{A}\bar{B} + AB) \\
&= (C \odot D)(A \odot B) + (C \oplus D)(A \oplus B) \\
&= (C \odot D)(A \odot B) + (\bar{C} \odot \bar{D})(\overline{A \odot B})
\end{aligned}$$

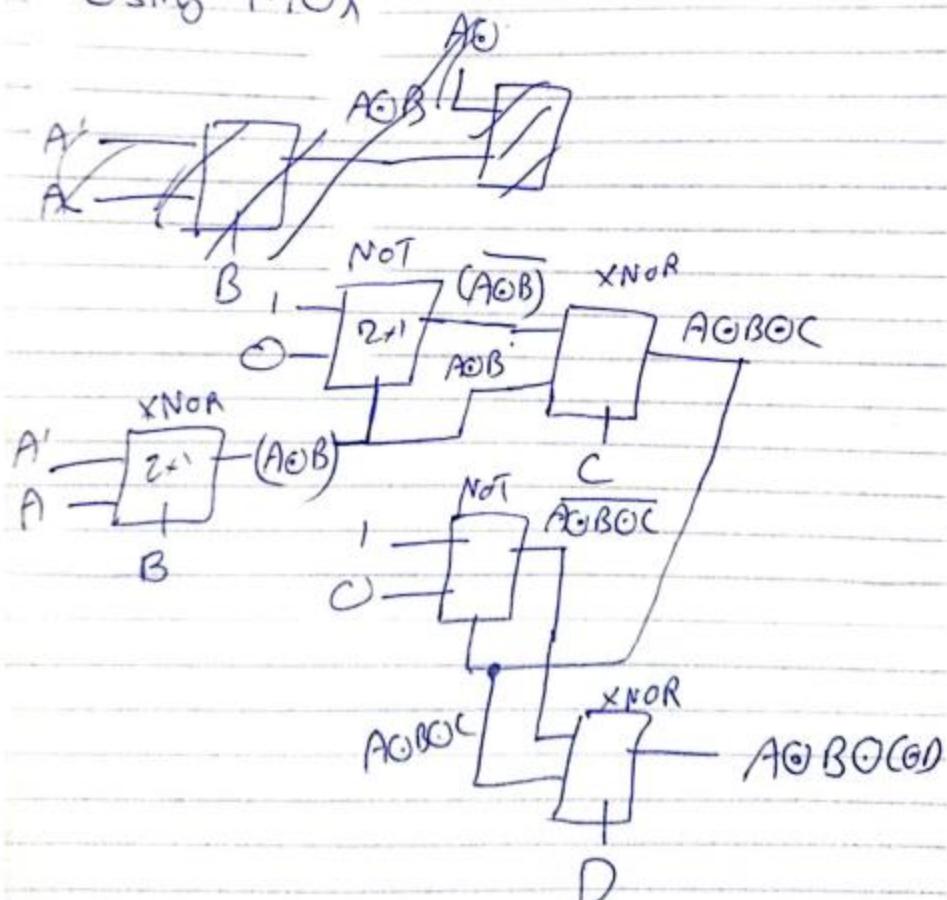
$$\begin{aligned}
&\Rightarrow Y \cdot X + \bar{Y} \cdot \bar{X} \\
&\Rightarrow XY + \bar{X}\bar{Y} \\
&= X \odot Y
\end{aligned}
\qquad
\begin{aligned}
A \odot B &= Y \\
C \odot D &= Y \\
&\quad X \text{ NOR}
\end{aligned}$$

$$= A \odot B \odot C \odot D$$

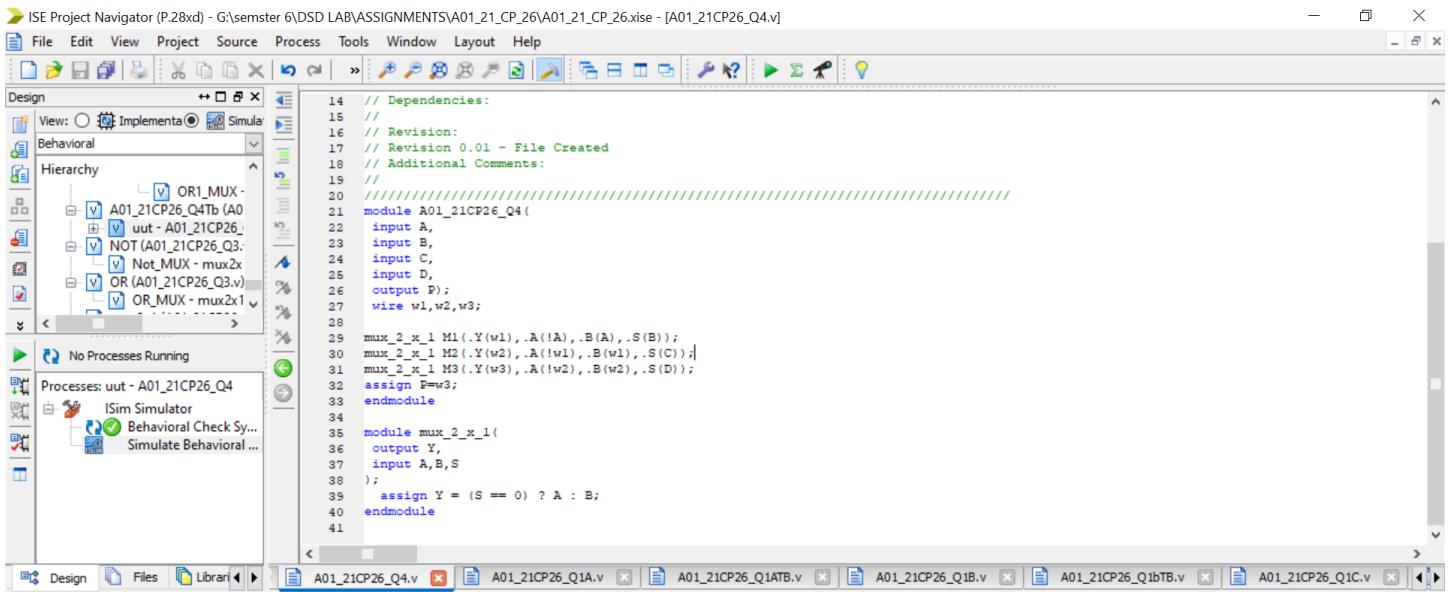
$A \oplus B \odot C \odot D$



Using MUX



Code:



```
'timescale 1ns / 1ps
///////////////////////////////
// Company:
// Engineer:
//
// Create Date: 16:30:40 01/28/2024
// Design Name:
// Module Name: A01_21CP26_Q4
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
/////////////////////////////
```

```
module A01_21CP26_Q4(
    input A,
    input B,
    input C,
    input D,
```

```

output P);

wire w1,w2,w3;

mux_2_x_1 M1(.Y(w1),.A(!A),.B(A),.S(B));
mux_2_x_1 M2(.Y(w2),.A(!w1),.B(w1),.S(C));
mux_2_x_1 M3(.Y(w3),.A(!w2),.B(w2),.S(D));

assign P=w3;

endmodule

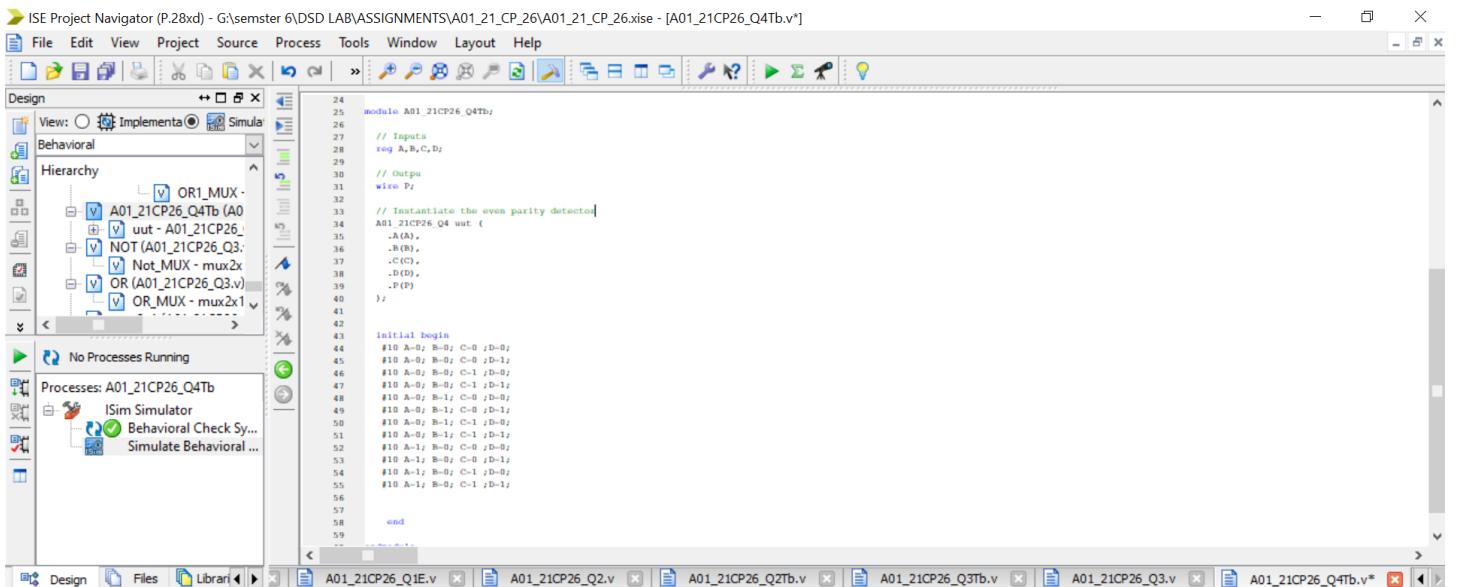
```

```

module mux_2_x_1(
    output Y,
    input A,B,S
);
    assign Y = (S == 0) ? A : B;
endmodule

```

TestBench:



```

`timescale 1ns / 1ps

///////////////////////////////
// Company:
// Engineer:
//
// Create Date: 16:32:50 01/28/2024
// Design Name: A01_21CP26_Q4
// Module Name: G:/semster 6/DSD LAB/ASSIGNMENTS/A01_21_CP_26/A01_21CP26_Q4Tb.v
// Project Name: A01_21_CP_26

```



```

#10 A=0; B=1; C=1 ;D=0;
#10 A=0; B=1; C=1 ;D=1;
#10 A=1; B=0; C=0 ;D=0;
#10 A=1; B=0; C=0 ;D=1;
#10 A=1; B=0; C=1 ;D=0;
#10 A=1; B=0; C=1 ;D=1;

```

end

endmodule

Simulation:

