University of Engineering and Technology,Taxila

Department of Computer Engineering

Lab Report 02

For the Course of DSD lab

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Section: Omega

Lab Instructor: Sir Shahid Ali

Course Instructor: Dr.Abdul rehman aslam

Date: 20-01-24.

Course Title: DSD Lab

Lab Tasks

Questions:

1. Design and Simulate four-input OR, XOR and XNOR gates using 2 input primitive gates

Code:

```
module q1(
  input wire a, b, c, d,
  output wire or_out, xor_out, xnor_out
);

  wire ab_or, cd_or;
  wire ab_xor, cd_xor;
  wire xnor_temp;

  assign ab_or = a | b;
  assign cd_or = c | d;

  assign ab_xor = a ^ b;
  assign cd_xor = c ^ d;

  assign xnor_temp = ~(ab_xor | cd_xor);

  assign or_out = ab_or | cd_or;

  assign xor_out = ab_xor ^ cd_xor;
  assign xnor_out = xnor_temp;
endmodule
```

timescale 1ns / 1ps

//

// Company:

// Engineer:

//

// Create Date: 12:45:09 01/17/2024

// Design Name:

// Module Name: q1

// Project Name:

// Target Devices:

// Tool versions:

```
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////

module q1(
  input wire a, b, c, d,
  output wire or_out, xor_out, xnor_out
);

  wire ab_or, cd_or;
  wire ab_xor, cd_xor;
  wire xnor_temp;

  assign ab_or = a | b;
  assign cd_or = c | d;

  assign ab_xor = a ^ b;
  assign cd_xor = c ^ d;

  assign xnor_temp = ~(ab_xor | cd_xor);

  assign or_out = ab_or | cd_or;

  assign xor_out = ab_xor ^ cd_xor;
  assign xnor_out = xnor_temp;
```

```
endmodule
```

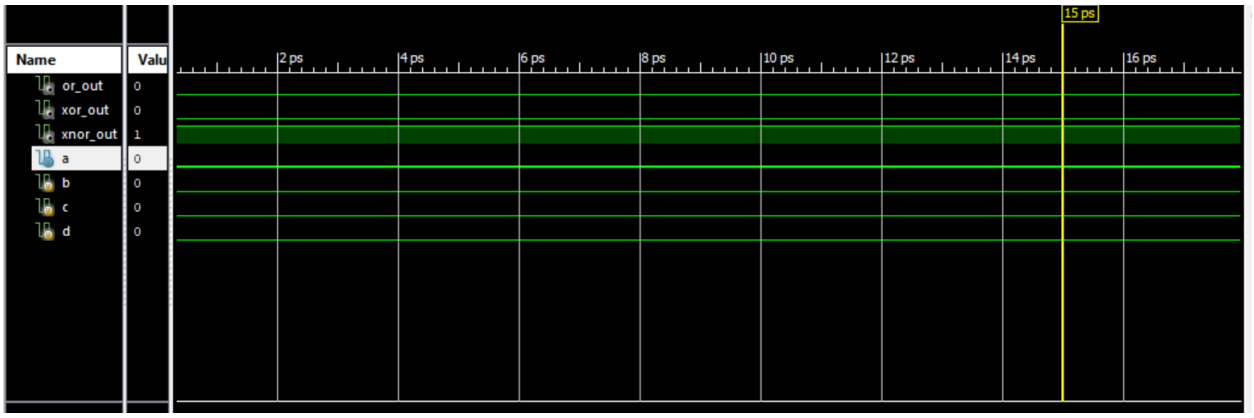
TestBench:

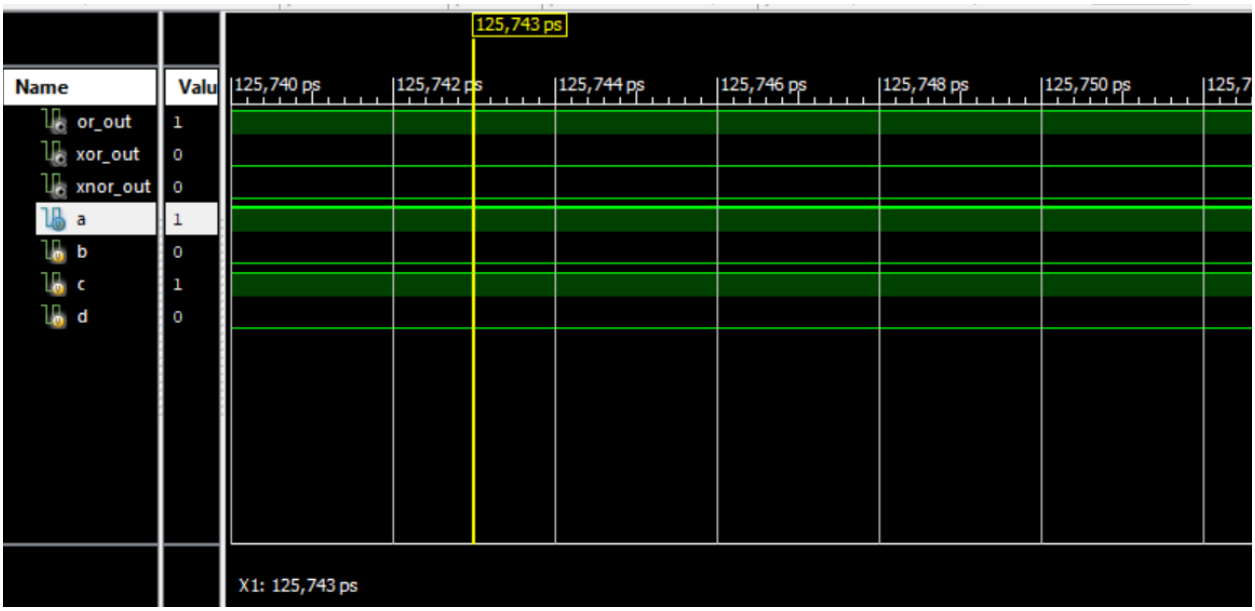
```
// Create Date:   13:00:06 01/17/2024
// Design Name:   q1
// Module Name:   C:/Users/Ibrahim/Desktop/New folder/CP21_26_Lab2_Qn1/q1test.v
// Project Name:  CP21_26_Lab2_Qn1

module q1test;

	// Inputs
	reg a;
	reg b;
	reg c;
	reg d;

	// Outputs
	wire or_out;
	wire xor_out;
	wire xnor_out;

	// Instantiate the Unit Under Test (UUT)
	q1 uut (
		.a(a),
		.b(b),
		.c(c),
		.d(d),
		.or_out(or_out),
		.xor_out(xor_out),
		.xnor_out(xnor_out)
	);

	 initial begin
  // Initialize Inputs
  a = 0;
```

```
    b = 0;
    c = 0;
    d = 0;

    // Wait 100 ns for global reset to finish
    #100;

    // Test sequence
    // Case 1: a=0, b=0, c=0, d=0
    #10 a = 0; b = 0; c = 0; d = 0;

    // Case 2: a=1, b=0, c=1, d=0
    #10 a = 1; b = 0; c = 1; d = 0;

    // Case 3: a=1, b=1, c=0, d=1
    #10 a = 1; b = 1; c = 0; d = 1;

    // Add more test cases as needed

  end

endmodule
```

```
module qltest;
    // Inputs
   reg a;
   reg b;
   reg c;
   reg d;
   // Outputs
   wire or_out;
   wire xor_out;
   wire xnor_out;
   // Instantiate the Unit Under Test (UUT)
   ql uut (
      .a(a),
      .b(b),
      .c(c),
      .d(d),
      .or_out(or_out),
      .xor_out(xor_out),
      .xnor_out(xnor_out)
   );
   initial begin
    a = 0;
    b = 0;
    c = 0;
    d = 0;
    #100;
    // Test sequence
    #10 a = 0; b = 0; c = 0; d = 0;
    #10 a = 1; b = 0; c = 1; d = 0;
    #10 a = 1; b = 1; c = 0; d = 1;
    end
endmodule
```

Simulations :





Task 2:

2. Simulate the design given in Figure. 1 using gate level modeling.

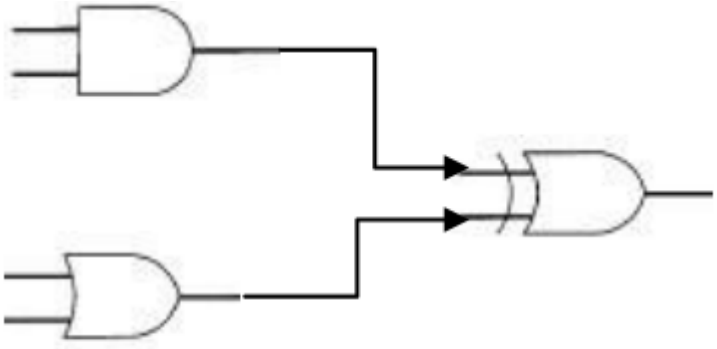


Figure 1: Design-1 for Lab Tasks

Code:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    13:20:54 01/17/2024
// Design Name:
// Module Name:    q2
// Project Name:
```

```
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module q2(input wire a, b, c, d,
 output wire y_xor);


wire w1;
wire w2;
and a1 (w1,a,b);
or a2 (w2,c,d);
xor a3 (y_xor,w1,w2);
endmodule
```

```
module q2(input wire a, b, c, d,
  output wire y_xor);

wire w1;
wire w2;
and a1 (w1,a,b);
or a2 (w2,c,d);
xor a3 (y_xor,w1,w2);



endmodule
```

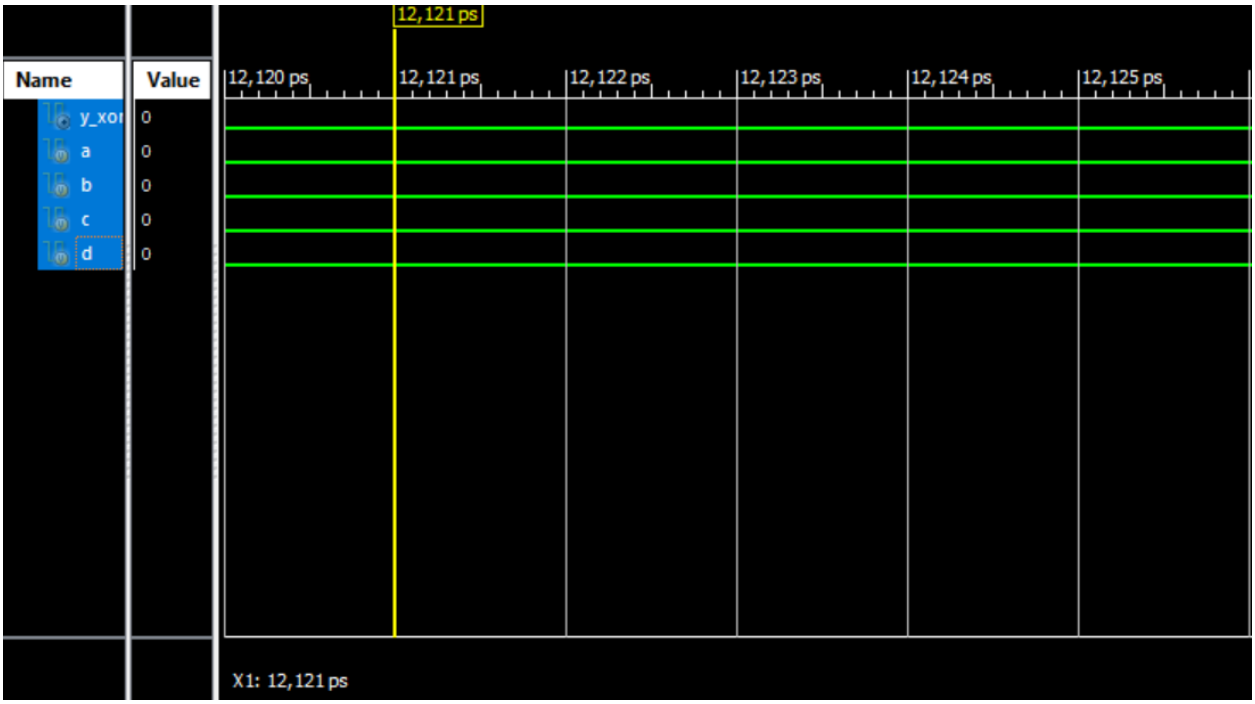
TestBench:

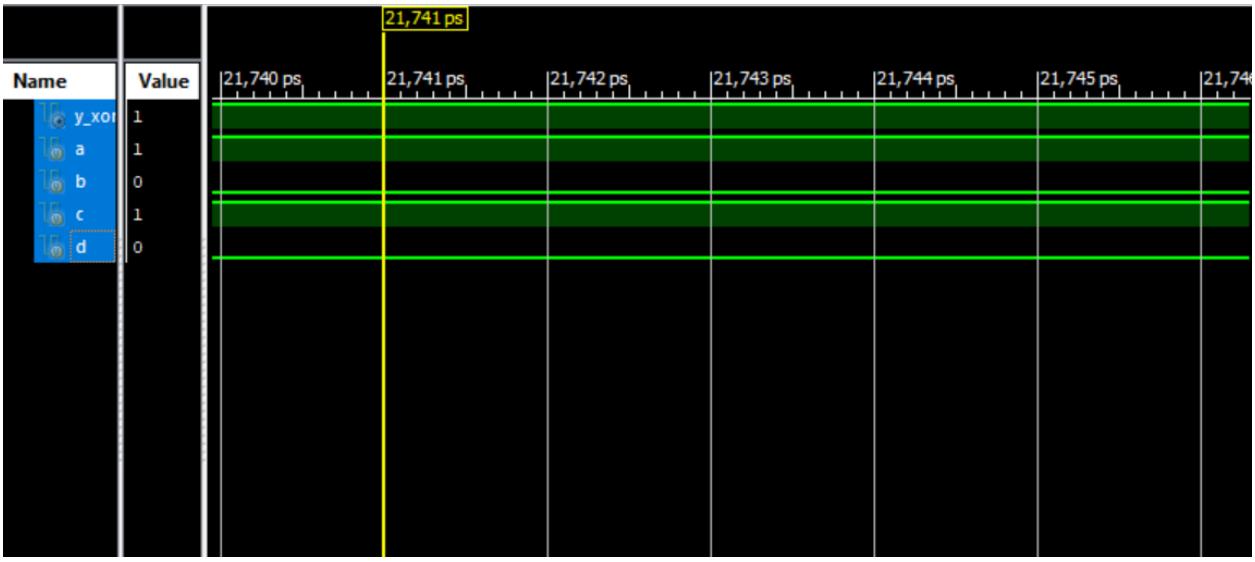
```
`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:   14:46:09 01/17/2024
// Design Name:   q2
// Module Name:   C:/Users/Ibrahim/Desktop/New folder/CP21_26_Lab1_Qn2/q2test.v
// Project Name:  CP21_26_Lab1_Qn2
// Target Device:
// Tool versions:
// Description:
//
// Verilog Test Fixture created by ISE for module: q2
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////

module q2test;

    // Inputs
    reg a;
    reg b;
    reg c;
    reg d;

    // Outputs
    wire y_xor;
```

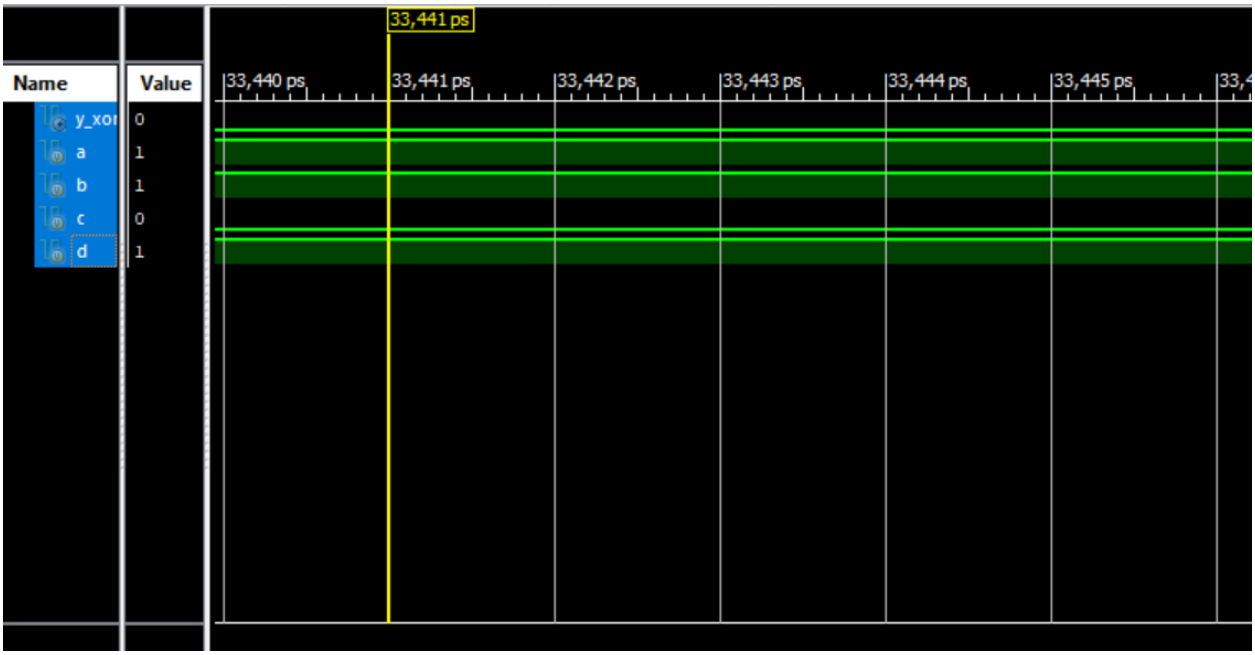
```
    q2  uut(
            .a(a),
            .b(b),
            .c(c),
            .d(d),
            .y_xor(y_xor)
    );

    initial begin

// Test sequence
  // Case 1: a=0, b=0, c=0, d=0
  #10 a = 0; b = 0; c = 0; d = 0;

  // Case 2: a=1, b=0, c=1, d=0
  #10 a = 1; b = 0; c = 1; d = 0;

  // Case 3: a=1, b=1, c=0, d=1
  #10 a = 1; b = 1; c = 0; d = 1;

            // Wait 100 ns for global reset to finish
            #100;

            // Add stimulus here

    end

endmodule
```

```
module q2test;
    // Inputs
    reg a;
    reg b;
    reg c;
    reg d;
    // Outputs
    wire y_xor;
    q2  uut(
        .a(a),
        .b(b),
        .c(c),
        .d(d),
        .y_xor(y_xor)
    );
    initial begin
    // Test sequence
     // Case 1: a=0, b=0, c=0, d=0
     #10 a = 0; b = 0; c = 0; d = 0;
     // Case 2: a=1, b=0, c=1, d=0
     #10 a = 1; b = 0; c = 1; d = 0;
     // Case 3: a=1, b=1, c=0, d=1
     #10 a = 1; b = 1; c = 0; d = 1;
       // Wait 100 ns for global reset to finish
       #100;
      end

endmodule
```

Simulations :







Task 3:

Simulate the gate level model of 4 to 1 Mux using Verilog (HDL).

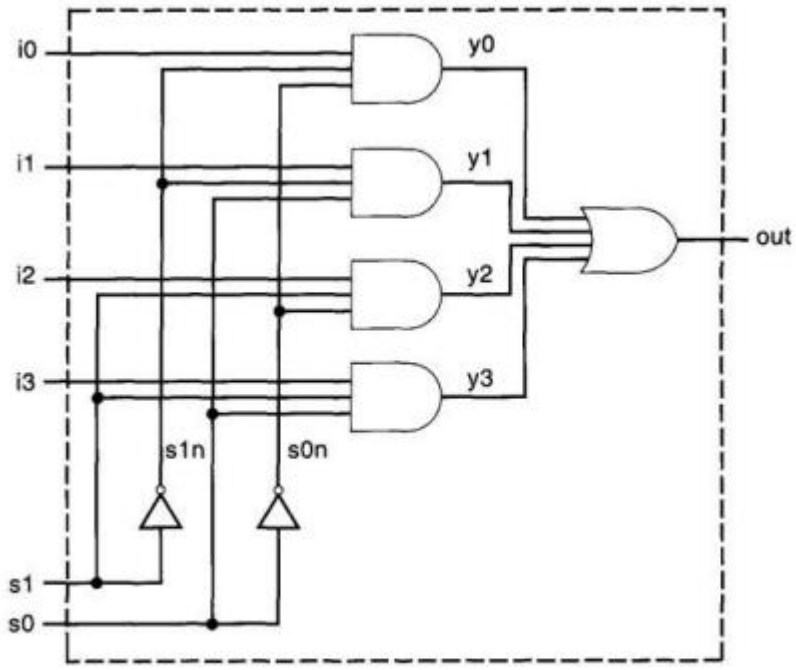


Figure 2: 4 x 1 Multiplexer

Code:

```
module q3 (
 input A,B,C,D,[1:0]S,
 output y
 );
wire w1,w2,w3,w4,n1,n2;
not x3(n1,S[0]);
not x2(n2,S[1]);
and a1(w1,A,n1,n2);
and a2(w2,B,S[0],n2);
and a3(w3,C,n1,S[1]);
and a4(w4,D,S[0],S[1]);
or o1(y,w1,w2,w3,w4);

endmodule
```

```
module q3 (
  input A,B,C,D,[1:0]S,
  output y
  );
wire w1,w2,w3,w4,n1,n2;
not x3(n1,S[0]);
not x2(n2,S[1]);
and a1(w1,A,n1,n2);
and a2(w2,B,S[0],n2);
and a3(w3,C,n1,S[1]);
and a4(w4,D,S[0],S[1]);
or o1(y,w1,w2,w3,w4);

endmodule
```

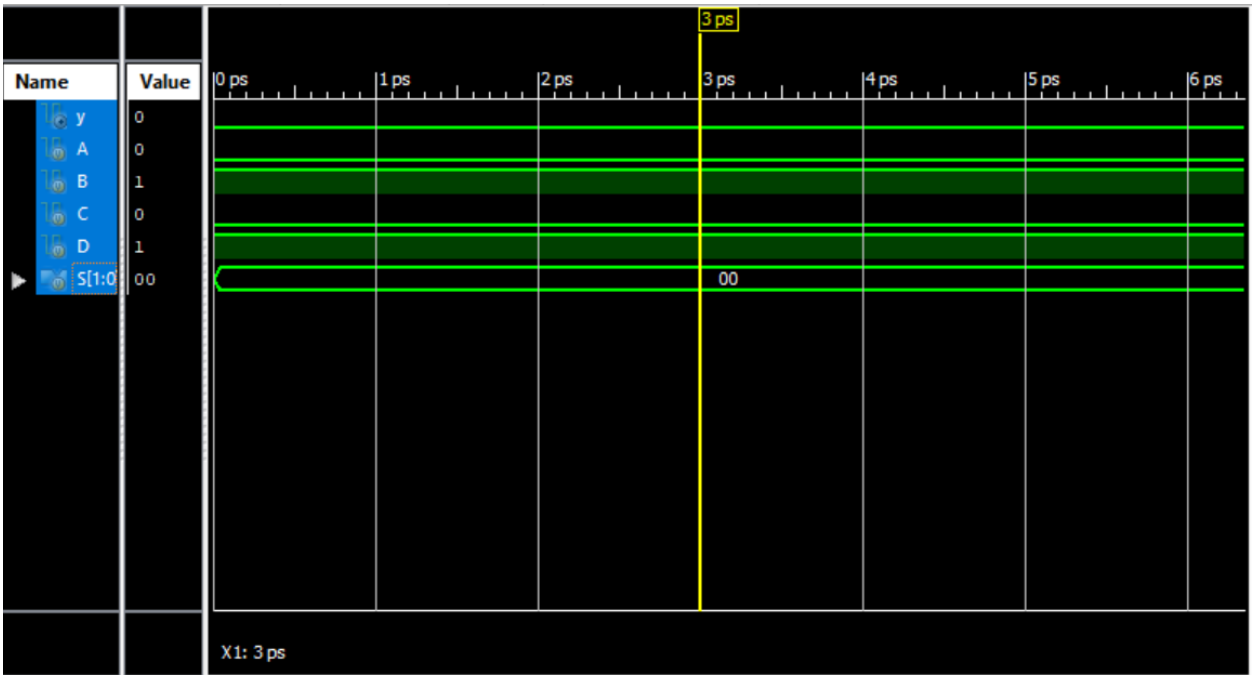
TestBench:

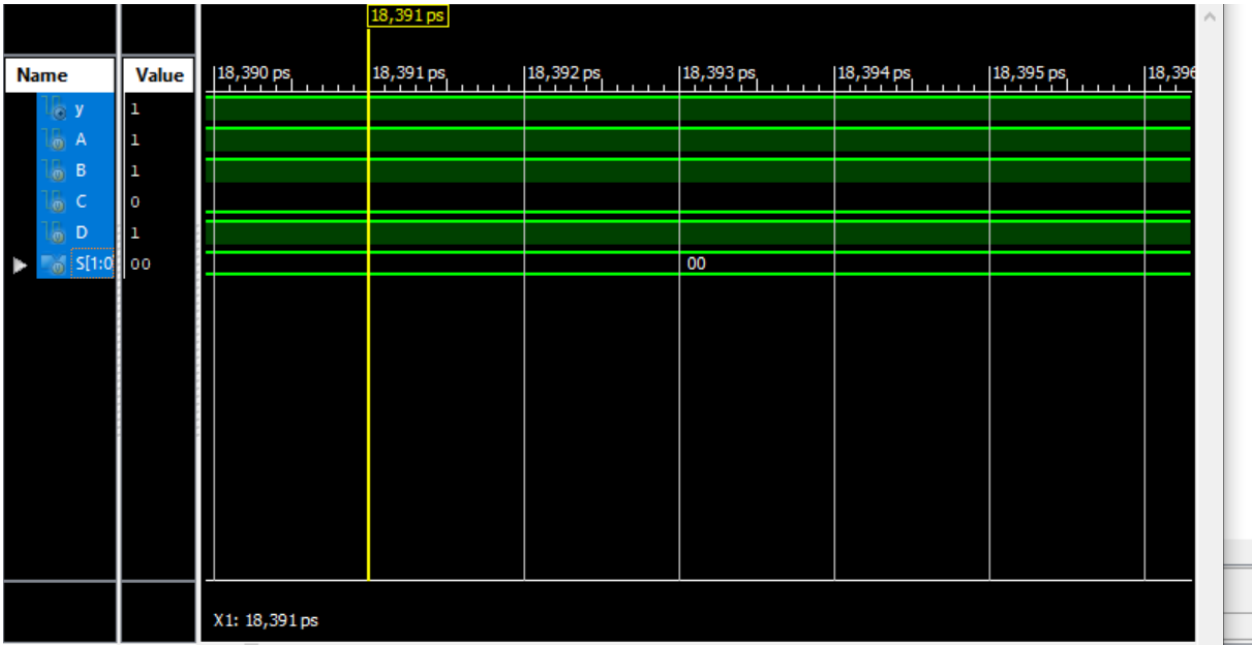
```
`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:   17:02:11 01/17/2024
// Design Name:   q3
// Module Name:   C:/Users/Ibrahim/Desktop/New folder/CP21_26_Lab2_q3/Q3test.v
// Project Name:  CP21_26_Lab2_q3
// Target Device:
// Tool versions:
// Description:
//
// Verilog Test Fixture created by ISE for module: q3
//
// Dependencies:
//
// Revision:
```

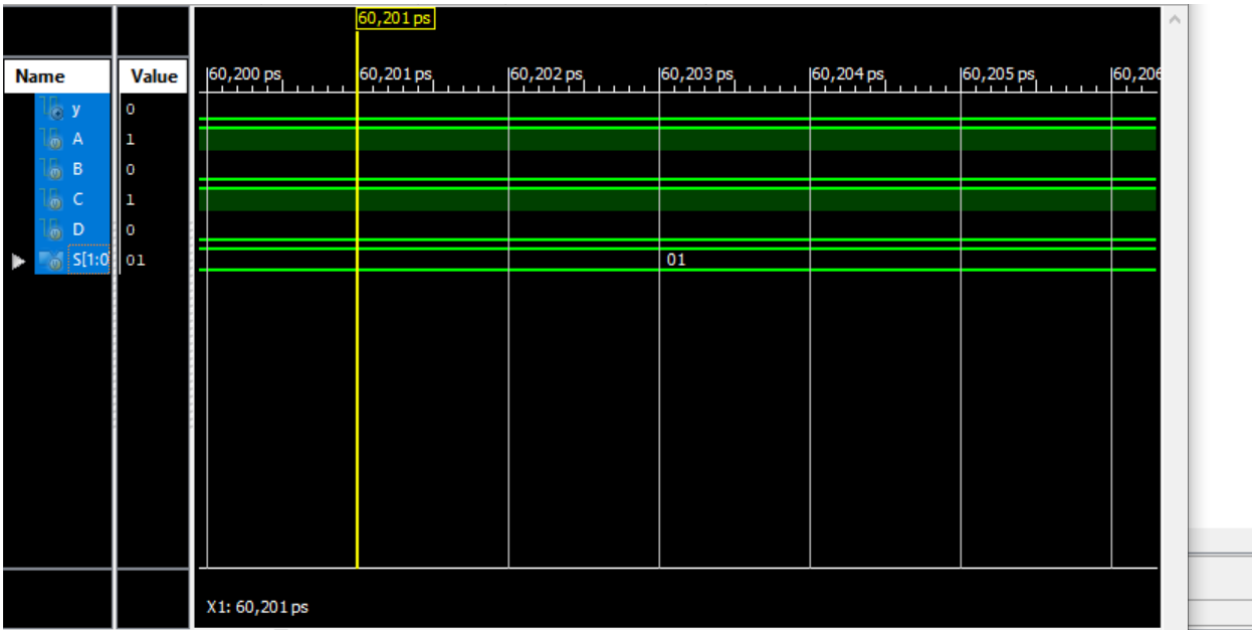
```
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module Q3test;
  // Inputs
  reg A, B, C, D;
  reg [1:0] S;
 // Output
  wire y;
  // Instantiate the module
  q3 uut (
    .A(A),
    .B(B),
    .C(C),
    .D(D),
    .S(S),
    .y(y)
  );
initial begin
  // Initialize inputs
  A = 0;
  B = 1;
  C = 0;
  D = 1;
  S = 2'b00;
  #10 A = 1;
  #10 B = 0;
  #10 C = 1;
  #10 D = 0;
  #10 S = 2'b01;
end
endmodule
```

```
module Q3test;
  // Inputs
  reg A, B, C, D;
  reg [1:0] S;
 // Output
  wire y;
  // Instantiate the module
  q3 uut (
    .A(A),
    .B(B),
    .C(C),
    .D(D),
    .S(S),
    .y(y)
  );
initial begin
  // Initialize inputs
  A = 0;
  B = 1;
  C = 0;
  D = 1;
  S = 2'b00;
  #10 A = 1;
  #10 B = 0;
  #10 C = 1;
  #10 D = 0;
  #10 S = 2'b01;
end
endmodule
```

Simulations :




18,391 ps
Name
Value
18,390 ps
18,391 ps
18,392 ps
18,393 ps
18,394 ps
18,395 ps
y
A
B
C
D
S[1:0
1
1
1
0
1
00
00
X1: 18,391 ps


60,201 ps
Name
Value
60,200 ps
60,201 ps
60,202 ps
60,203 ps
60,204 ps
60,205 ps
y
A
B
C
D
S[1:0
0
1
0
1
0
01
01
X1: 60,201 ps