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Project Title: **Stopwatch on Fpga**

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Project Report: Stopwatch Design Using Seven-Segment Displays on Nexys 4 FPGA

Introduction

This project involves the design and implementation of a stopwatch using Verilog for deployment on a Nexys 4 FPGA. The stopwatch is capable of displaying hours, minutes, seconds, and tenths of a second on four separate seven-segment displays. The implementation leverages a 100 MHz clock signal for precise timekeeping and incorporates functionalities such as start, stop, and reset, controlled via push buttons on the FPGA board. This report details the methodology, design considerations, and functionality of the stopwatch, ensuring efficient resource usage and smooth operation on the FPGA.

Design Methodology

The stopwatch design is modular, consisting of three main components: the top module, the stopwatch logic module, and the seven-segment display driver module. The top module integrates the other two modules and handles the input/output interface with the FPGA board. The stopwatch logic module manages the counting of time, including debouncing the start and stop buttons to ensure accurate control. The seven-segment display driver module handles the display of the time on the seven-segment displays, including the multiplexing of the displays to show different digits at appropriate intervals.

Stopwatch Logic Module

The stopwatch logic module is responsible for the core functionality of the stopwatch. It includes debouncing logic for the start and stop buttons, ensuring that button presses are accurately registered without noise. The module uses a 100 Hz clock signal derived from the 100 MHz system clock to drive the counters for tenths of seconds, seconds, minutes, and hours. Each counter wraps around appropriately (e.g., seconds from 59 to 0, tenths of seconds from 99 to 0) and increments the next higher counter. The module also includes logic to handle the start, stop, and reset operations, ensuring the stopwatch can pause and resume accurately.

Seven-Segment Display Driver

The seven-segment display driver module controls the visual representation of the stopwatch on the FPGA's seven-segment displays. It includes logic to multiplex the four displays, updating each display at a high enough frequency to appear continuous to the human eye. The module converts binary-coded decimal (BCD) values from the stopwatch logic into the appropriate segment patterns to display digits from 0 to 9. It also handles the decimal point placement, ensuring it appears only on the appropriate display.

Button Debouncing

Button debouncing is crucial to ensure that each button press is accurately registered without false triggers. The implementation uses a series of flip-flops to filter out noise and mechanical bounce from the buttons, providing stable input signals to the stopwatch control logic.

Clock Signal Generation

A clock divider is used to convert the 100 MHz input clock to a 100 Hz signal. This involves counting clock cycles and toggling an output signal every 500,000 cycles. The 100 Hz signal is then used to increment the time counters, ensuring precise timekeeping.

Binary to BCD Conversion

The stopwatch counters operate in binary, but seven-segment displays require BCD inputs. The conversion is done by simple arithmetic operations within the stop_watch module, dividing each counter value by 10 to obtain the tens digit and using the remainder as the ones digit.

Timing and Clock Management

A critical aspect of the design is the accurate management of timing and clock signals. The 100 MHz clock signal from the FPGA is used to generate a 100 Hz clock signal for driving the time counters. This is achieved through a clock divider, which counts the appropriate number of clock cycles to toggle the 100 Hz signal. This ensures that the stopwatch increments in tenths of a second, providing precise timekeeping. The design also includes considerations for minimizing clock skew and ensuring synchronous operation across the different modules.

Resource Utilization

The design is optimized for efficient resource usage on the Nexys 4 FPGA. By using a modular approach and efficient Verilog coding practices, the design minimizes the use of logic elements and other FPGA resources. The use of a clock divider reduces the need for additional clock management resources, while the multiplexing of the seven-segment displays allows for a reduction in the number of required I/O pins. This ensures that the design can run smoothly on the FPGA without exceeding resource limitations.

Testing and Verification

Thorough testing and verification are critical to ensure the accurate functionality of the stopwatch. The design was tested on the Nexys 4 FPGA board, verifying each functionality, including start, stop, reset, and the accurate display of time. Simulations were conducted to check the correctness of the debouncing logic, the timing of the counters, and the display driver. Edge cases, such as the wrap-around of the counters and simultaneous button presses, were also tested to ensure robust operation.

Future Work

Future enhancements could involve adding more features, such as lap time recording, interfacing with external displays, or even wireless communication for remote control and monitoring. Additionally, optimizing the design for lower power consumption and exploring alternative clock frequencies could be areas of further exploration. Expanding the stopwatch functionality to include countdown timers or integrating it with other FPGA-based systems could also provide valuable extensions to this project.

Conclusion

The design and implementation of a stopwatch using seven-segment displays on the Nexys 4 FPGA have been successfully completed. The project demonstrates the effective use of Verilog for FPGA programming, incorporating precise timing, efficient resource usage, and robust functionality. The stopwatch meets all specified requirements, including accurate timekeeping, clear display, and responsive control via push buttons. This project serves as a practical example of digital design and FPGA implementation, showcasing the capabilities of the Nexys 4 board in handling complex timekeeping and display tasks.

References

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- FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version by Pong P. Chu
- Digital Design and Computer Architecture by David Harris and Sarah Harris