A Fast-Transient Fully-Integrated Digital LDO with Current-Estimation Algorithm based Coarse Loop

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***Abstract*—In this brief, a fully-integrated output-capacitor-free (OCF) digital low-dropout regulator (DLDO) is proposed utilizing a current-estimation algorithm (CEA) based coarse loop controller to achieve fast voltage droop (V_{Droop}) recovery with improved line and load regulations. The proposed CEA-based controller quickly determines the target output switch-code by estimating the current-voltage ratio of power MOSFETs, enabling fast V_{Droop} recovery during load current (I_{LOAD}) transients. Complementing the CEA-based coarse loop, the proposed OCF-DLDO incorporates asynchronous and fine loops. The asynchronous loop supplies an instant dynamic current during I_{LOAD} transients, rapidly restoring the V_{OUT}, while the fine loop reduces output voltage ripples and quiescent current during steady-state of the DLDO. The proposed OCF-DLDO was fabricated in a 65-nm CMOS process with an active area of 0.075 mm^2. Measurement results demonstrate that the proposed DLDO operates with an input voltage range of 0.7 V – 1.2 V. It achieves a figure-of-merit as low as 0.383 ps when driving 26 mA of I_{LOAD} with a peak current efficiency of 99.4 %.**

***Index Terms*—Digital LDO, fast transient, current-estimation algorithm, output-capacitor-free,**

I. Introduction

LOW-dropout regulators (LDOs) are widely used in system-on-chips (SoCs) for efficient point-of-load (PoL) power delivery with fast transient response and small footprint [1]. Multiple LDOs can be integrated into SoCs without bulky passive components like inductors and capacitors in switching-mode regulators [2]. Digital versions of LDOs (DLDOs) have gained significant attention due to their design simplicity, scalability, and wide range of input (V_{DD}) and output voltages (V_{OUT}) while driving μA to sub-ampere load currents [3]. However, conventional DLDOs, as depicted in Fig. 1(a) utilizing a binary clocked comparator and an integral-controller based on bi-directional shift registers (SRs), rely on high clock frequency (F_{CLK}) for improved performance [1]–[3]. Yet, this high F_{CLK} incurs a large quiescent current (I_Q) which reduces the overall current and power efficiencies of a DLDO.

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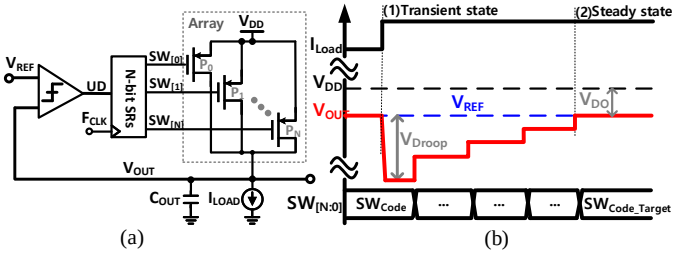


Fig. 1. Typical DLDO: (a) circuit diagram (b) load transient response.

Dual-feedback loop DLDOs [4]–[10] have effectively addressed the power-speed trade-off of a typical DLDO. In dual-loop DLDOs [4], [8], [10], [11], a high-gain coarse loop controller with a higher F_{CLK} is implemented to quickly reduce the large voltage error during transient-state. Conversely, a high-resolution fine loop controller with a slower F_{CLK} is implemented for the steady-state operation of a dual-loop DLDO to reduce the I_Q and voltage ripples V_{RIPP}. It indicates that, even in the coarse loop, F_{CLK} influences the transient response of dual-loop DLDOs [4], [8], [10], [11]. Fig. 1(b) illustrates the load transient waveforms of DLDOs [4], [5], [10] using typical SRs based digital controllers. These controllers recover the voltage droop (V_{Droop}) by adjusting their output codes ($SW_{[N:0]}$) at each rising edge of F_{CLK} until the target output code $SW_{Code[Target]}$ is achieved and V_{OUT} becomes equal to V_{REF}. This approach adjusts only one SW_{Code} per F_{CLK} period, resulting in prolonged recovery time (T_{REC}) of V_{Droop}. Notably, the T_{REC} of DLDOs [1], [4], [5], [10] increases with higher V_{Droop} at higher I_{LOAD} transients.

To address these shortcomings, we propose a current-estimation algorithm (CEA)-based controller for the coarse loop of the proposed DLDO. This CEA-based controller updates its output (SW_{Code}) by estimating the current-voltage ratio of power MOSFETs, enabling quick determination of the $SW_{Code[Target]}$ and significantly reducing the T_{REC} of V_{Droop}, even during large I_{LOAD} transients. The rest of the paper is organized as follows: Section II derives the relationship between the controller's $SW_{Code[Target]}$, I_{LOAD}, and the dropout voltage (V_{DO}) of the DLDO. Section III discusses the proposed CEA-based coarse loop and compares its performance with existing typical SRs controllers. The proposed output-capacitor-free (OCF) DLDO is presented in Section IV. Section V presents the measurement results, and Section VI concludes the paper.

II. Relationship Between Target SW_{Code} and I_{LOAD}

DLDOs commonly use unary-weighted PMOS transistor sizing due to its high resolution [1], [4], [5], [10]. Fig. 1(a)

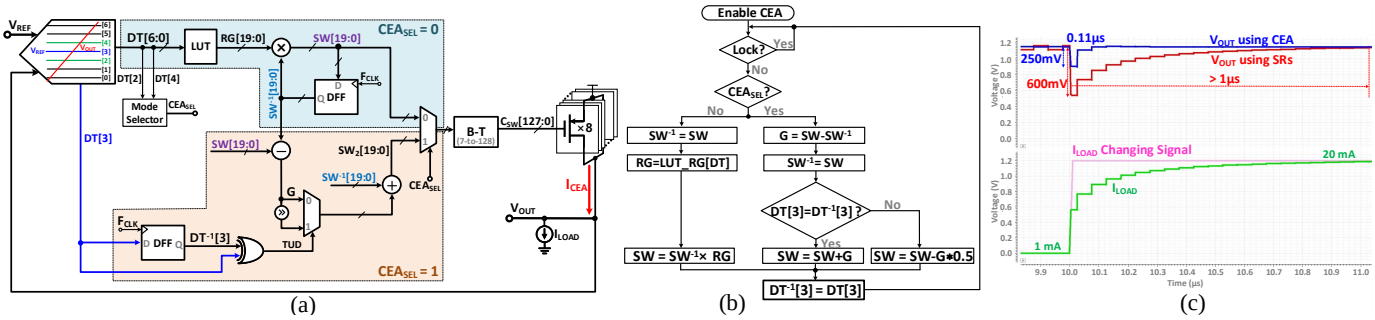


Fig. 2. Proposed CEA-based Coarse loop (a) simplified block diagram, (b) flow diagram, and (c) simulated load transient comparison using proposed CEA-based coarse loop and SRs loop.

shows a typical DLDO with a unary-weighted PMOS array. Here, the number of turned-on transistors depends on the switch code $SW_{[N:0]}$ of the SRs controller, determined within the feedback loop operation to achieve V_{OUT} = V_{REF} at a particular I_{LOAD}. PMOS transistors are turned-on in the deep-triode region and function as r_{ON} resistors, while turned-off transistors behave like open circuits [Fig. 1(a)]. The turned-on state of a PMOS in this switch array can be expressed as follows:

$$I_{PMOS} = \mu_p C_{ox} \frac{W_p}{L_p} (V_{SG} - |V_{thp}|) V_{SD} \tag{1}$$

Similarly, I_{LOAD} can be calculated from the number of turned-on PMOS transistors corresponding to the SW_{Code} value.

$$\begin{aligned} I_{LOAD} &= I_{PMOS} \times SW_{Code} \\ &= \mu_p C_{ox} \frac{W_p \times SW_{Code}}{L_p} (V_{SG} - |V_{thp}|) V_{SD} \\ &= k \times SW_{Code} \times V_{SD} \end{aligned} \tag{2}$$

Co-efficient (k) models the process parameters and voltage ($V_{SG} - |V_{thp}|$). V_{SD} indicates the voltage difference between V_{DD} and V_{OUT}, and it is called the dropout voltage (V_{DO}). During the load-transient state as shown in Fig. 1(b), V_{DO} becomes equivalent to V_{Droop} at a particular SW_{Code} and I_{Load}. Accordingly, eq. 2 for the load-transient state is given as:

$$I_{LOAD}(transient - state) = k \times SW_{Code} \times V_{Droop} \tag{3}$$

Similarly, in the DLDO's steady-state, V_{Droop} is fully recovered after multiple iterations of SW_{Code} [Fig. 1(b)] and V_{OUT} equals V_{REF} at the target $SW_{Code[Target]}$. It provides the steady-state current equation of DLDO.

$$I_{LOAD}(steady - state) = k \times SW_{Code} \times V_{DO} \tag{4}$$

Equating eq. 3 and eq. 4 provides the $SW_{Code[Target]}$ to achieve the steady-state of the DLDO.

$$SW_{Code[Target]} = \frac{SW_{Code} \times V_{Droop}}{V_{DO}} \tag{5}$$

Eq. 5 indicates that knowing the present SW_{Code} and V_{DO} enables an immediate estimation of the $SW_{Code[Target]}$ for the DLDO's the steady-state during I_{Load} transients. By deriving the eq. 5, we propose the CEA-based coarse loop, which promptly adjusts the V_{Droop} by estimating $SW_{Code[Target]}$. This leads to the significant reductions in V_{Droop} and T_{REC} during I_{Load} transients for the proposed OCF-DLDO.

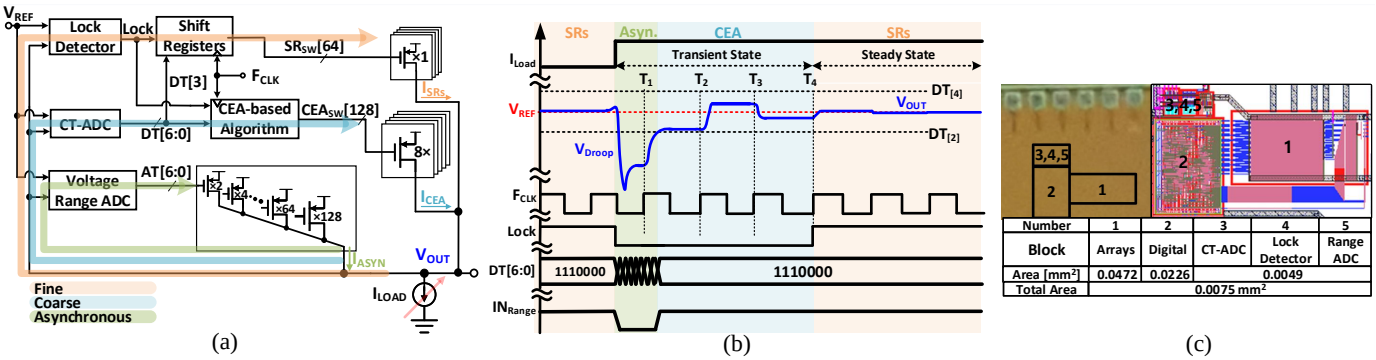
III. Proposed CEA-Based Coarse Loop

Fig. 2(a) shows the simplified block diagram of the proposed current-estimation algorithm (CEA)-based coarse loop implemented in the proposed OCF-DLDO. During start-up, the continuous-time ADC (CT-ADC) performs a non-uniform quantization and generates 7-thermometric bits DT[6:0]. Among these bits, DT[3] is considered at the V_{REF} level and changes its polarity when V_{OUT} is approximately equal to V_{REF}. DT[2] and DT[4] represent a voltage range ($V_{REF}\pm\Delta$) around the V_{REF}. Based on this voltage range, the operating mode of the proposed CEA is decided. The mode selector block generates the control signal CEA_{SEL} from DT[2] and DT[4] to select the operating mode of the CEA-based coarse loop. When the V_{OUT} is outside the voltage range $V_{REF}\pm\Delta$, CEA_{SEL} remains zero. However, when V_{OUT} enters the $V_{REF}\pm\Delta$ range, CEA_{SEL} changes its polarity from 0 to 1. CEA_{SEL} level determines which output bits of the two different operating modes of the CEA controller are used to control the PMOS transistors, as depicted in Fig. 2(a).

When CEA_{SEL} = 0, all DT[6:0] bits are passed to a look-up table (LUT) as shown in Fig. 2(a). The LUT generates the 20-bit binary-code RG[19:0]. These values are computed using the voltage difference ratio between V_{DD}, V_{OUT}, and V_{REF}, which can be expressed as follows:

$$RG[19:0] = \frac{V_{DD} - V_{OUT}}{V_{DD} - V_{REF}} \tag{6}$$

As a result, LUT continually generates RG[19:0] until the voltage differences in eq. 6($V_{DD} - V_{OUT}$ and ($V_{DD} - V_{REF}$) becomes equal. Subsequently, RG[19:0] is fed to a 20-bit multiplier, where the upper 7-bits represent the integer part, and the lower 13 bits represent the fractional part. The 7-bit integer part is then transformed into 128-bit thermometric code using a binary-to-thermometric (B-to-T) converter that controls the PMOS transistors and generates the current I_{CEA}. This current is adjusted to match I_{LOAD} for voltage regulation. When CEA_{SEL} = 0 and V_{OUT} is out-of $V_{REF}\pm\Delta$ range, the proposed CEA loop performs coarse-gain variations within one F_{CLK} cycle, to rapidly bring V_{OUT} within $V_{REF}\pm\Delta$ range, thus reducing the transient time. Contrarily, when V_{OUT} approaches the $V_{REF}\pm\Delta$ range CEA_{SEL} switches from low to high, the proposed CEA loop initiates its fine-gain iterations to precisely match V_{OUT} with V_{REF}. This reduces V_{OUT} fluctuations and achieves fine load regulation. The fine-gain variations start with the mid-bit DT[3] of DT[6:0], which is delayed by one



(a) (b) (c)

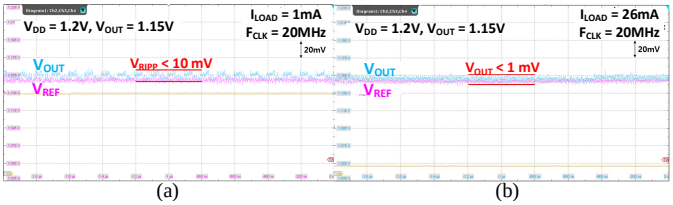
Fig. 3. Proposed OCF-DLDO (a) block diagram and (b) operating waveforms (c) die micrograph and layout.

F_{CLK} cycle and then compared with DT^{-1}[3]. If DT[3] and DT^{-1}[3] are different, and TUD = 1, the gain (G) of the CEA is reduced to half of the current gain to achieve fine regulation. The feedback-loop continues iterating and reducing the gain (G) by half in each F_{CLK} cycle until DT[3] and DT^{-1}[3] becomes equal, and the gain (G) of CEA is fixed. The overall operation of the proposed CEA based coarse loop is depicted in a flow diagram in Fig. 2(b). In Fig. 2(b), $Lock$ indicates the enabling of the CEA coarse loop of the DLDO, which is described in detail in Sec. IV.

Fig. 2(c) compares the load transient response of the proposed CEA-based coarse loop with SRs-based loop at V_{OUT} = 1.15 V, F_{CLK} = 20 MHz, and ΔI_{LOAD} = 19 mA. The proposed CEA-based loop demonstrates a V_{Droop} of 250 mV and recovers it within T_{REC} = 0.11 μs, while the SRs-based loop experiences a larger V_{Droop} of 600 mV and T_{REC} of more than 1 μs.

IV. Proposed Fast-Transient OCF-DLDO

Fig. 3(a) shows the detailed block diagram of the proposed OCF-DLDO. The OCF-DLDO consists of three loops: two synchronous (F_{CLK} operated) loops and one asynchronous (clock-less) loop. The asynchronous loop functions as a fast proportional (P-control) system, providing instant dynamic current I_{ASYN} similar to an output capacitor (C_{OUT}). It effectively suppresses V_{Droop} during load current transients. The loop is realized by directly connecting a 7-bit V_{OUT} range detector ADC to a binary-weighted PMOS array, as shown in Fig. 3(a). The V_{OUT} range detector ADC compares V_{OUT} with seven predefined voltage ranges centered around V_{REF}, spanning 30–200 mV. When V_{OUT} is sufficiently close to V_{REF} (*i.e.,* <30 mV) during the DLDO's steady-state, all thermometric bits AT[6:0] become high, turning-off the binary-weighted power transistors. The asynchronous loop has been previously proposed in our tri-loop DLDO [12], and its operation principle and design considerations are detailed there. The proposed coarse loop consists of a continuous-time ADC (CT-ADC), a current-estimation algorithm (CEA)-based controller, and a 128-bit unary-weighted PMOS array, as shown in Fig. 3(a). The CT-ADC employs seven logic-threshold-triggered comparators (LTTC) to perform non-uniform quantization. It generates skewed-threshold voltage levels in each LTTC and produces 7-thermometric bits (DT[6:0]) [12]. The employed CT-ADC ensures high steady-state accuracy of the proposed OCF-DLDO without compromising its speed during transient states.



(a) (b)

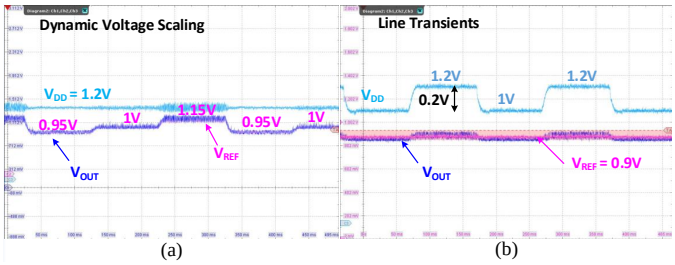
Fig. 4. Oscilloscope captures of V_{RIPP} of the OCF-DLDO at (a) I_{LOAD} = 1 mA and (b) I_{LOAD} = 26 mA.

The CEA controller, based on DT[6:0], adaptively estimates the coarse loop current (I_{CEA}) to match to the load current I_{LOAD}. During start-up or load transient states, if the voltage difference between V_{OUT} and V_{REF} increases, the proposed CEA-based controller turns-on/off a larger number of PMOS transistors within a F_{CLK} cycle. Conversely, as the voltage difference decreases, the CEA-based controller performs fine-regulation by halving the number of turned-on/off transistors in each F_{CLK} cycle until $V_{OUT} \approx V_{REF}$. The fine loop consists of a typical shift-registers (SRs) based controller and a small-sized unary-weighted PMOS array. It operates during the steady-state of the DLDO to reduce steady-state voltage ripples (V_{RIPP}) and quiescent current (I_Q).

The switching between the coarse and fine loops is determined by the "$Lock$" signal generated by a lock detector as shown in Fig. 3(a). When V_{OUT} reaches within the predefined lock range ($\approx$ 10 mV) of the lock detector, $Lock$ signal toggles from 0 to 1, transitioning the loop from coarse to fine. The switching process is further illustrated in Fig. 3(b). As shown, during a load-transient state (when I_{LOAD} steps-up), the asynchronous loop rapidly supplies I_{ASYN} to compensate for V_{Droop} before the synchronous CEA-based coarse loop responds. At the next rising of $F_{CLK}(T_1)$, the CEA-based controller recovers the V_{Droop} upto IN_{Range} ($DT_{[2]}$ - $DT_{[4]}$), substantially reducing the voltage difference between V_{OUT} and V_{REF}. At T_2 and T_3, the CEA-based controller further reduces the voltage difference using fine current estimations, as discussed in Sec. III. Once, V_{OUT} enters the predefined lock range of lock detector, $Lock$ switches high, freezing the coarse loop and triggering the fine loop to reduce V_{RIPP} and I_Q.

V. Measurement Results

The proposed output-capacitor-free DLDO (OCF-DLDO) was designed in a 65-nm CMOS process and occupies an active area of 0.075 mm^2, as shown in Fig. 3(c). It generates V_{OUT} from 0.65 – 1.15 V using V_{DD} of 0.7 – 1.2 V, and supplies



(a) (b)

Fig. 5. Oscilloscope captures of (a) dynamic voltage scaling and (b) line transient performance of the OCF-DLDO.

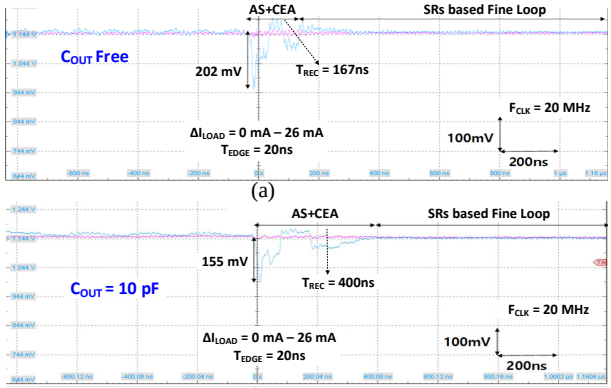


Fig. 6. Oscilloscope captures showing the load transient performance of the proposed DLDO at (a) C_{OUT} = 0 and (b) C_{OUT} = 10 pF.

an I_{LOAD} of 1 mA to 26 mA. V_{RIPP} performance of the proposed OCF-DLDO is shown in Fig. 4 for minimum and maximum I_{LOAD} at V_{OUT} = 1.15 V. The OCF-DLDO exhibits 10 mV and 1 mV of V_{RIPP} at I_{LOAD} of 1 mA and 26 mA, respectively. Fig. 5(a) shows the dynamic voltage scaling (DVS) accuracy of the proposed OCF-DLDO at V_{DD} = 1.2 V and I_{LOAD} = 1 mA. It accurately tracks the fast-changing V_{REF} from 0.95 V to 1.15. Line transient performance of the proposed OCF-DLDO is shown in Fig. 5(b), when the V_{DD} is switched between 1.0 V to 1.2 V at V_{REF} = 0.9 V and I_{LOAD} = 1 mA. The proposed OCF-DLDO achieves a line regulation of 0.05 mV/mV.

Fig. 6 shows measured load transient responses of the proposed DLDO, comparing cases with and without C_{OUT} (C_{OUT} = 0 and C_{OUT} = 10 pF). These measurements were taken by switching the I_{LOAD} from 0 mA to 26 mA (ΔI_{LOAD} = 26 mA) with T_{EDGE} = 20 ns at V_{OUT} = 1.15 V, V_{DD} = 1.2 V, and F_{CLK} = 20 MHz. As shown in Fig. 6(a), even without C_{OUT} (*i.e.,* C_{OUT} = 0), the proposed DLDO shows reduced V_{Droop} of 202 mV due to an instant dynamic current supply of asynchronous loop. Then the proposed CEA based coarse loop recovers this V_{Droop} within 200 ns of T_{REC}. Adding C_{OUT} = 10 pF [Fig. 6(b)] reduces V_{Droop} to 155 mV for the same load current (*i.e.,*ΔI_{LOAD} = 26 mA), and it is fully recovered in T_{REC} = 400 ns.

Table I summarizes the proposed OCF-DLDO performance and its comparison with state-of-the-art DLDOs. The proposed OCF-DLDO outperforms its counterparts with faster T_{REC}, efficient load regulation, and lower figure-of-merit (FOM).

VI. Conclusion

An output-capacitor-free DLDO with mitigated voltage droop (V_{Droop}) and fast-transient response is presented. The proposed current-estimation algorithm (CEA) based coarse loop enables fast V_{Droop} recovery during load current transients by quickly estimating the target switch code to activate exact number of PMOS transistors for load regulation. Fabricated DLDO in a 65-nm CMOS achieved a minimum FOM of 0.383 ps with peak current efficiency of 99.4 %.

TABLE I
Performance Summary and Comparison

	This Work	[4]	[5]	[6]	[8]	[9]
Process [nm]	65	65	130	130	65	65
Topology	AS+CEA	SRs	SRs	PID	VCO	SRs
V_{DD} [V]	0.7–1.2	0.6–1.2	0.5–1.2	0.5–1.22	0.9–1.2	0.6–1.0
V_{OUT} [V]	0.65–1.15	0.4–1.1	0.45–1.14	0.35–1.17	0.5–1.1	0.55–0.95
$I_{LOAD,\,MAX}$ [mA]	26	100	4.6	145	19	4.5
C_{OUT} [nF]	0–0.01	1	1	1.5	0.2	1
ΔV_{OUT} [mV] @ ΔI_{LOAD} [mA]	155@26*	55@98	90@1.4	280@40	80@3	118@4.4
T_{REC} [ns] @ ΔV_{OUT} [mV]	<400@155*	700@55	1100@90	55@280	90@80	5900@118
ΔI_{LOAD} T_{EDGE} [ns]	20	20	N/A	0.1	5	N/A
Load Reg [mV/mA]	0.04	0.06	<10	N/A	0.15	0.422
I_Q [µA]	167	82	751	3200	131	10.2
Current Eff. [%]	99.4	99.92	98.30	97.8	99.3	99.7
FOM_1 [ps]	0.383	0.43	34500	63.9	342	62.2
Area [mm^2]	0.075	0.01	0.114	0.18	0.059	0.09

*Measurements are performed using C_{OUT} = 0.01 nF. N/A = Not Addressed.

$$FOM_1 = \frac{C_{OUT} \times \Delta V_{OUT}}{\Delta I_{LOAD}} \times \frac{I_Q}{\Delta I_{LOAD}}$$

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