FAST-NUCES, Peshawar

Department of Computer Science

Spring 2020

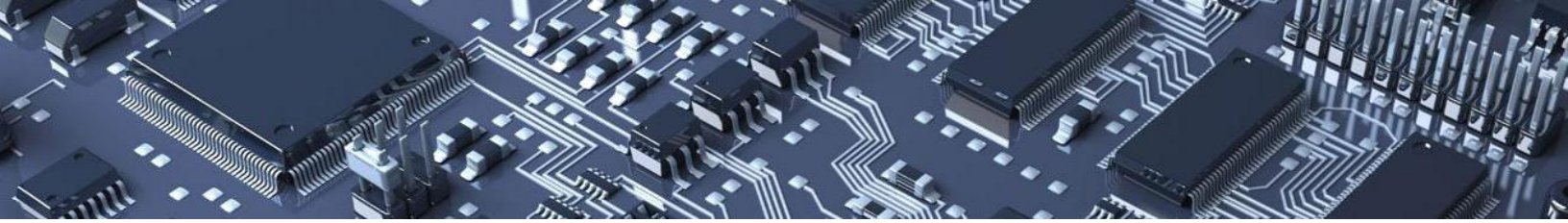
Lab Instructor: Muhammad Yousaf

Sequential Digital Design

Laboratory Manual

Asynchronous Logic Design

Using Latches



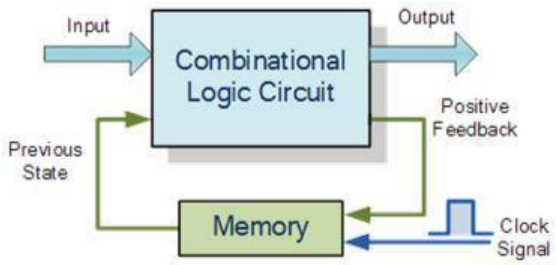
Objectives

- To become familiar with sequential logic circuits.
- To differentiate between synchronous and asynchronous logic circuits.
- To become familiar with latches.
- To implement and observe the operation of different latches.
- To become familiar with latches' timing diagrams.

Theoretical Background

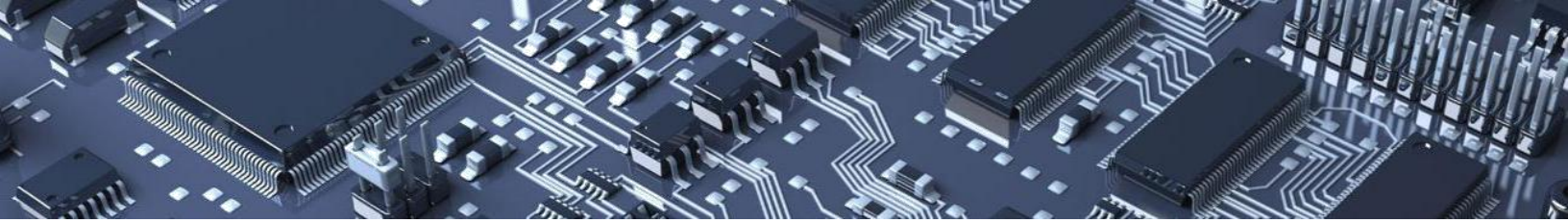
Sequential Circuits:

Digital electronics is classified into combinational logic and sequential logic. Combinational logic output depends on the inputs levels, whereas sequential logic output depends on stored levels and also the input levels.



The memory elements are devices capable of storing binary information. The binary information stored in the memory elements at any given time defines the state of the sequential circuit. The input and the present state of the memory element determine the output. Memory elements next state is also a function of external inputs and present state. A sequential circuit is specified by a time sequence of inputs, outputs, and internal states. Examples of sequential circuits are latches, flip flops, counters, registers, and time state generators.

So, combinatorial circuits are ones whose outputs depend on the current input state. When inputs change, the outputs do not depend on the previous inputs. Sequential circuits are similar, but they do also rely on previous input states. It can be inferred that they have memory.



There are two types of sequential circuits. Their classification depends on the timing of their signals:

- Synchronous sequential circuits
- Asynchronous sequential circuits

Synchronization is achieved by a timing device called a clock pulse generator. Clock pulses are distributed throughout the system in such a way that the memory elements are affected only with the arrival of the synchronization pulse. Synchronous sequential circuits that use clock pulses in the inputs are called **clocked-sequential circuits**. They are stable and their timing can easily be broken down into independent discrete steps, each of which is considered separately.

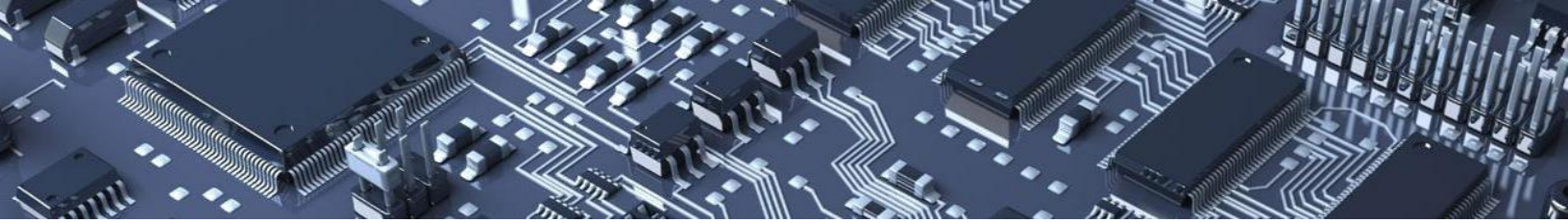
Synchronous:

The same clock signal is applied to each memory element, and changes in state occur when the clock changes state from one level to another (edge triggered).

Asynchronous:

Asynchronous sequential logic is not synchronized by a clock signal; the outputs of the circuit change directly in response to changes in inputs. The advantage of asynchronous logic is that it can be faster than synchronous logic, because the circuit doesn't have to wait for a clock signal to process inputs.

Synchronous Sequential Circuit	Asynchronous Sequential Circuit
Easy to design	Difficult to design
Clocked flip flop act as memory element	Unclocked latch or time delay act as memory element
Slower	Faster as clock is not present
The status of memory element is affected only at the active edge of clock, if input is changed.	The status of the memory element will change any time as soon as input is changed.



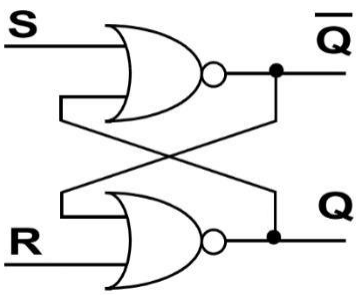
Latches:

The latch is a level sensitive circuit that will change its output state due to a change of states on its inputs. As a result, the latch is an asynchronous device.

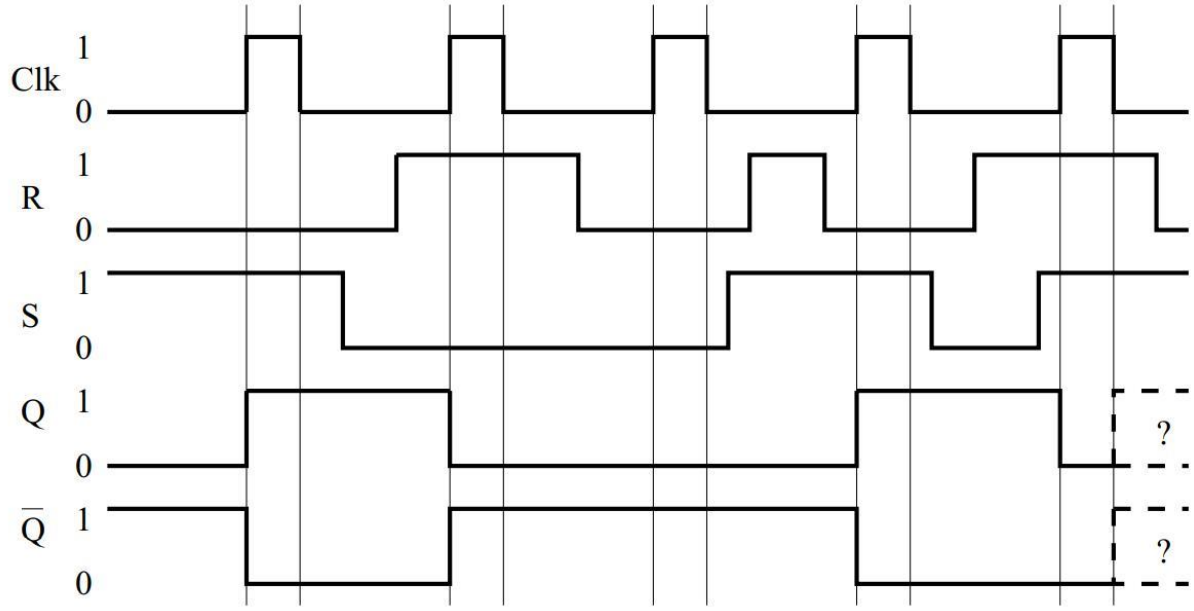
Set-Reset Latch (SR latch)

The SR latch is a circuit with two cross-coupled NOR gates or two cross-coupled NAND gates, and two inputs labeled S for set and R for reset.

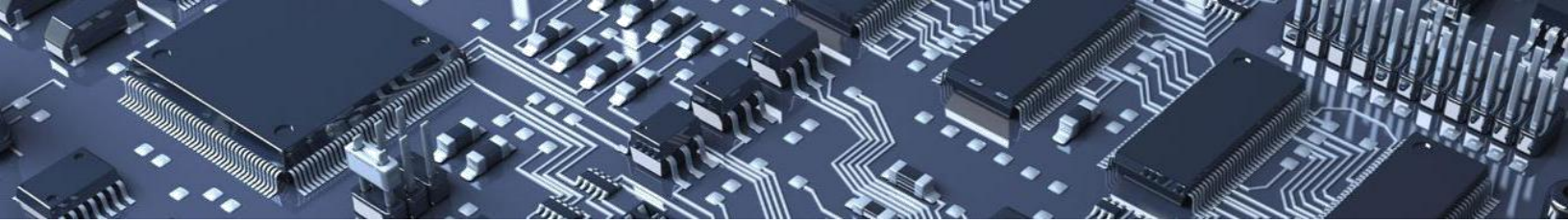
Active High SR Latch



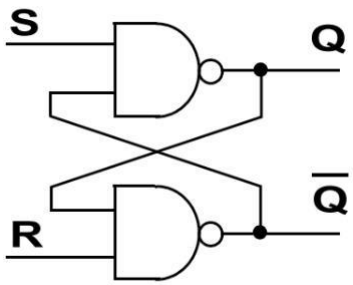
Set (S)	Reset (R)	Q	Q'
0	0	Q	Q'
0	1	0	1
1	0	1	0
1	1	0 (undefined)	0 (undefined)



Active High SR Latch Timing Diagram



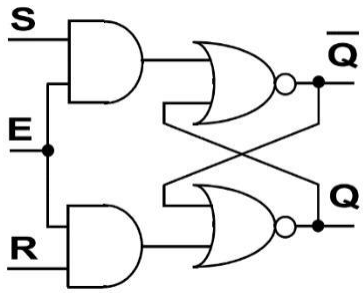
Active Low SR Latch



Set (S)	Reset (R)	Q	Q'
0	0	1 (undefined)	1 (undefined)
0	1	1	0
1	0	0	1
1	1	Q	Q'

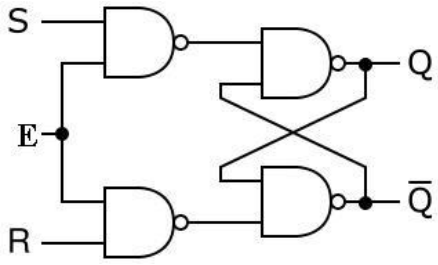
Enabled Set-Reset (SR) Latch (Gated Latch)

Active High Enabled SR latch

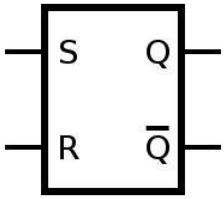


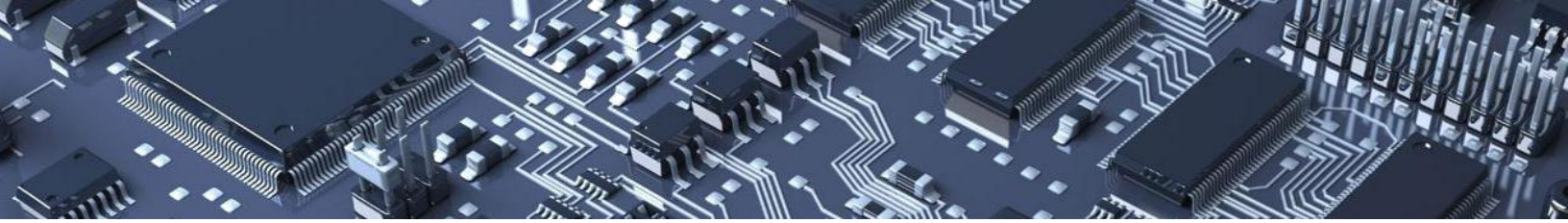
E	Set (S)	Reset (R)	Q	Q'
0	x	x	Q	Q'
1	0	0	Q	Q'
1	0	1	0	1
1	1	0	1	0
1	1	1	0 (undefined)	0 (undefined)

The following circuit is also a high active enabled SR latch.



The symbol of SR latch is shown in the following figure.

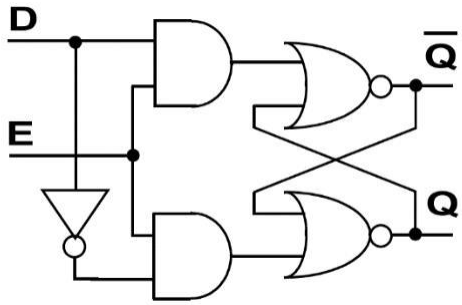




Data Latch (D latch)

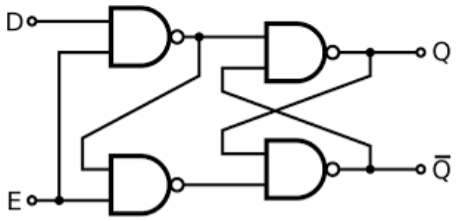
Another gated latch is the gated D latch. It can be obtained from a gated S-R latch by connecting S to D and R to D′.

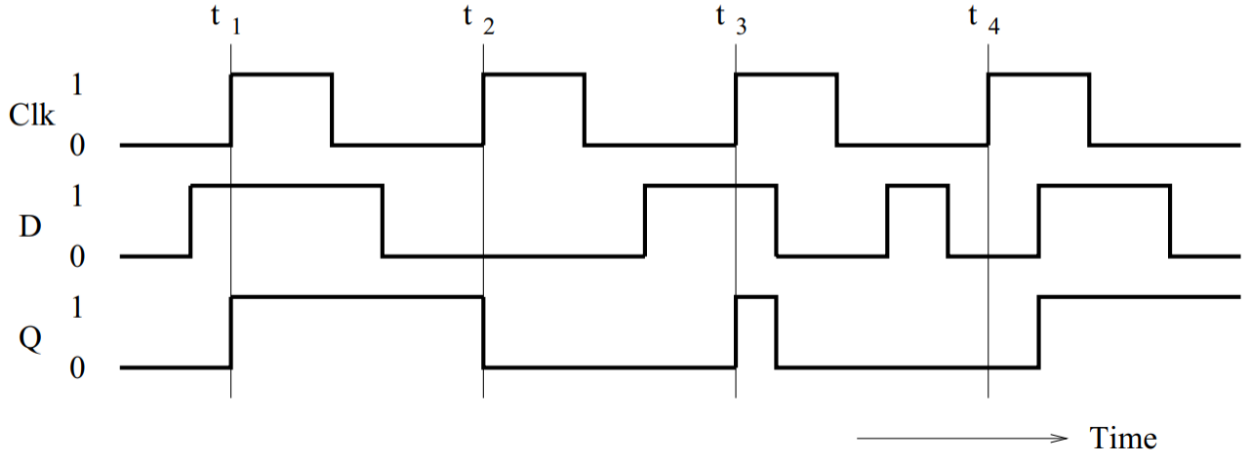
Active High Enable



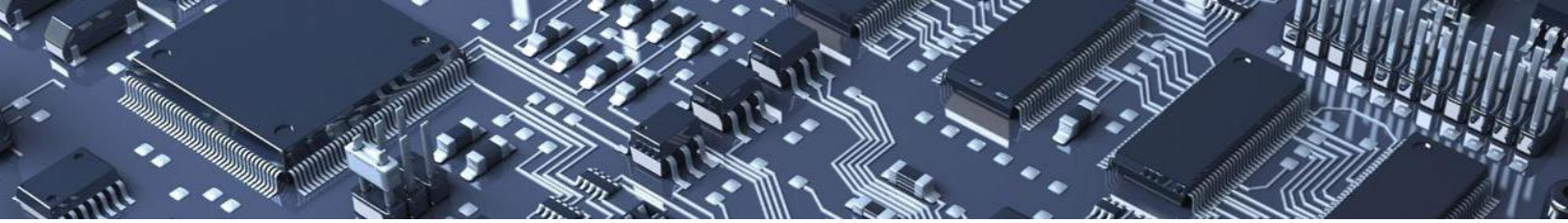
E	Data (D)	Q
0	x	Q
1	0	0
1	1	1

Which is the same as the following circuit

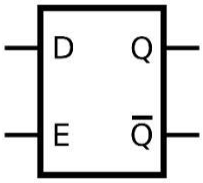




D Latch Timing Diagram



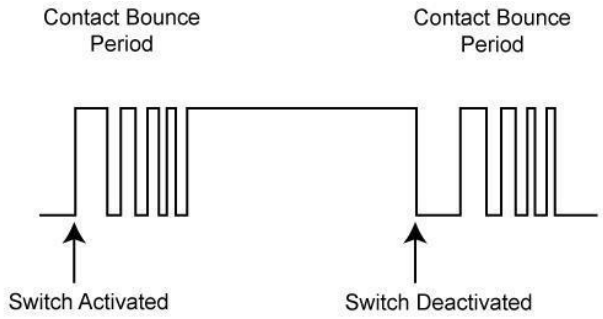
The symbol of D latch is shown in the following figure.



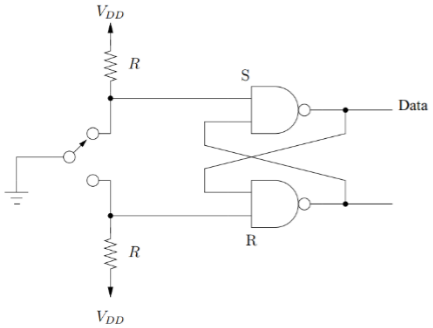
Latch Applications

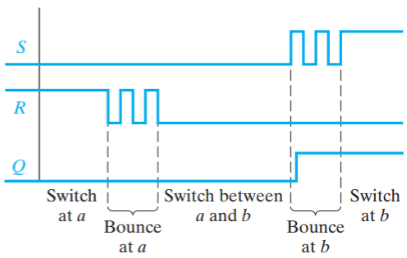
SR Latch Debouncing Circuit

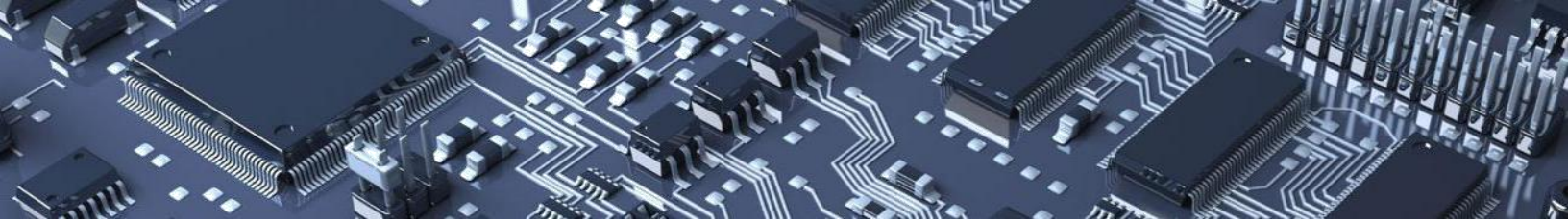
What is switch bounce? When you push a button, press a micro switch or flip a toggle switch, two metal parts come together. For the user, it might seem that the contact is made instantly. That is not quite correct. Inside the switch there are moving parts. When you push the switch, it initially makes contact with the other metal part, but just in a brief split of a microsecond. Then it makes contact a little longer, and then again, a little longer. In the end the switch is fully closed. The switch is bouncing between in-contact, and not in-contact. "When the switch is closed, the two contacts actually separate and reconnect, typically 10 to 100 times over a period of about 1ms."



Solution:





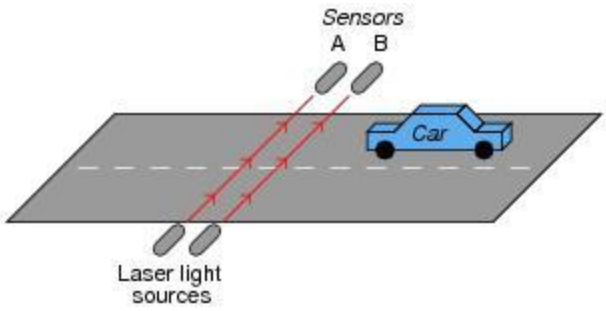


Hardware debouncing technique uses an S-R latch to avoid bounces in the circuit. S-R circuit is most effective of all debouncing approaches. The figure below is a simple debouncing circuit which is often used.

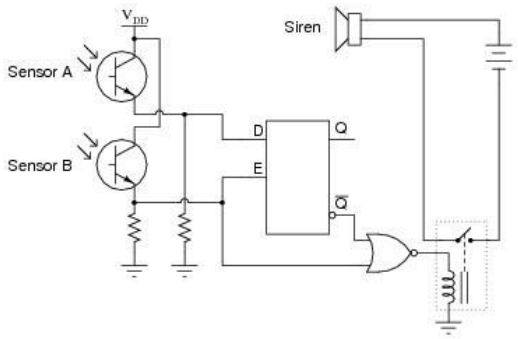
Wrong Way Detector using D Latch

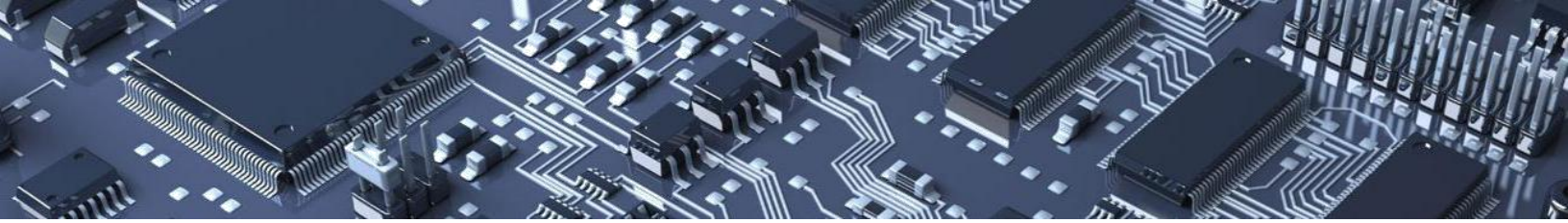
A one-way street is needed to be equipped with an alarm to signal drivers going the wrong way. The sensors work by light beams being broken when an automobile passes between them. The distance between the sensors is less than the length of a normal car, which means as a car passes by, first one beam is broken, then both beams become broken, then only the last beam is broken, then neither beam is broken. The sensors are phototransistors sensitive only to the narrow spectrum of light emitted by the laser light sources, so that ambient sunlight will not “fool” them.

Design an asynchronous sequential logic circuit that applies the specified system.



Solution:





Question

Draw the timing diagram for the previous circuit. Show the signal for D, E, Q, Q' and the output of the NOR gate.

Lab Tasks:

Equipment's required:

- Circuit Wizard Simulation Software.
- KL-31001 trainer kit.
- IC 7404(NOT), IC 7408(AND), IC 7432(OR), IC 7400(NAND), IC 7402(NOR).
- Connecting wires and Breadboard.
- The Datasheets of the IC's.

Implementation

Use Circuit Wizard to design, test and simulate the required circuits, then implement the circuits practically in the laboratory.

1. Active high SR latch using NOR.
2. Active low SR using NAND.
3. Enabled AND-NOR SR Latch.
4. Enabled NAND SR latch.
5. D latch.
6. Wrong Way Detector.

Good Luck