National University

of Computer & Emerging Sciences Peshawar Campus

Name: _____ Roll No: _____

Program: BS (CS)
Semester: Spring – 2020
Time Allowed: 45 minutes
Course: Computer Logic Design (EL227)

Examination: Mock Lab Exam
Total Weight: 5
Date: 23rd July, 2020
Lab Instructor: Muhammad Yousaf

Note: There are a total of nine questions (1 - 9) and you need to solve *only one* of the following. Each student will be solving different question from others using simple trick.

How to Choose Question: Figure out last digit of your Roll No and only solve that question, i.e.

Roll No: p190005 => Last Digit = **5**, so this student will solve **Q#5** only.
Roll No: p190038 => Last Digit = **8**, so this student will solve **Q#8** only.

Instructions:

- Only Handwritten Solution on copy/paper/register is acceptable.
- There is no need of any tool/Logically software for today's exam.
- Late submissions on gmail/slack will be highly discouraged. Please don't embarrass me by making any kind excuses.

Submission: Upload Pics/Scan images of your handwritten solution on slate only.

Q1. Given this function, you need to implement it using NAND gates only.

$$F = wxy + wyz + xyz + xyz' + wxyz$$

- Draw the truth table from this function?
- Implement its circuit diagram using NAND gates only?
- Simplify it using K-map?

Q2. Implement the following function using $\sum$**m (1, 3, 4, 6)** Decoders. First construct the Boolean function from given sum-of-minterms.

Q3. Use the Karnaugh map below to find a minimum ***product-of-sums*** expression for $\sum$**m(0,1,9,13,15)** . Make full use of these don't care conditions $\sum$**d(3,4,5,6,8)** for simplification. Also draw the circuit diagram of ***simplified expression*** using NAND gates only.

Q4. Implement a 6-bit binary subtractor, i.e. subtracting (**B_5 B_4 B_3 B_2 B_1 B_0**) from (**A_5 A_4 A_3 A_2 A_1 A_0**) using **Block** diagram.
Required Item:

1. 7483 (4 bit adder)
2. 7486 (XOR gate)
3. 7404 (NOT gate)

Hint:

- Basic concept of subtraction: A-B = A + (2's Complement of B)
- A 6-bit adder may be implemented by two 4-bit adders.

Q5. Implement the following;

- Full Adder circuit with NAND gates only.
- Half subtractor circuit with NOR gates only.

Q6. Implement the following function using $\sum\mathbf{m(0,3,5,6)}$ Multiplexers. First construct the Boolean function from given sum-of-minterms.

Q7. Given this function, you need to implement it using NAND gates only.

$$\boldsymbol{F = (w + x + y)\,.\,(x + y + z).\,(x + y + z').\,(w + x + y + z)}$$

- Draw the truth table from this function?
- Implement its circuit diagram using NOR gates only?
- Simplify it using K-map?

Q8. Implement Asynchronous counter using any kind of Flip Flops. Must show the K-map simplification from its truth table.

Q9. Implement 1:8 De-Mux using two 1:4 De-Muxes with truth tables and circuit diagrams using NAND gates only.