

LAYER-STACK Sym N° Mils MM Qty Plated

01-16 + 1 18 0.46 3 YES

× 2 25 0.64 2 NOT

□ 3 39 1.00 34 YES

• 4 102 2.60 4 NOT

x 5 125 3.18 2 NOT

- 1. This drawing is CAD generated. No manual changes authorized after release.
- 2. All printed wiring boards to be manufactured in accordance with IPC-610 Class 2.

  In case of conflict this drawing governs all other specifications.
- 3. Material, copper sheet laminate, copper clad FR4 170Tg. Interior layers (if applicable) to be 0.5oz copper. Exterior layers to be 1oz copper finished. Final thickness to be 0.063" (1.6mm).
- 4. All holes are plated through holes unless noted otherwise. Minimum plated through holes to have 25um thick walls.
- 5. All finished trace widths to be +/- 20% measured at the bottom, minimum finished spacing to be 100um.
- 6. All exposed copper to be finished with ENIG Solder finish over clean bare copper.
- 7. Drill boards using drill data, drill patterns, and drill table provided. Hole locations shall be 0.003" (0.075mm) about true position (radial error). All finished holes to be +/-0.003" (0.075mm) diameter unless noted otherwise. All finished vias to be +/-0.003" (0.075mm) to closed diameter.
- 8. Minimum annular ring to be 50um external layers and 25um internal layers (if applicable).
- 9. Layer to layer misalignment shall not exceed 75um (radial error) about true position.
- 10. Solder mask construction to be SMOBC using green LPI solder mask material. Solder mask to be 18 ~ 50um thick after curing, both sides.
- 11. Solder mask misalignment shall not exceed 0.003" (0.075mm). Solder mask may overlap through hole solder pads by 0.001" (0.025mm) maximum, but shall not overlap SMT pads.
- 12. Silkscreen should be applied over solder mask using a white epoxy-based ink. The silkscreen should not overlap solder pads unless noted otherwise.
- 13. Dimensions shown reflect the board size after plating.
- 14. The circuit board manufacturer shall apply a name and date code on the bottom side of the board in copper etch.