Enhanced Digital Discriminator

- Future possible FPGA-based algorithms for EDD:
  - NSOT (number of samples over threshold)
  - v-NSOT (one sample over one threshold , next one over another)
  - Area
  - Digital filtering

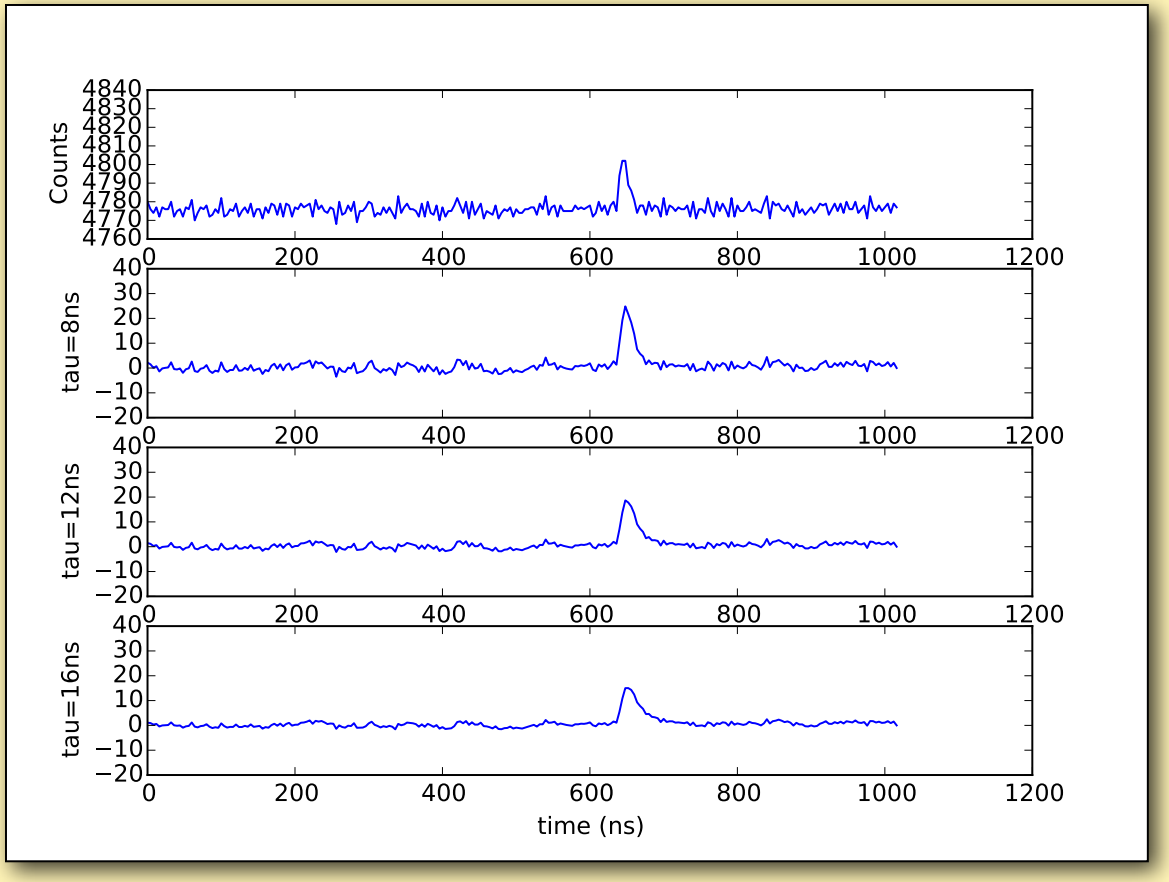
Digital Filtering

- Infinite Impulse Response (IIR)
  - Use a sum of current and N earlier digitizations to arrive at new filtered waveform
    - N = 1 here: First order
  - Advantages & Disadvantages:
    - Advantages: fast, simple, easy to implement
    - Disadvantages: can be unstable
- Finite Impulse Response (FIR)
  - Convolve current waveform with template (noise-free) waveform
  - Advantages and Disadvantages
    - Advantages: stable
    - Disadvantages: slow, harder to implement

IIR

- Algorithm (provided by Tyler):
  - y[0] = x[0]*T/tau
  - y[t] = exp[-T/tau]*y[t-T] + x[t]*T/tau

x = input, y=output,
t = time, T = sampling period,
tau = filter time const.



This plot was shown earlier by Steven Wren.

IIR

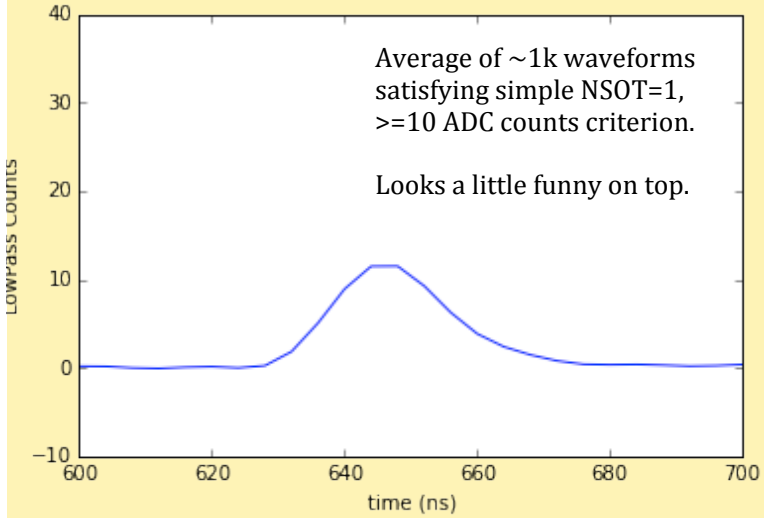
- What would make the IIR unstable?
  - Keeping the “order” low improves stability
    - The filter used here is order 1 (see slide 2)
- We could test possible instability-inducing scenarios by manipulating waveforms
  - E.g., adding a sharp bipolar pulse
- Suggestions for testing instability welcome

FIR

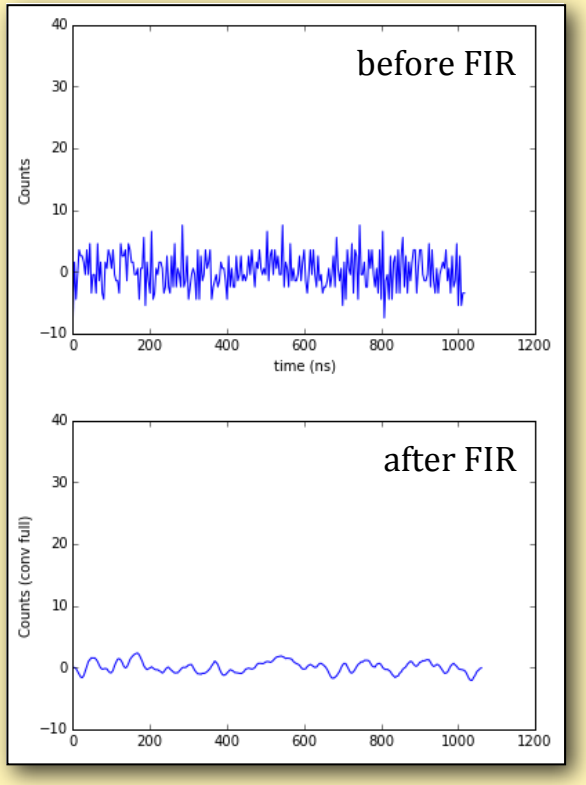
- Algorithm
  - Create a template waveform
    - Done here using an average waveform
  - Convolve template with incoming digitizations
    - Implies performing a convolution at the digitization rate (yikes)
      - Each convolution involves O(100) multiplications (yikes^2)
        - Assumes a template with O(10) bins
    - Before talking about feasibility in an FPGA, let's see how algorithm works in regular software

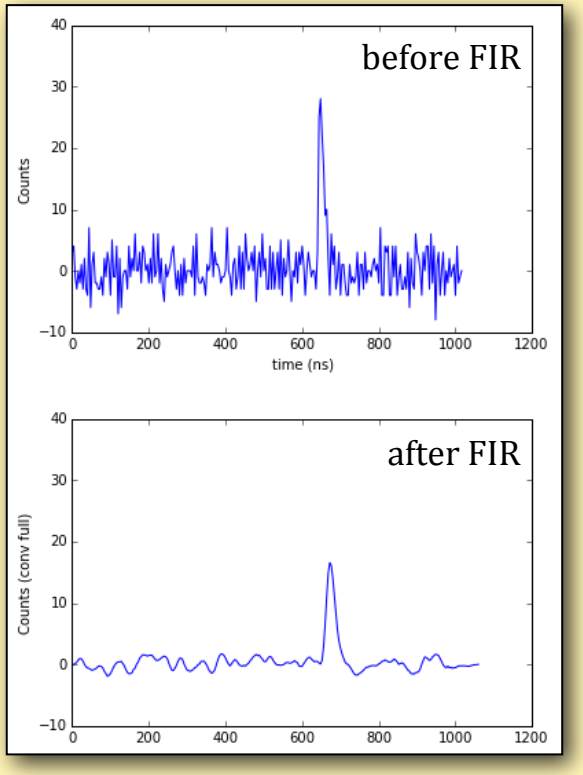
FIR

Template waveform



Sample pure noise and ~SPE waveforms





FIR in an FPGA

- Does FIR have a hope of being fast enough?
  - Quartus has documentation for implementing an FIR in an FPGA
    - Uses altmult_add “megafunction” (link)
  - Not sure how well this would port to Tyler’s implementation with the input signal split into 4 phase-shifted branches...
- With help from Graham Miller (Manchester), Steven Wren and I are going to investigate FIR (and IIR) implementation in the FPGA
  - Steven is working on characterizing the PMT now
  - Anticipate starting FIR/IIR investigation next week