VCC

J1
debug/prog
1
2
3
GND

I2C pullup -> Standard / recommended values

VCC

TP4
Vcc
VCC
TP5
gnd
GND

VCC
U1
ATtiny402

VCC

RESET/PA0 6
PA1 4 scl
PA2 5 sda
PA3 7
PA6 2 gpo
PA7 3

GND 8

GND

TP1
scl
TP2
sda

VCC VCC

R1
4k7
R2
4k7

VCC
U2
ST25DV04K

SDA 5
SCL 6
GPO 7

V_EH 1 V_EH
AC0 2
AC1 3

VCC

JP1
NC

Open to make device standalone
if ATtiny already populated

open drain

TP3
gpo

GND

PA6 is configured as input with pullup

Note: the ST logo serves as
the first pin Marker

AE1
Antenna_Loop

VCC VCC

bulk cap

C1
0.1uF
C2
47uF

GND GND

VCC

C3
0.1uF

Not needed -> Device is inherently stable
enough because it is usually powert via NFC

GND

Current ~~antenna~~ coil design :
6 Turns, 75mm x 50mm,
0.6mm track width,
0.6mm track spacing

generator for design pattern (link)

The ST25DV04 only allows for one link to be active at once (RF or I2C).
The GPO output from the ST25 is used as a busy signal for the ATtiny.
It is pulled low in case of RF activity.

$$L = \frac{1}{4\pi^2 f^2 C}$$

The resonant frequency should be 13.56MHz as pecified by ISO 15693.
With a nominal internal tuning cap (28.5pF), the inductance should be around 5.01uH.
However the the internal tuning cap can vary from 24.8pF to 30.2pF.
Therfore the optimum it can vary from 4.56uH to 5.55uH.
AN3249 recommends to assume a capacitance of 29pF.
Therefore the coil should be around 4.75uH.

IO table for the ATtiny

SOIC 8-pin	Pin Name (1,2)	Other/Special	ADC0	AC0	USART0	SPI0	TWI0	TCA0	TCB0	CCL
6	PA0	RESET/UPDI	AIN0		XDIR	SS				LUT0-IN0
5	PA1		AIN1		TXD	MOSI	SDA	WO1		LUT0-IN1
4	PA2	EVOUT0	AIN2		RxD	MISO	SCL	WO2		LUT0-IN2
7	PA3	EXTCLK	AIN3	OUT	XCK	SCK		WO0/WO3		
8	GND									
1	VDD									
2	PA6		AIN6	AINN0	TXD	MOSI			WO	LUT0-OUT
3	PA7		AIN7	AINP0	RXD	MISO		WO0		LUT1-OUT

E Fachschaft Elektrotechnik

Fabian Steiner
Sheet: /
File: nfc_tag.kicad_sch
Title: NFC card
Size: A4   Date: 2024-09-15   Rev: V0.0.2
KiCad E.D.A. 8.0.1   Id: 1/1