BB Block

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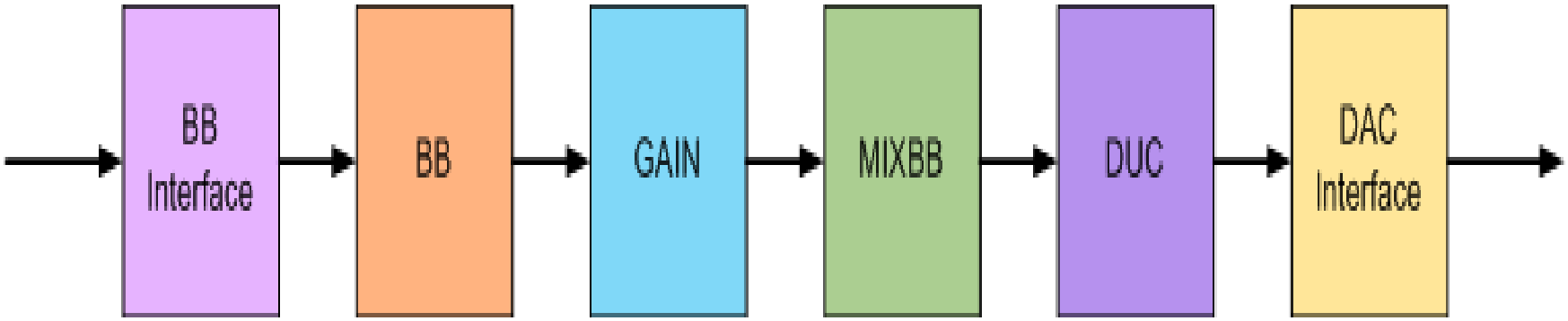
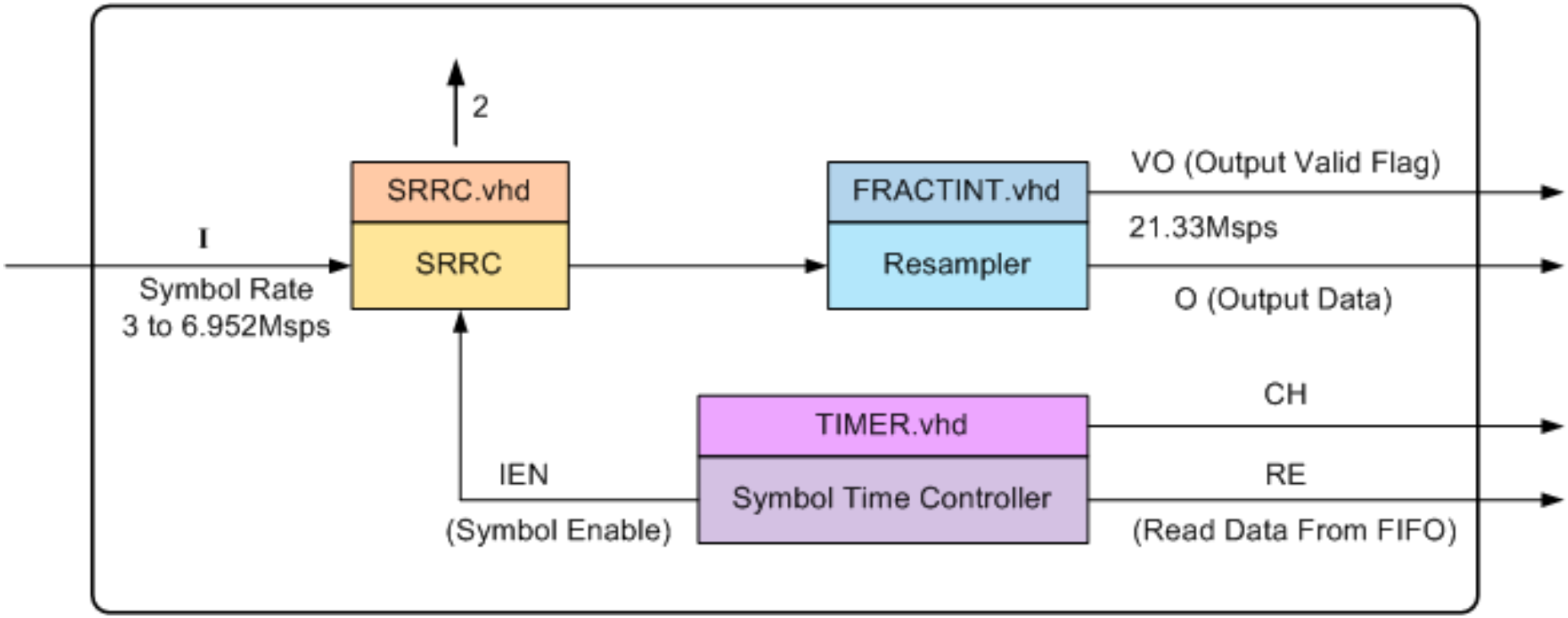
EdgeQAM Design Architecture



BB Interface: control the data between the previous module and BB block
BB: Input symbol rate: 3 to 6.952Msps
Output rate:21.33Msps.
One can support 16 channels
DAC Interface: control the data between DUC and DAC
DUC Output: 4096Msps

BB Block Architecture



BB Block Port Definition

Configuration Port			
Port	**Direction**	**Date Type**	**Description**
PCLK	In	std_logic	Configuration clock (Lower frequency)
WA	In	Ufix_7_0	Configuration address
DI	In	Ufix_32_0	Configuration data
WE	In	Bool	Configuration enable (High effective)
Port Related with Symbol Control			
CLK	In	std_logic	System clock
I	In	2xFix_5_4	Input symbol I&Q, both are Fix_5_4
VI	In	Bool	Input symbol valid flag (High effective)
RE	Out	Bool	Read enable for FIFO (BB Interface)
CH	Out	Ufix_4_0	Select which channel data sent to BB
O	Out	2xFix_16_14	BB Block output data I&Q, both are Fix_16_14
VO	Out	Bool	BB Block output data valid flag (High effective)

BB, GAIN, MIXBB Configuration Method I (Supposed using two BBs each support 16 channels)

The First BB Block Configuration Parameters					
	Configuration Control Signal			Configuration Data	Module
WEB0	WE	WA(6) = 0	WA(5 downto 4) = 0	DI(31 downto 0)	BB/TIMER (Symbol Rate)
WEG0	WE	WA(6) = 0	WA(5 downto 4) = 1	DI(15 downto 0)	GAIN
WEF0	WE	WA(6) = 0	WA(5 downto 4) = 2	DI(31 downto 0)	MIXBB
WA(3 downto 0) = 0~15 indicate the channel number					

The Second BB Block Configuration Parameters					
	Configuration Control Signal			Configuration Data	Note
WEB1	WE	WA(6) = 1	WA(5 downto 4) = 0	DI(31 downto 0)	BB/TIMER (Symbol Rate)
WEG1	WE	WA(6) = 1	WA(5 downto 4) = 1	DI(15 downto 0)	GAIN
WEF1	WE	WA(6) = 1	WA(5 downto 4) = 2	DI(31 downto 0)	MIXBB
WA(3 downto 0) = 0~15 indicate the channel number					

BB, GAIN, MIXBB Configuration Method II (Supposed using two BBs each support 16 channels)

- **WEB0: symbol rate configuration enable signal for the first BB block (WEB1 similar to WEB0)**
- **WEG0: Gain configuration enable signal for the first GAIN block (WEG1 similar to WEG0)**
- **WEF0: Mix configuration enable signal for the first MIXBB block (WEF1 similar to WEF0)**

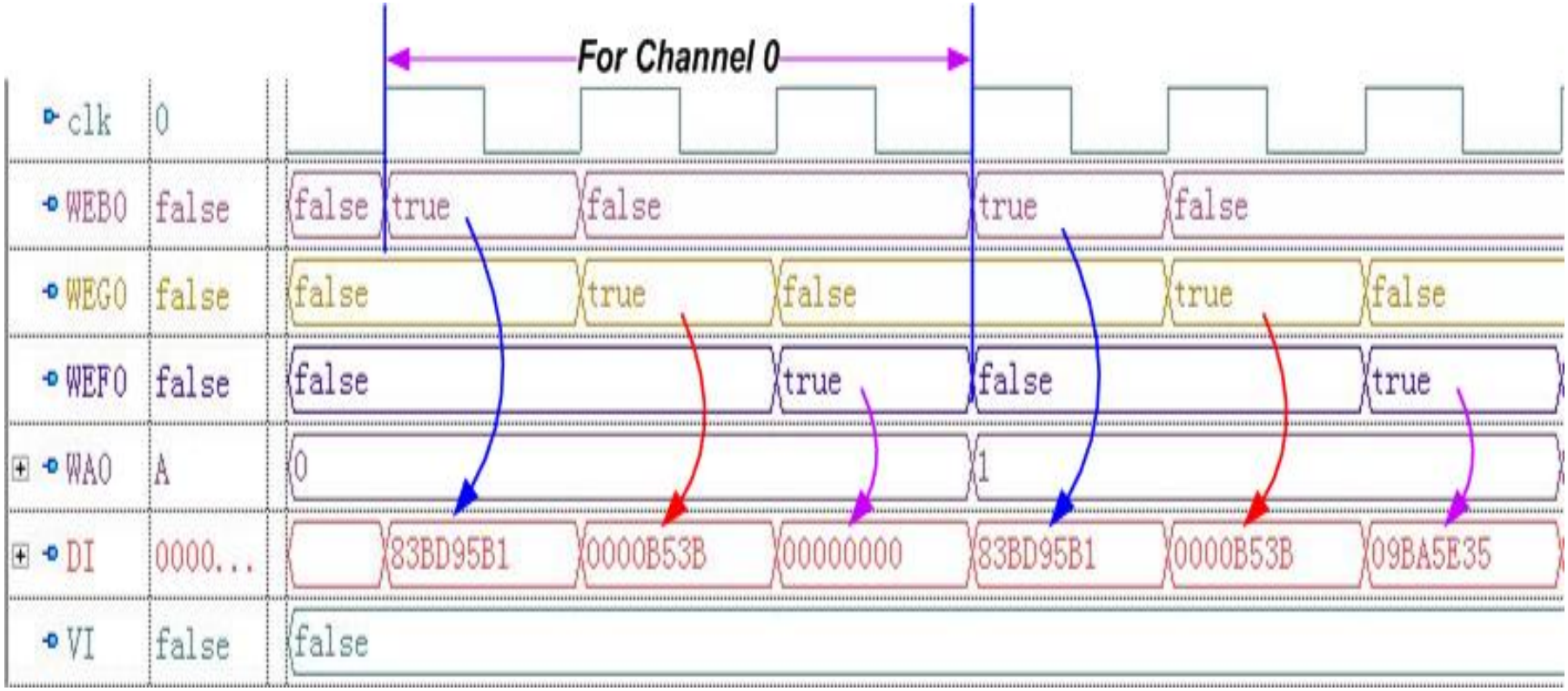
WEB0 <= WE and WA(6)='0' and WA(5 downto 4) = 0;
WEG0 <= WE and WA(6)='0' and WA(5 downto 4) = 1;
WEF0 <= WE and WA(6)='0' and WA(5 downto 4) = 2;
==========
WEB1<= WE and WA(6)='1' and WA(5 downto 4) = 0;
WEG1<= WE and WA(6)='1' and WA(5 downto 4) = 1;
WEF1<= WE and WA(6)='1' and WA(5 downto 4) = 2;

How to Compute Configuration Data

Symbol Rate	M-code	*2*round(R/12*2^31)+1*
	VHDL	*TO_UNSIGNED(INTEGER((R/12.0)*2.0**31),31)&"1"*
Gain	M-code	*round(10^(-G/20)*2^16-1)*
	VHDL	*TO_UNSIGNED(INTEGER(10.0**(-G/20.0)*2.0**16-1.0),32)*
Mix Freq	M-code	*round(F/24*2^32)*
	VHDL	*UNSIGNED(TO_SIGNED(INTEGER(FI/24.0*2.0**DI_TEMP'length),32))*

Example:
R = 6.175339, DI = 32'h83BD95B1
G = 3, DI = 32'h0000B53B
F = 0.912, DI = 32'h09BA5E35

Configuration Timing

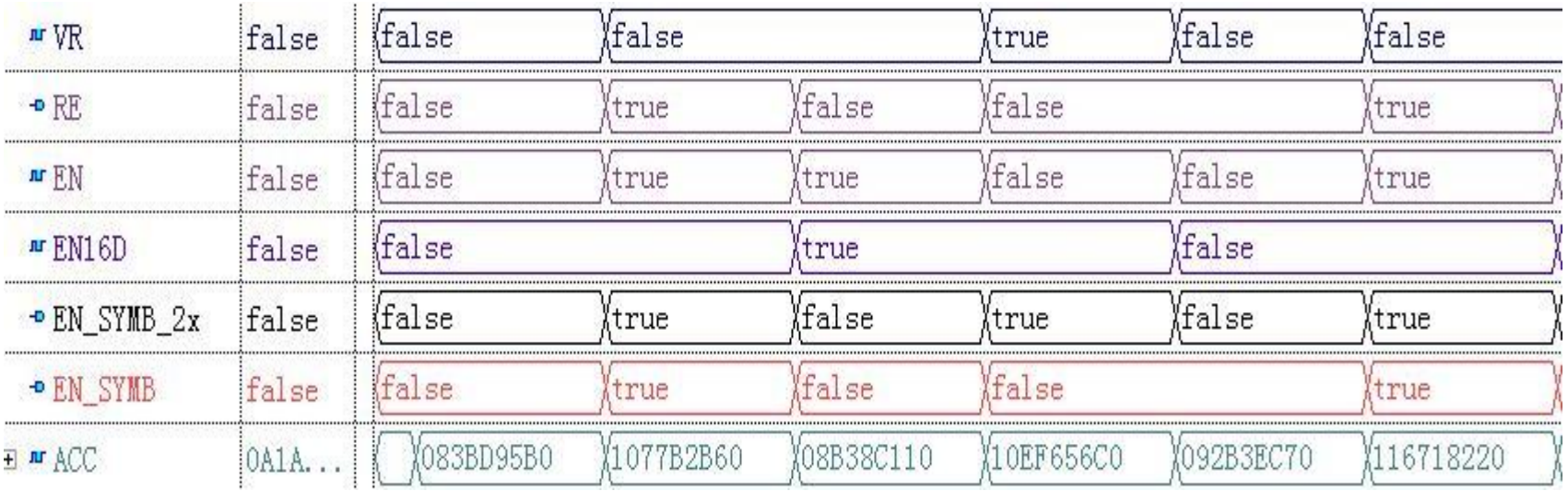


Note:

1. VI should be **FALSE** and WE should be **TRUE** during configuration
2. Configuration clock is PCLK
3. VI should be **TRUE** and WE should be **FALSE** after configuration

Some Notes in Timer

- When configurate symbol rate, the LSB of DI is always ‘1’ which is used as input data enable signal
- The MSB of ACC is used to indicate overflow of accumulator. Because RE is related to it, the MSB of ACC decides the symbol update rate (EN_SYMB_2x is just the MSB of ACC in the below figure)



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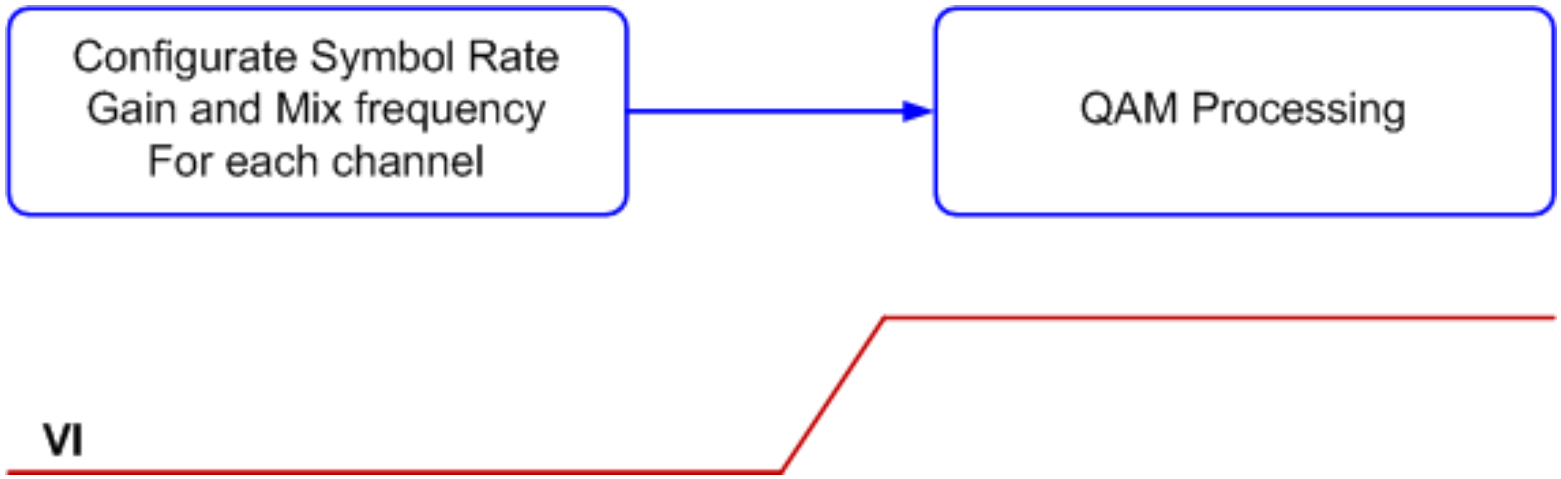
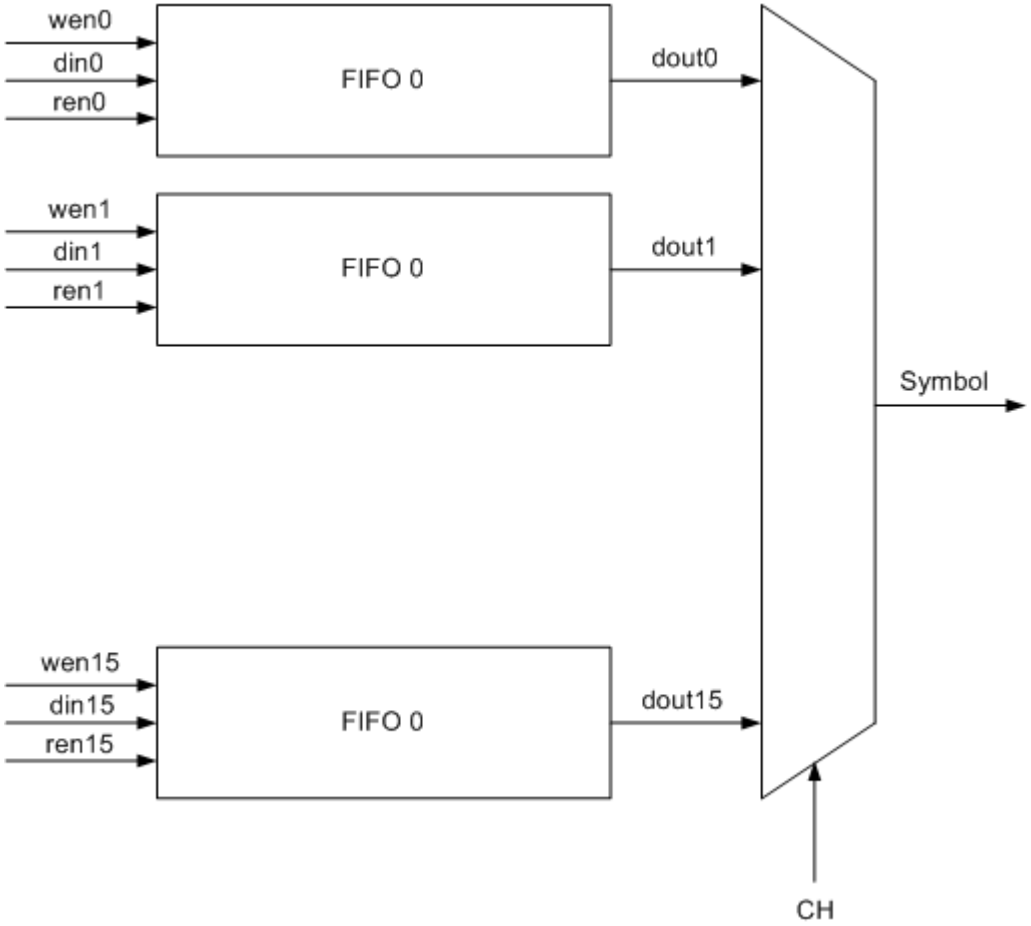
Work Flow of BB Block



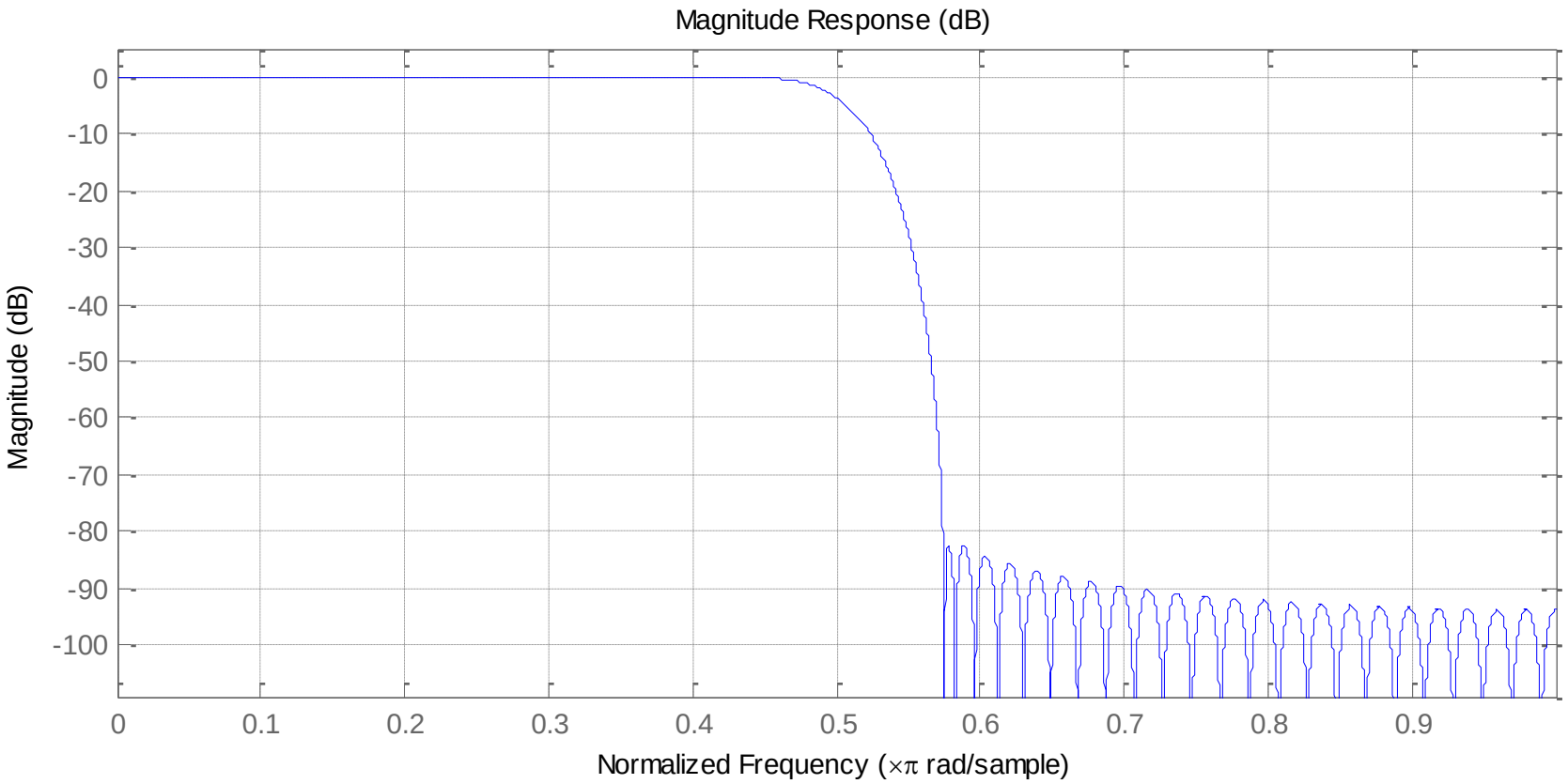
BB Interface Diagram



RE and CH are feedback signals as the output of BB.
ren0 <= RE and CH=0;
ren1 <= RE and CH=1;
ren2 <= RE and CH=2;
reni <= RE and CH=i;
And so on.

SRRC Performance
C_SRRC_15

SRRC Magnitude Response with Roll-off Factor 0.15



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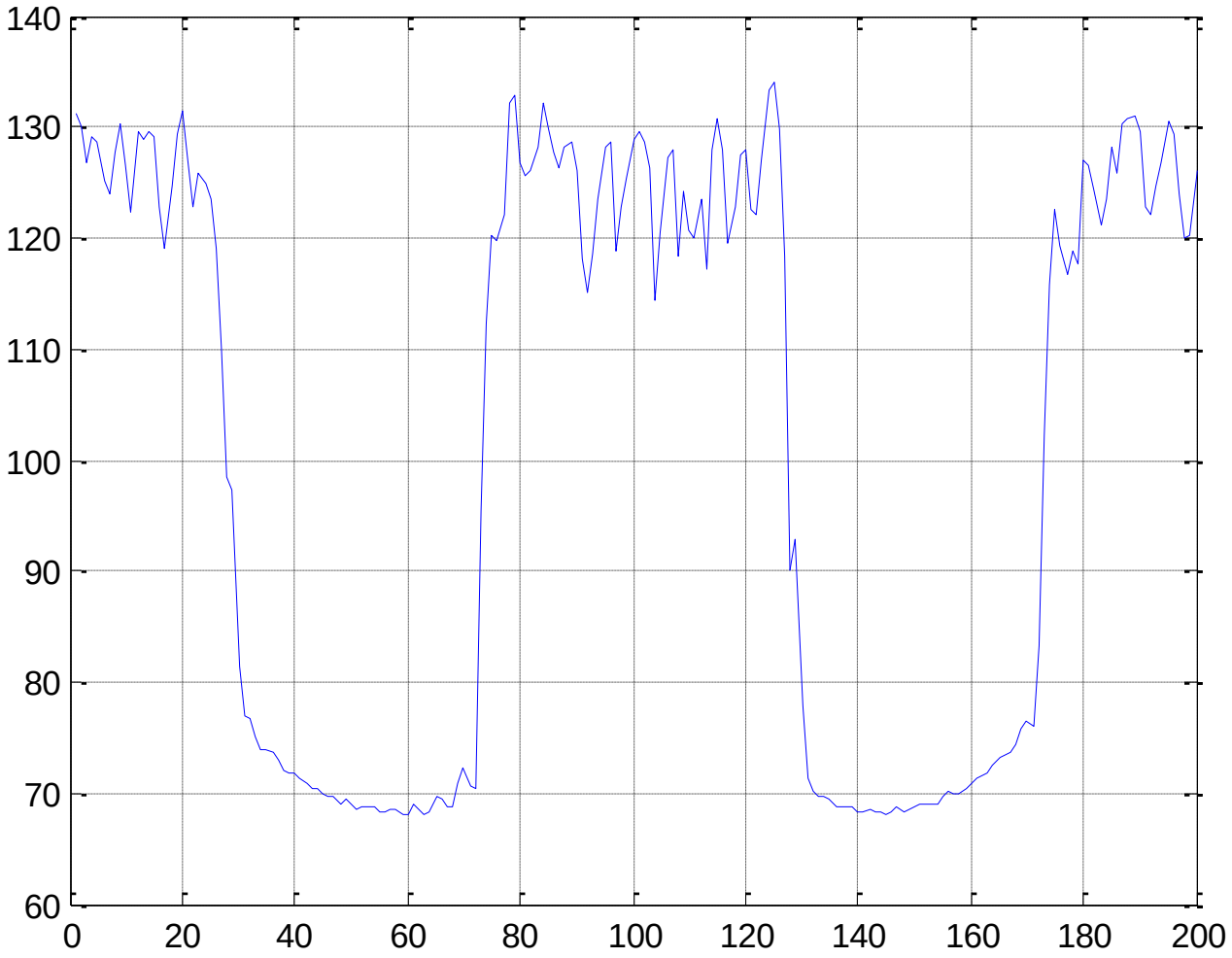
SRRC Output
Frequency Domai with Blackman window



Delay Unit

- BDelay.vhd
- UDelay.vhd
- Delay.vhd
- All the delay unit has the same function. That is to delay the input data with predefined clock period.
- The parameter “SIZE” determines the delay taps.
- BDelay: input data type => boolean
- UDelay: input data type => unsigned
- Delay ： input data type => std_logic_vector

Resource Estimation for One BB Block (In PlanAhead after Elaborate)

RIL Macro Resources

Macro type	Flop	LUT	BRAM	DSP48
Bitwise Logic	0	2	0	0
Arithmetic	0	1236	0	16
Multiplexers	0	1770	0	0
Storage	5037	2469	16	0
Total	**5037**	**5477**	**16**	**16**

RIL Hierarchy Resources

Child	Flop	LUT	BRAM	DSP48
bd	3	4	0	0
fi	1188	784	16	16
sr	3743	4608	0	0
tm	99	73	0	0
ud	0	4	0	0
Primitives	4	4	0	0

Resource Estimation for Two BB Block (In PlanAhead, After Synthesis)

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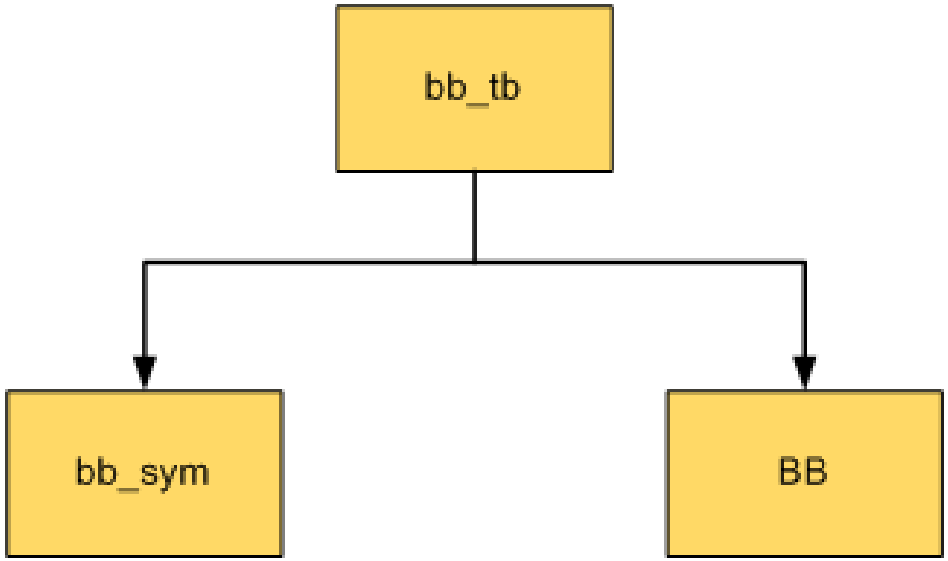
Simulation Hierarchy



bb_sym: Generate Pseudo-random QAM256 Symbol