A DOA and RSS-based Localization Radio System with a CPW-Fed Monopole Array Antenna at the ISM 5.8 GHz Band

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***Abstract*—A complete radio system is designed and built to sound a radio channel in real time and accurately determine the location of a hidden transmitter. According to the given specifications, the implemented receiver is portable and performs the real-time location and channel sounding of a specific transmitter of a BPSK modulated PN9 sequence at the ISM 5.8GHz band. A CPW-Fed monopole antenna array that exhibits high directivity beam switching capability is successfully built. It is a passive component with good input return loss at 5.8GHz. The front-end is properly characterized achieving a correct reception with a minimum input power of -70dBm. The data acquisition, configuration of the front-end modules and control of the antenna directivity are implemented in the PL of the Zynqberry, while the digital signal processing for to the location and channel sounding are performed in the PS. The results are plotted in real time in a graphical interface.**

***Index Terms*—Channel Sounding, Real-Time Localization, DOA, RSS, Monopole Antenna Array, Zynqberry, PDP**

I. Introduction

REAL-TIME location is significantly affected by the high complexity of the signal propagation environment between the transmitter and the receiver. Multipath effect is one of the most challenging problems for wireless technologies, as it can reduce the signal measurement accuracy and degrade the localization performance. Usually, an unknown number of noisy signals arrive to the receiver simultaneously, each from a different direction and with a certain amplitude. Antenna arrays are used in many digital signal processing applications, due to their ability to locate signal sources. In fact, DOA (Direction of Arrival) estimation is a key task of channel sounding, for which various algorithms have been developed [1].

DOA of the signal does not only depend on the SNR (Signal to Noise Ratio) and on the channel structure, but also on the antenna array parameters and their calibration. Therefore, collecting the noisy RSS (Received Signal Strength) measurements can be helpful to estimate the source position. The RSS can be obtained from the In-Phase and Quadrature components of the received complex signal. The main purpose of this paper is to give an overview of an RSS DOA-based System with a Monopole Antenna Array designed to sound a radio channel in real time and accurately determine the location of a hidden transmitter.

The specifications of the transmitter are briefly stated in Section II. Section III gives a detailed description of the receiver and its principal components (antenna array, Front-End, hardware implementation and software implementation). In Section IV, the performance of the proposed approach is analyzed by presenting measurements obtained for distinct test scenarios. A list of parts and materials is shown in Section V, followed by Section VI, with the main conclusions from the presented work.

II. Transmitter Details

To localize the transmitter and also perform the radio channel sounding, the reception system must be designed according to the transmitter's characteristics. These are: (1) The transmitter's center frequency is within the 5GHz ISM band (Industrial, Scientific and Medical band). The frequency range of this band is 5.725–5.875GHz, where the carrier frequency is nominally 5.8GHz. Thus, the receiver must be capable of tuning to any frequency within this band. (2) The carrier is modulated using BPSK (Binary Phase Shift Keying). (3) The baseband transmitter signal is a PN (Pseudo-Noise) sequence generated by a linear 9th order feedback shift-register (PN9) at a rate of 1 Mchips/s. (4) The baseband signal is filtered using a RC (Root Raised Cosine) filter with a roll-off factor of 0.5. (5) The modulated signal is amplified and applied to a single monopole antenna. (6) The EIRP (Effective Isotropic Radiated Power) of the transmitter does not exceed ISM limitations in the 5GHz ISM band, which are 30dBm transmit power, 36dBm EIRP.

III. Description of the System

Fig 1 shows the overall structure of the receiver, composed by an antenna array, a Front-End and a Zynqberry Board.

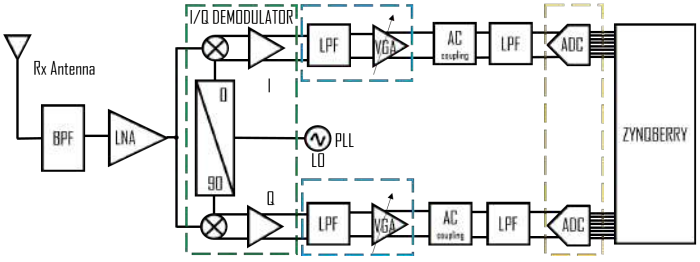

Fig. 1: Block diagram of the Receiver Front-End

A. Antenna Array

The incoming signal is received sequentially from four different directions in the azimuthal plane. With this purpose, we have used CST Microwave Studio to design a CPW (Coplanar Wave Guide)-Fed Monopole Antenna Array with Integrated PIN Diode Switches [2]. This electrically steerable beam allows to reduce the power consumption and diminish multipath. The antenna is found to achieve a remarkable balance between complexity and performance. In Fig.2, the driven element (1) is encircled by four parasite elements (2–5) of height 8mm ($\lambda/4$). The parasitic element configuration is controlled by a quarter wavelength CPW line.

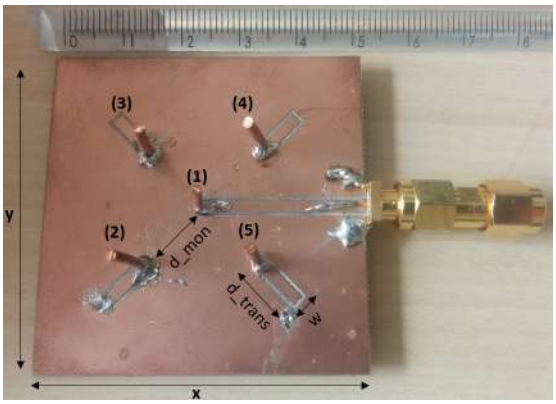

Fig. 2: Dimensions of the Antenna Array

The measured reflection coefficient $|S11|_{dB}$ is below -10dB from 5.7 to 6.1GHz, as seen in Fig. 3.

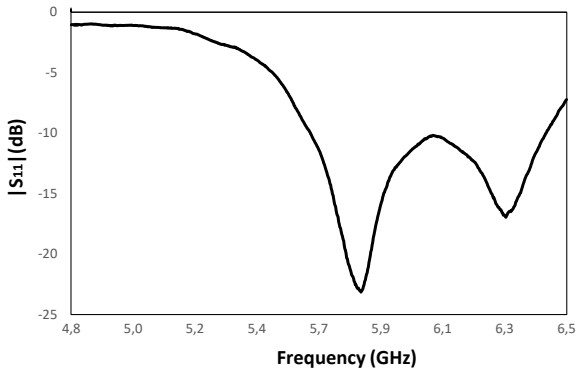

Fig. 3: Measured reflection coefficient $|S11|_{dB}$

Practically, capacitors and PIN diode switches are used to short- and open-circuit the CPW line to provide high and low impedance at the base of the parasite monopole. The PIN diode is placed about a quarter wavelength away from the capacitor, close to the parasite base (8mm). The configuration of the parasite element can be altered by providing enough current to the PIN diode switches (Fig.4). They act as a short circuit when supplied with 1V, and as an open circuit when they are not fed. The bias circuit for the diodes is composed by a 68nH inductor and a 115Ω resistor.

The dimensions of the designed antenna array in Fig. 2 are detailed in Table I and the dielectric substrate used in this design is an FR4 substrate with a thickness of 0.8mm.

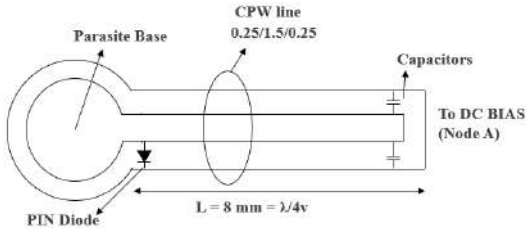

Fig. 4: Diagram of CPW line of the parasite elements

TABLE I: Antenna Array Dimensions

x	y	d_trans	d_mon	w
50mm	50mm	10mm	13mm	2mm

B. Front-End

As shown in Fig. 1, the signal goes through a 5.5GHz BPF (Band Pass Filter). The LNA (Low Noise Amplifier) amplifies the signal 10dB when operating in gain mode. If it is in bypass mode it introduces a loss of 7dB. Then, the signal is down converted to 2MHz by the I/Q demodulator, fed by a LO (Local Oscillator) signal at 5.798GHz generated by a PLL (Phase Locked Loop). From now on, the interfaces are differential, in order to avoid the lossy baluns placed as board output/input interfaces, and to suppress the even order-harmonics that cannot be filtered out in single-ended interfaces [3]. The baseband signal passes through a VGA (Variable Gain Amplifier) with a baseband programmable filter. The DC offset provided by the IQ demodulator can be removed in this stage. AC Coupling (SMA DC Blocks) and low pass filtering are performed in both I and Q branches at the output of the VGA. The next stage is the analog to digital conversion of incoming IQ differential signals with a resolution of 16 bits at sampling frequency of 12MSPS. The samples are outputted in Dual Data Rate mode through PCI and an ADC Adapter Board was designed to read those samples with the Zynqberry.

Fig. 5 shows the main components of the receiver and the general specifications are highlighted in Table II. The receptor is organized in two different layers. The top layer contains the Zynqberry platform, the ADC and the antenna array and the rest of the elements form the bottom layer.

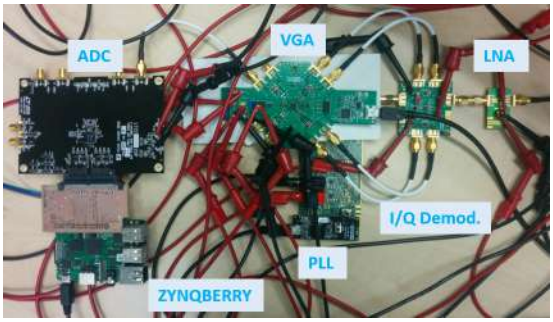

Fig. 5: Main Components of the Receiver

TABLE II: Front-End Specifications

	Units	LNA	PLL	I/Q DEMOD.	VGA	ADC
VDD	V	3.3	6	5	3.3	5
Current	mA	44	242	300	61	112
Power Gain	dB	10	-	5.8	30-60	0
Noise Figure	dB	1.6	-	15.5	30	56.9

C. Hardware implementation

The Xilinx *Zynq-7010 All Programmable SoC* integrates a dual-core or single-core ARM Cortex ™-A9 based PS (Processing System) and a Xilinx PL (Programmable Logic) in a single Raspberry Pi compatible platform. As seen in Fig.6, all the available GPIOs (General Input Output Ports) of this platform are used for the data acquisition, the configuration of the VGA, PLL and ADC modules through SPI and the control of the directivity of the antenna array.

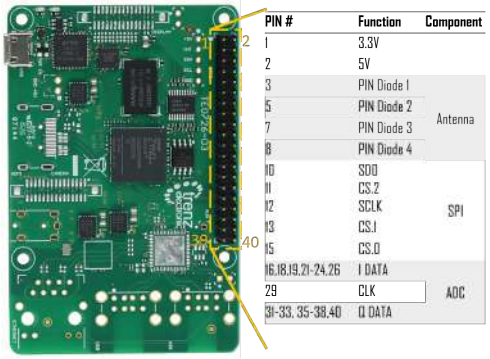

Fig. 6: Diagram of the Zynqberry Pin Connections

Fig.7 shows the structure of the PL and PS in the Zynqberry. The clock frequency of the created hardware design in the PL is 100MHz. The ADC is configured in DDR (Double Data Rate) to reduce the number of pins to 17: 8 for I branch, 8 for Q branch and 1 for the output clock reference of the ADC. The dataflow is as follows: First of all, the created hardware design stabilizes the incoming asynchronous data from those pins using *STAB* RTL (Register Transfer Logic) module, composed by a chain of 3 D Flip-Flops. Next, the *DEMUX* RTL module performs the demultiplexing of the incoming bits joining them in a single "IQ-vector" of 32 bits (16 bits Q and 16 bits I). This module reads the even bits of I and Q branches each rising edge of the ADC's clock reference and also the odd bits each falling edge. Then, the "IQ-vector" is sent to a FIFO buffer. Finally the data is transferred to PS using a Xilinx AXI DMA (Direct Memory Access) that is controlled by a synchronization RTL module called *FIFO TO DMA SYNCH*, which is in charge of setting the time for changing the directivity of the antenna array. Concretely, it transfers 5 received and sampled PN9 sequences to the PS each time the antenna is pointing in one direction.

The *MUX* RTL module is created and the AXI GPIO is used in the PL to control the directivity of the array antenna from the PS.

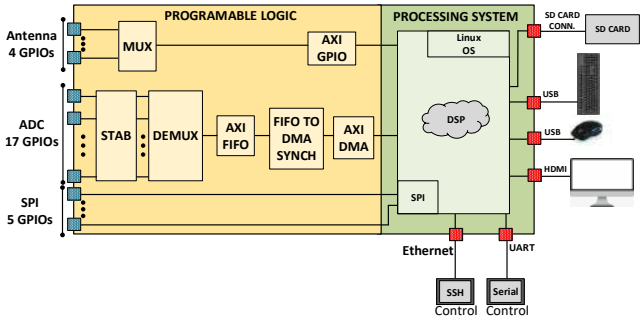

Fig. 7: Block Diagram of the implemented design on the Zynqberry

D. Software implementation

Two user applications are created in the PS. The first one is called *SPI* and is used to configure the PLL, VGA and ADC modules. The second one, called *DSP*, performs the DOA estimation and the channel sounding. Fig. 8 shows the complete workflow of *DSP* application.

Taking into account that it takes 511 μs to send a PN9 sequence and as the sampling frequency is 12MSPS, one complete PN9 sequence is formed by 6132 samples. As 5 PN9 sequences are received while the directivity of the antenna array is kept constant, it means that the data are processed in blocks of 30660 samples (or 122640 Bytes). The received samples from the PL of the Zynqberry are analyzed in the PS in order to detect the direction from which the signal comes with the most strength. First of all, the signal is downconverted from 2MHz to baseband and passes through an RRC filter with a roll-off factor of 0.5. Ideally, the BPSK signal uses the I channel, but due to the RF impairments and the non-ideal channel, the received data might have a Q component. Advantage of the latter is taken and used to correct the experimented offsets.

RSSI (Received Signal Strength Indicator) is a measurement of the power present in the received radio signal. The power of each length-511 frame is calculated and the values obtained for different angles of the antenna directivity are compared. The one with the highest power is the one from which the transmitted signal is more likely to come. Therefore, the receiver is moved along that direction to carry out new measurements and estimate again the DOA.

Once the directivity with highest power is detected, the channel sounding is performed. For the timing synchronization that is subsequently carried out, it is necessary to generate an ideal PN9 sequence. Fig. 9 shows the computed circular buffer correlation between the real part of the received signal and the ideal PN sequence. At this point, the signal is downsampled, because it had an oversampling factor of 12, introduced by the ADC.

To characterize the time delay of the channel, the PDP (Power Delay Profile) is calculated. $P(\tau)$ gives the distribution

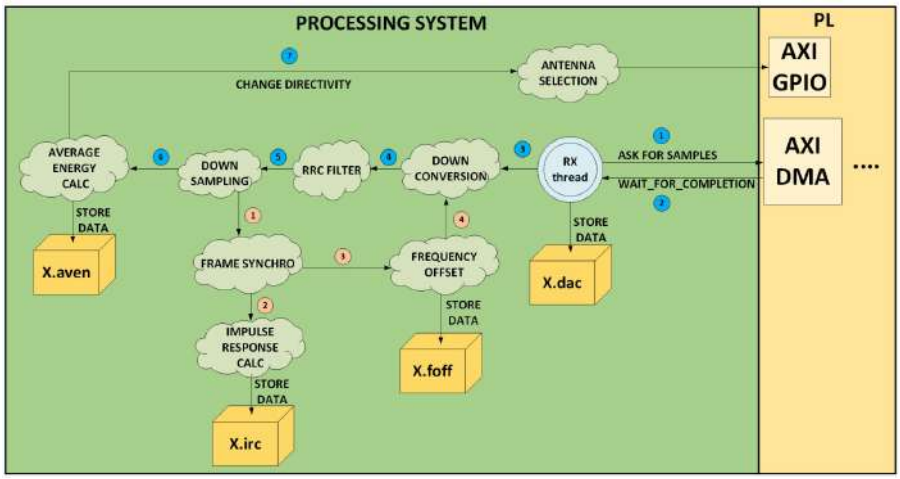

Fig. 8: Block Diagram of *DSP* user application: DOA and Channel Sounding Implementation

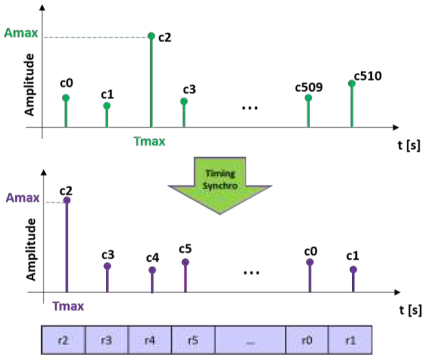

Fig. 9: Diagram of the Circular Buffer Correlation and Timing Synchronization

of signal power received over a multipath channel as a function of propagation delays. In the PDP plot, the signal power of each multipath is plotted against their respective propagation delays. Specifically, $P(\tau)$ is the Fourier Transform of the autocorrelation function of the channel impulse response $h(t,\tau)$. Taking the Fast Fourier Transform of the ideal PN sequence and the received signal (Y(f) and X(f)), the frequency domain description of the channel in (1) is obtained. By computing the IFFT (Inverse Fourier Transform) of H(f), $h(t,\tau)$ is obtained, and thus, the PDP.

$$H(f) \approx Y(f)/X(f) \tag{1}$$

IV. Measurements with the System

This section presents the measurements obtained when testing the receiver with the laboratory equipment and the designed software. We transmitted a PN9 sequence with an output power of 0dBm. The spectrum of the signal at the output of the VGA, down converted to 2MHz, is the one in Fig.10. We took measurements with the antenna array pointing in the four directions, and a difference in the received power can be clearly observed. In this case, the signal was coming from direction (2), where the measured power is -3.77dBm, whereas it is lower than -18dBm in the rest of the directions. The received waveforms also present coherent shapes when evaluating them in time domain, allowing the correct identification of the direction of the incoming wave. The front-end allows input powers up to -70dBm.

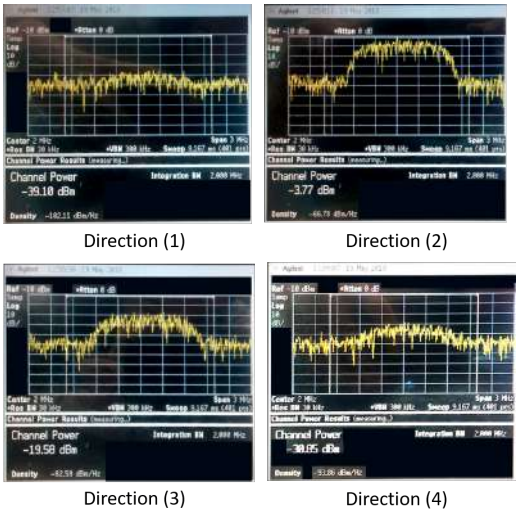

Fig. 10: Spectrum of the signal in four directions

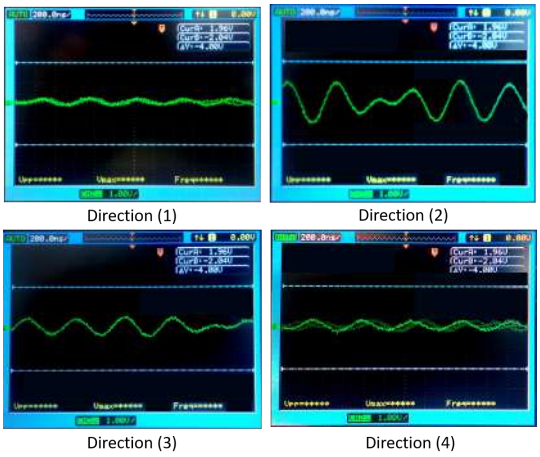

Fig. 11: Waveform in time-domain in four directions

TABLE III: Bill of Materials

Qty (Units)	Name	Ref	Price per Unit (€)	Distributor
1	I/Q DEMOD.	ADL5380 - EVALZ	95.1	Digikey
1	BPF	5515BP15B725E	0.39	Digikey
1	LNA	OM7870: BGU7258 WLAN LNA	128.74	NXP
1	VGA	ADRF6518-EVALZ-ND	190.19	Digikey
1	PLL	EV-ADF4355-3SD1Z-ND	237.73	Digikey
1	ADC	DC1975A-A-ND	164.1	Mouser
1	ZYNQBERRY Z7010	TE0726 TRM	101.43	Digikey
11	PIN diode	630-HPND-4005	19.14	Mouser
1	Controller Board	SDP-S	39.37	Analog Devices
1	Card Assembly	SAM11495-ND	8.76	Digikey
4	DC Blocks SMA	744-1268-ND	15.52	Digikey
1	Board CLK Generator	1528-1206-ND	6.53	Digikey
TOTAL COST			**1265.77** ($**1484.17**)	

The graph in Fig.12 is the PDP obtained when plotting the received voltage values processed and stored in a file. It shows the impulse response of the channel as a function of time, where it is observed that the device is able to detect and synchronize a signal with time offset.

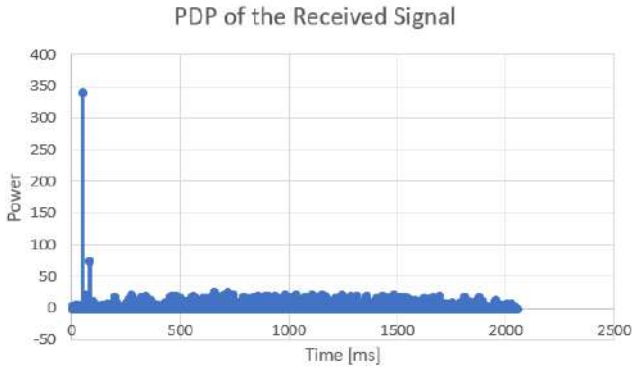

Fig. 12: PDP of the channel impulse response

V. Parts and Materials

Table III shows the list of parts and materials required for the set up of the receiver, including where to obtain them and their cost. Moreover, apart from these components, we have used some other materials (such as wires and connectors) and testing laboratory equipment provided by the university.

VI. Conclusion

A 5.8GHz real-time location and channel sounding portable receiver is demonstrated to be appropiate and innovative for its efficient DOA estimation, beam switching antenna array design and didactic purpose for fading channel illustration.

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