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TECHNICAL ARTICLE

LOW POWER PRECISION DATA ACQUISITION SIGNAL CHAIN FOR SPACE CONSTRAINED APPLICATIONS

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Introduction

For many applications in the instrumentation, industrial, and healthcare industry, system designers develop a wide range of data acquisition cards for interfacing with various sensor types: optical, temperature, pressure, magnetic, vibration, and acoustic, to name a few. The output signals from these sensors are typically single-ended or differential. In such applications, the analog front end takes either a single-ended or differential signal and performs gain or attenuation, antialiasing filtering, and level shifting as required and then drive the inputs of the ADC at the full-scale level. Both single-ended to differential and fully differential signal chain configurations require extra circuitry to level shift the input signal. However fully differential signal chain offers greater noise rejection and twice the signal swing at the expense of increased power and a more complex signal chain. The analog front end sometimes use an optional instrumentation amplifier or JFET amplifier before the ADC driver stage for high impedance sensors interface. Depending on application requirements, system designers either multiplex the outputs from the various sensors into a single data acquisition channel or use simultaneous sampling to digitize the signals from individual sensors to allow an increased sampling rate per channel. They are pushed to find innovative ways to maintain balance among optimum performance, thermal power dissipation, and increased circuit density challenges. A typical high level sensors-to-bits data acquisition signal chain is shown in Figure 1.

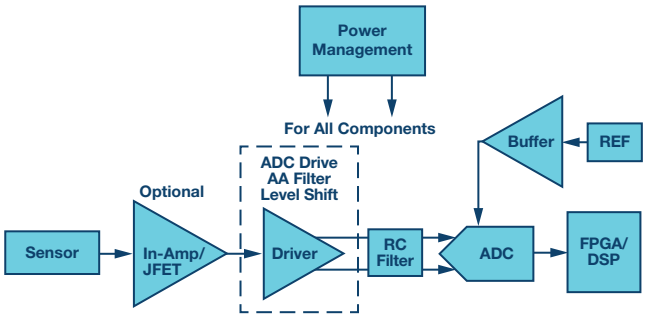

Figure 1. Typical sensors-to-bits data acquisition signal chain.

Two popular methods are single-ended-to-differential conversion and differential-to-differential conversion.

This article proposes a low power precision data acquisition system solution for fully differential and single-ended input signal configurations, focuses on its key design considerations, and demonstrates how to achieve optimum performance for space constrained applications. The low power signal chain presented here utilizes the ADA4940-1 low noise fully differential amplifier, AD7982 differential-input 18-bit PulSAR® ADC, and ADR435 precision voltage reference that also eases analog signal conditioning by eliminating the need for an extra driver stage and saving board space.

Fully Differential 18-Bit Data Acquisition Signal Chain

Successive approximation register (SAR) ADCs are used in myriad applications for their high precision performance, low latency, and relatively reduced power dissipation. Fully differential input unipolar SAR ADCs offer higher resolution and better ac and dc performance and the majority of them require the input common mode to be at $V_{REF}/2$ in order to maximize the signal swing and differential antiphase signal (180° out of phase with each other) on each of its inputs. This can involve level shifting the incoming signal. The precision, low power, 18-bit, 1 MSPS AD7982 differential input unipolar PulSAR ADC requires a differential ADC driver for optimum performance. This ADC offers a versatile serial digital interface compatible with SPI, QSPI, and other digital hosts. The interface can be configured for a simple 3-wire mode for the lowest I/O count, or a 4-wire mode that allows options for the daisy-chained readback and busy indication. The 4-wire mode also allows independent readback timing from the CNV (convert input), which enables simultaneous sampling with multiple converters.

Manufactured using Analog Devices proprietary SiGe complementary bipolar process, the low power, low noise, fully differential amplifier, ADA4940-1, is optimum for driving 16-bit and 18-bit ADCs with minimal degradation in performance. As shown in Figure 2, it drives the differential inputs of the AD7982, 18-bit, 1 MSPS ADC and the ADR435, low noise, precision 5 V reference is used to supply the 5 V needed for the ADC. The ADR435 provides sufficient output current and eliminates the need of a reference buffer by using a 22 µF decoupling capacitor on the REF pin of the AD7982. All the ICs shown in Figure 2 are available in small footprints, including 3 mm × 3 mm LFCSP, 4 mm × 4 mm LFCSP, and 3 mm × 5 mm MSOP, which helps to reduce board space.

A single-pole, 2.7 MHz, RC (22 Ω, 2.7 nF) low-pass filter is placed between the ADC driver output and the ADC inputs to help limit the noise at the ADC inputs and reduce the effect of kickbacks coming from the capacitive DAC input of an SAR ADC. However, too much bandlimiting can affect settling time and increase distortion. Therefore, it is very important to find the optimal RC values for this filter. C0G or NP0 type capacitors are recommended for an RC filter that has high Q, a low temperature coefficient, and stable electrical characteristics under varying voltages. A reasonable value of series resistance should be chosen to keep the amplifier stable and limit its output current.

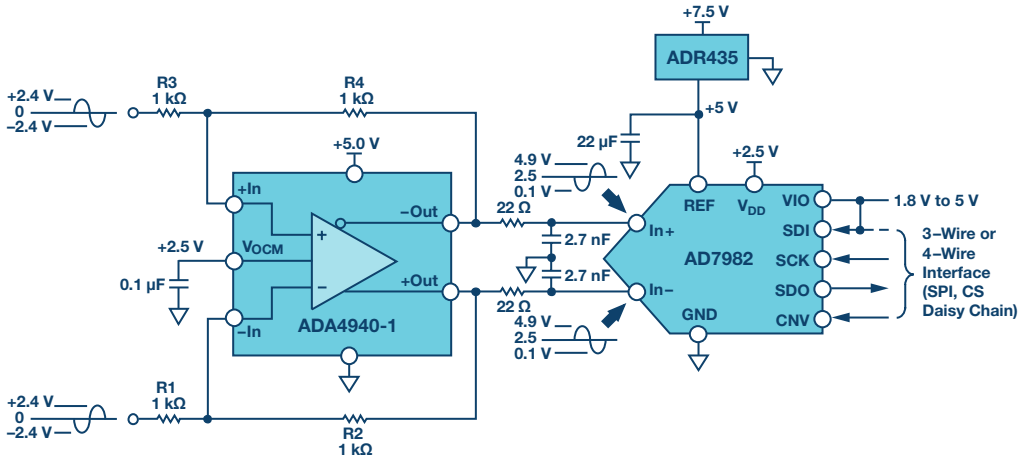

Figure 2. Low power, fully differential, 18-bit, 1 MSPS data acquisition signal chain (simplified schematic: all connections and decoupling not shown).

A low distortion, high performance signal source, the Audio Precision® SYS-2702, is used in all the test cases below to achieve the optimum performance. In this case, a 9.6 V p-p differential output from the signal source is fed into the ADC driver inputs to get full-scale dynamic range performance of the ADC using a 5 V reference. With an output common-mode voltage of 2.5 V, each ADA4940-1 output swings between 0.1 V and 4.9 V, opposite in phase, providing a gain of 1 and a 9.6 V p-p differential signal to the ADC input. Note that each ADA4940-1 input requires 200 mV footroom from the ground and 1.2 V headroom from 5 V supply. Each ADA4940-1 output also requires 100 mV footroom and headroom from the ground and 5 V supply, respectively.

When used as an ADC driver, the ADA4940-1 allows the user to do the necessary signal conditioning, including level shifting and attenuating or amplifying the signal for more dynamic range using four resistors, thus eliminating the need for an extra driver stage. The ratio of feedback resistors (R2 = R4) to gain resistors (R1 = R3) sets the gain, where R1 = R2 = R3 = R4 = 1 kΩ.

For a balanced differential input signal, the effective input impedance would be 2× gain resistor (R1 or R3) = 2 kΩ, and for an unbalanced (single-ended) input signal, the effective impedance would be approximately 1.33 kΩ using the equation

$$\frac{R3}{1-\frac{R4}{2\times(R3+R4)}}$$

A termination resistor in parallel with the input can be used if required.

The ADA4940-1 internal common-mode feedback loop forces common-mode output voltage to equal the voltage applied to the V_{OCM} input and offers an excellent output balance. The differential output voltage depends on V_{OCM} when two feedback factors β1 and β2 are not equal and any imbalance in output amplitude or phase produces an undesirable common-mode component in the output and causes a redundant noise and offset in the differential output. Therefore, it's imperative that the combination of input source impedance and R1 (R3) should be 1 kΩ in this case (that is, β1 = β2) to avoid the mismatch in the common-mode voltage of each output signal and prevent the increase in common-mode noise coming from the ADA4940-1.

Noise Analysis

As signals travel through the traces of a printed circuit board (PCB) and long cables, system noise accumulates in the signals and a differential input ADC rejects any signal noise that appears as a common-mode voltage. Differential signals increase the dynamic range of the ADC, and they offer better harmonic distortion performance.

The expected signal-to-noise ratio (SNR) of this 18-bit, 1 MSPS data acquisition system can be calculated theoretically by taking the root sum square (RSS) of each noise source–ADA4940-1, ADR435, and AD7982.

The ADA4940-1 offers low noise performance of typically 3.9 nV/√Hz at 100 kHz as shown in Figure 3.

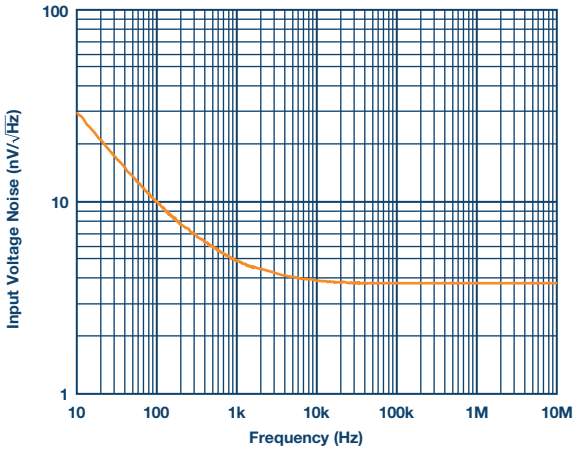

Figure 3. ADA4940-1 input voltage noise spectral density vs. frequency.

It is important to calculate the noise gain of the differential amplifier in order to find its equivalent output noise contribution.

The noise gain of the differential amplifier is:

$$NG = \frac{2}{(\beta 1 + \beta 2)} = 2 \text{ V/V}$$

where

$$\beta 1 = \frac{R1}{R1 + R2} = 0.5$$

and

$$\beta 2 = \frac{R3}{R3 + R4} = 0.5$$

are two feedback factors.

The following differential amplifier noise sources should be taken into account:

- Since the ADA4940-1 input voltage noise is 3.9 nV/√Hz, its differential output noise would be 7.8 nV/√Hz.
- The ADA4940-1 common-mode input voltage noise (e_{OCM}) is 83 nV/√Hz from the data sheet, so its output noise would be

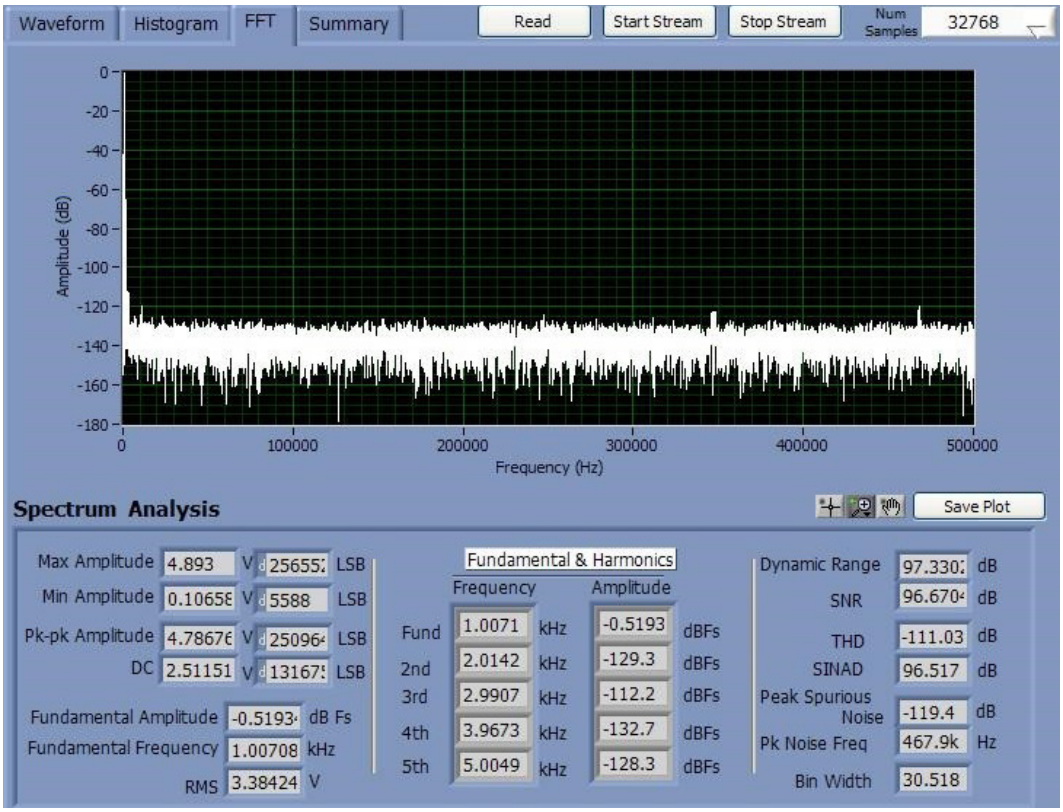

Figure 4. FFT plot, f_{IN} = 1 kHz, F_S = 1 MSPS (ADA4940-1 configured as fully differential driver).

$$- e_{OCM} \times (\beta 1 - \beta 2) \times NG = 0.$$

- Noise from the R1, R2, R3, and R4 resistors can be calculated based on the Johnson-Nyquist noise equation for a given bandwidth. $e_{Rn} = \sqrt{(4k_B TR)}$, where k_B is the Boltzmann constant (1.38065 × 10 – 23 J/K), T is the resistor's absolute temperature in kelvin, and R is the resistor value in ohms (Ω). The noise from the feedback resistors would be $e_{R2} = e_{R4} = 4.07$ nV/√Hz.
- The noise from the R1 would be $e_{R1} \times (1 - \beta 1) \times NG = 4.07$ nV/√Hz and R3 would be $e_{R3} \times (1 - \beta 2) \times NG = 4.07$ nV/√Hz.
- The ADA4940-1 current noise is 0.81 pA/√Hz from the data sheet.
  - Inverting input voltage noise:

    $iIN- \times R1 || R2 \times NG = 0.81$ nV/√Hz
  - Noninverting input voltage noise:

    $iIN+ \times R3 || R4 \times NG = 0.81$ nV/√Hz

So, the equivalent output noise contribution from the ADA4940 would be:

$$= \sqrt{(7.9e-9)^2 + (0)^2 + 4 \times (4.07e-9)^2 + 2 \times (0.81e-9)^2}$$
$$= 11.33 \text{ nV}/\sqrt{\text{Hz}}$$

The total integrated noise at the ADC input (after RC filter) would be

$$11.33 \text{ nV}/\sqrt{\text{Hz}} \times \sqrt{(2.7e6 \times \pi/2)} = 23.26 \ \mu\text{V rms}$$

The rms noise of AD7982 can be calculated from its typical signal-to-noise ratio (SNR) of 98 dB for a 5 V reference.

$$e_{AD7982} = 10^{\left(-\frac{SNR}{20}\right)} \times V_{signal-\text{rms}} = 10^{\left(-\frac{98}{20}\right)} \times 3.353 \text{ V}$$
$$= 44.50 \ \mu\text{V rms}$$

Using these numbers, the total noise contribution from the ADC driver and ADC would be

$$V_{noise\text{-}rms} = \sqrt{(23.26e-6)^2 + (44.50e-6)^2} = 50.22 \ \mu\text{V rms}$$

Note that the noise contribution from the ADR435 reference is ignored in this case as it's negligible.

So, the theoretical SNR of the data acquisition system can be estimated as shown below.

$$SNR = 20 \times log\left(\frac{V_{signal-\text{rms}}}{V_{noise-\text{rms}}}\right) = 20 \times log\left(\frac{3.353 \text{ V}}{50.22 \ \mu\text{V rms}}\right)$$
$$= 96.95 \text{ dB}$$

The AD7982 achieves typically 96.67 dB of SNR and –111.03 dB of THD for a 1 kHz input signal as shown in its FFT performance of Figure 4. The measured SNR of 96.67 dB in this case is pretty close to the theoretical estimated SNR of 96.95 dB above. The actual loss from the target SNR of data sheet specified 98 dB is attributed to the equivalent output noise contribution from the ADA4940 differential amplifier circuit. The typical INL and DNL performance of the AD7982 is shown in Figure 5.

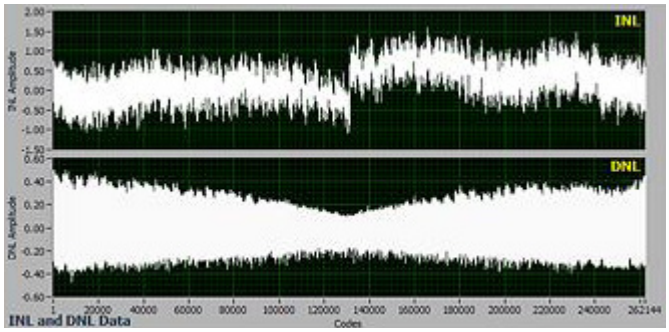

Figure 5. INL and DNL plot with sampling frequency of 1 MSPS (min/max INL = +1.6/–1.1 LSB and DNL = ±0.5 LSB).

Single-Ended-to-Differential 18-Bit Data Acquisition Signal Chain

In many applications, the single-ended-to-differential configuration is most commonly used with differential ADCs because the output signals from many sensors are typically single-ended and in some cases the stage following the sensors being an instrumentation or JFET amplifier. In this case, these signals require single-ended-to-differential conversion using extra circuitry in order to feed the signal in to the differential input ADC down the stream and take advantage of the full-scale range of the ADC. The single-ended-to-differential conversion can be implemented using a discrete amplifiers solution in several ways and each method has its own pros and cons. However, it comes at the expense of extra board space and added cost. The proposed low power solution using a fully differential ADC driver offers optimum performance in a single-ended-to-differential conversion configuration and the integrated output common-mode control of an ADC driver also eases the pain of level shifting the signal, eliminating the need for an extra signal conditioning stage. The same circuit can also accept a ±4.8 V single-ended input signal from signal source to generate the fully differential output signal of 9.6 V p-p and drive the ADC inputs to maximize dynamic range performance as shown in Figure 6. The AD7982 achieves typically 95.89 dB of SNR and –110.14 dB of THD for a 1 kHz input signal as shown in its FFT performance of Figure 7.

Power Dissipation

Many data acquisition systems demand low power and reduced board size for space constrained applications. The AD7982 operates from a single V_{DD} supply of 2.5 V and dissipates only around 6.1 mW at 1 MSPS using a 5 V reference and 3 V VIO supply. Its power also scales linearly

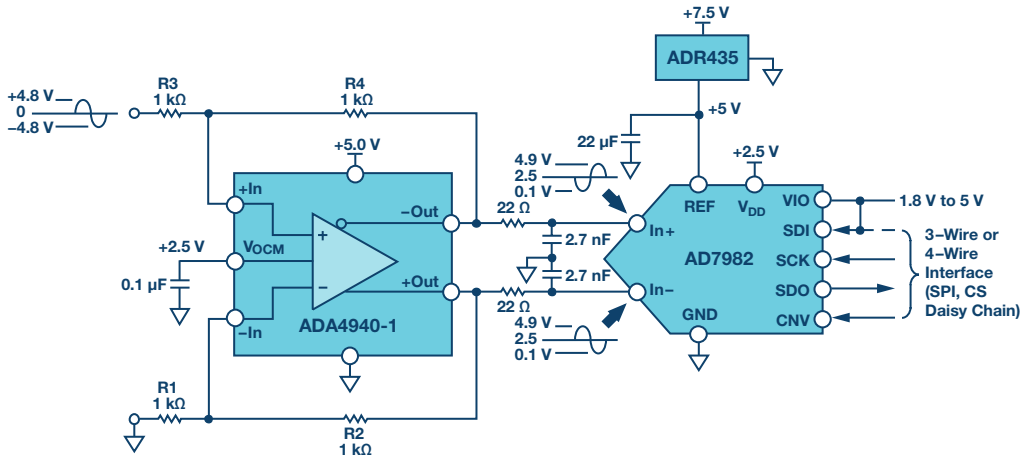

Figure 6. Low power, single-ended to differential, 18-bit, 1 MSPS data acquisition signal chain (simplified schematic: all connections and decoupling not shown).

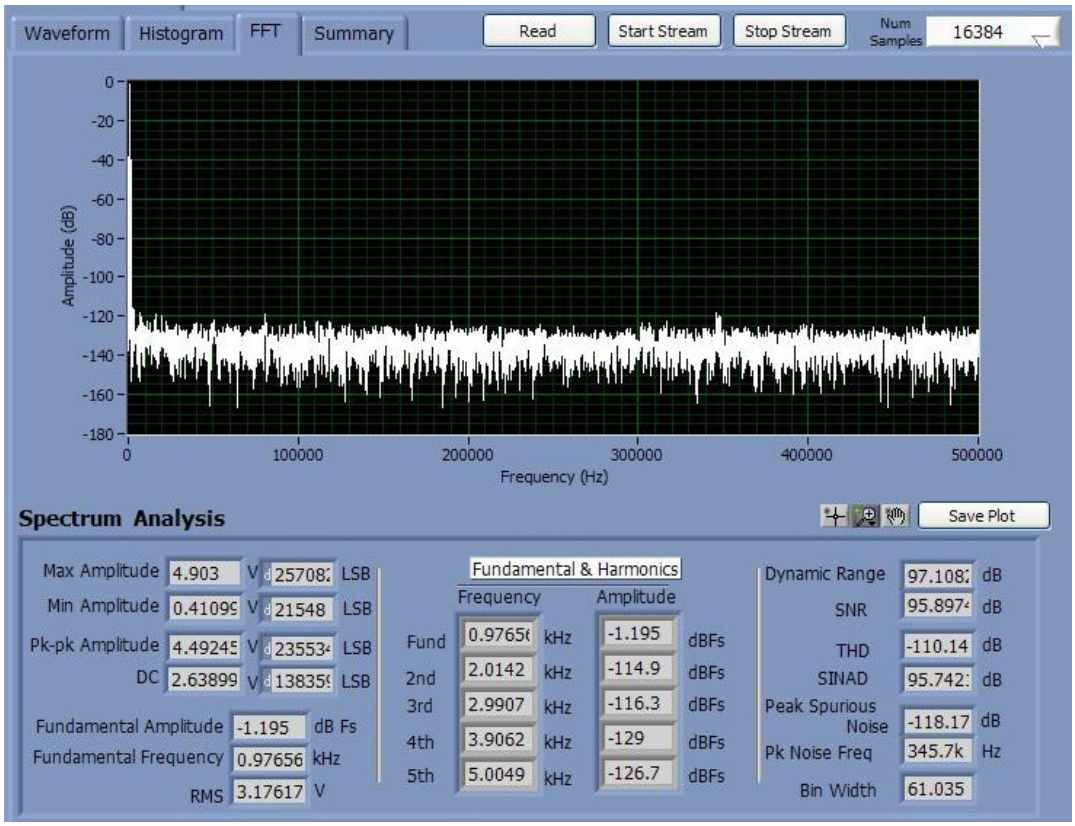

Figure 7. FFT plot, f_{IN} = 1 kHz, F_S = 1 MSPS (ADA4940-1 configured as a single-ended to differential driver).

with the throughput as shown in Figure 8, making the ADC well suited for both high and low sampling rates even as low as a few Hz. This feature enables very low power consumption for battery-powered portable instruments. The reference voltage of the ADC can be set independently of the supply voltage (V_{DD}) that dictates the input full-scale range of the ADC. In this case, the 5 V reference voltage for the AD7982 is applied externally on the REF pin from the ADR435 precision band gap reference, which operates from an on-board 7.5 V supply and dissipates typically 4.65 mW.

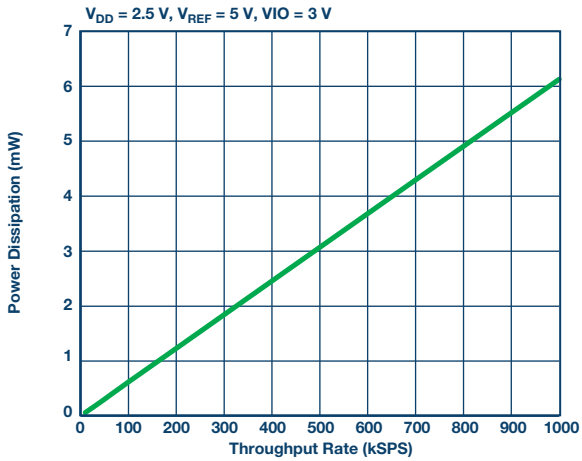

Figure 8. AD7982 power dissipation vs. throughput.

The ADA4940-1 operates from a 5 V single supply and dissipates typically 6.25 mW. Its outputs swing from 0.1 V to 9 V with a 2.5 V common-mode and accommodate a full-scale input to the ADC. Its rail-to-rail outputs can be driven to within 0.1 V of each power rail with a minimal degradation in ac performance for an audio frequency range.

The total power dissipation of the proposed data acquisition system including ADC driver, ADC, and the reference is typically around 17 mW.

Evaluation Setup

The simplified test setup using the Audio Precision SYS-2702 signal source, ADA49xx-1 EVAL-BRDZ, EVAL-AD7982SDZ PulSAR AD7982 evaluation board and EVAL-SDP-CB1Z system demonstration platform connected together is shown in Figure 9. A PC with Windows 7 equipped with a USB port is used to run the AD7982 PulSAR evaluation software for all the tests above.

It is important to scrutinize the noise, bandwidth, settling time, input and output headroom/footroom, and power requirements when selecting an ADC driver for driving the SAR ADC for a given application. The proposed 18-bit data acquisition signal chains for single-ended and fully differential input signal configurations presented here achieve optimized performance, only dissipating around 17 mW total power and saving board space for increased channel density by eliminating an additional analog signal conditioning stage. The alternative low power precision signal chain using the ADA4940-1 is ideal for driving the 16-bit, 1 MSPS/500 kSPS differential PulSAR ADCs AD7915/AD7916, which are drop-in replacements for the AD7982 and achieve optimized performance for space constrained applications. For more information on recommended amplifiers for driving the high resolution precision PulSAR ADCs, refer to the Analog Devices ADC Driver Selection Guide. For designing differential amplifier circuits, download the free and easy to use intuitive Analog Devices DiffAmpCalc™ tool.

Reference

Ardizzoni, John and Jonathan Pearson. *"'Rules of the Road' for High Speed Differential ADC Drivers." Analog Dialogue,* Vol. 43, No. 2, 2009.

About The Author

Maithil Pachchigar is an applications engineer in the Instrumentation, Aerospace, and Defense business unit at Analog Devices in Wilmington, MA. He joined ADI in 2010 and focuses on the precision ADC product portfolio and customers in the instrumentation, industrial, healthcare, and energy segments. Having worked in the semiconductor industry since 2005, he has published numerous technical articles, application notes, and blogs. He received an M.S.E.E. degree from San Jose State University in 2006 and an M.B.A. degree from Silicon Valley University in 2010. He can be reached at *maithil.pachchigar@analog.com.*

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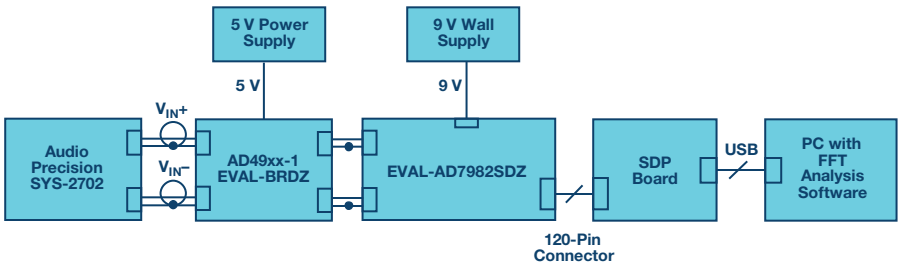

Figure 9. Evaluation setup functional block diagram.

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