Computer Architecture

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Problem:

Build CPU based on following requirements:

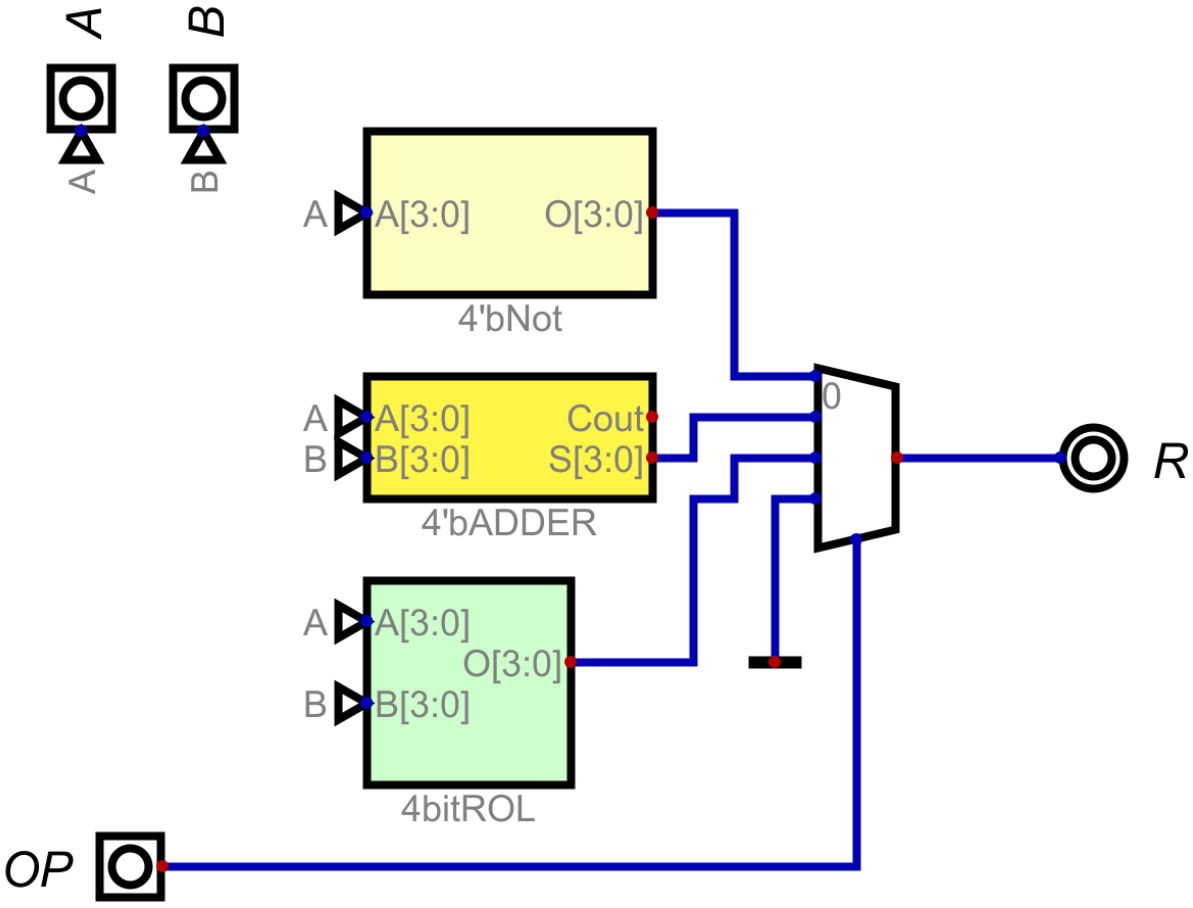
1. **Word Size of CPU = 4**
2. **ALU Operations = NOT, ADD, ROL**
3. **Register Number = 4**
4. **Size of RAM = 8**
5. **Word size of ISA and RAM = 15**
6. **CPU Instructions = Register Mode, Immediate Mode , JMP, JNE**

Solution:

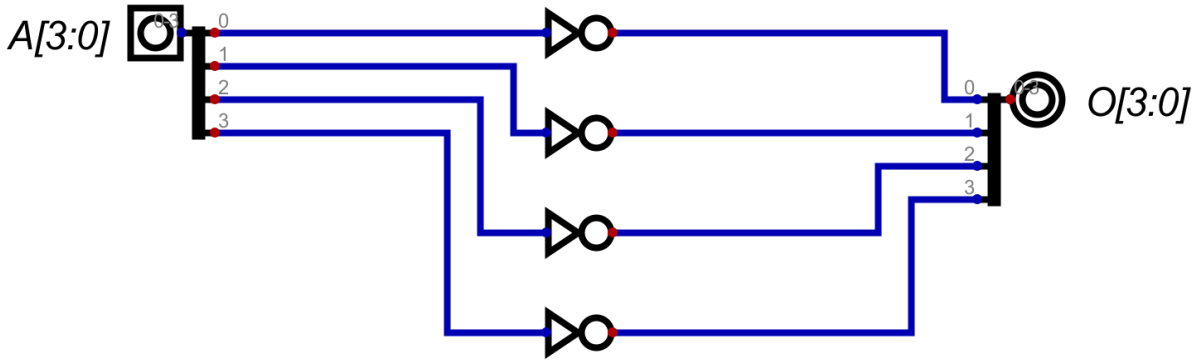
Simulator Design:

1. **ALU Circuit (Top to Bottom all circuits):**

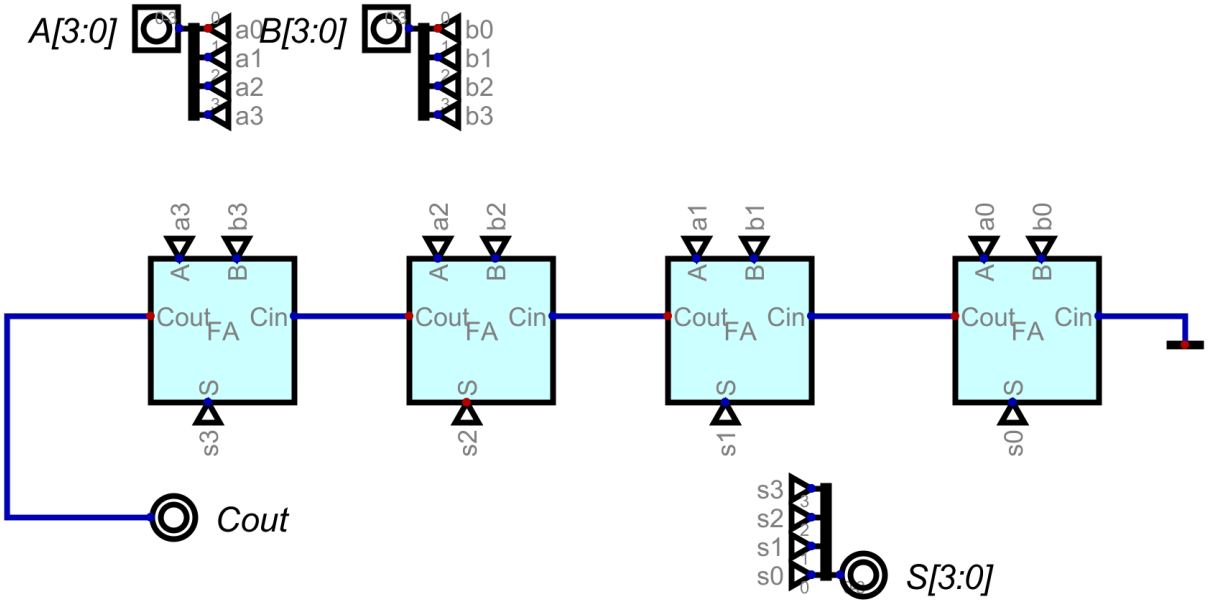
I. 4 bit ALU



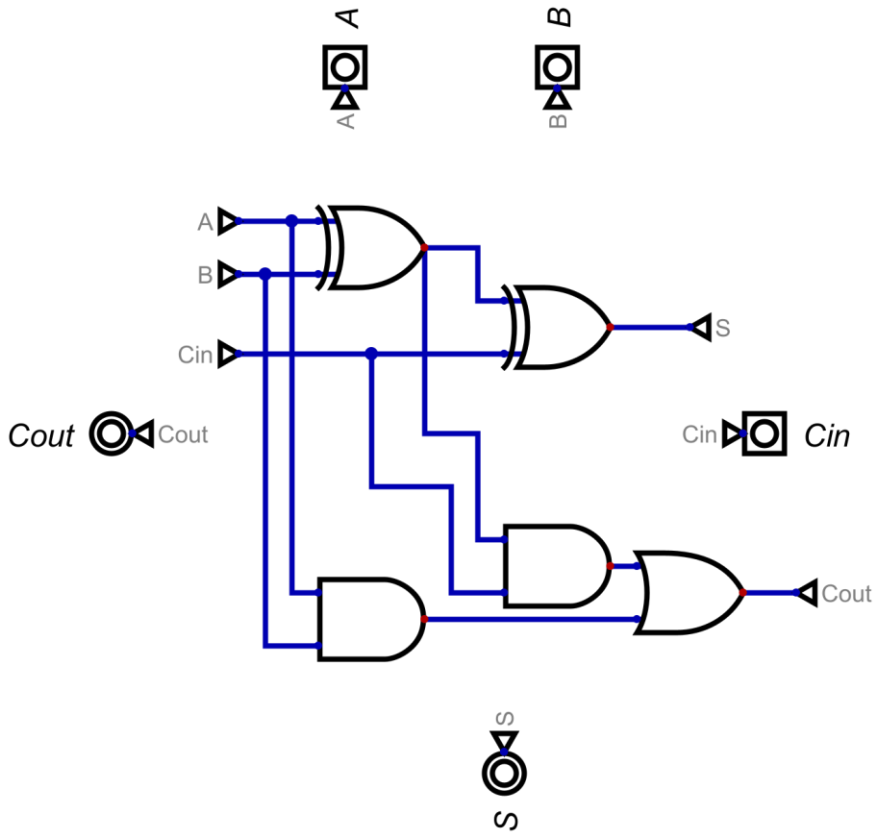
II. 4 bit NOT



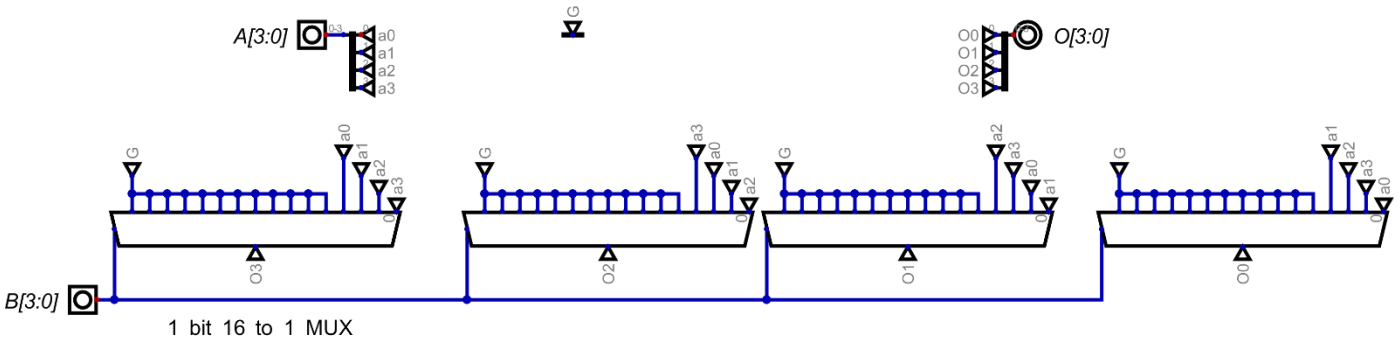
III. 4 bit Adder



a. 1 bit Adder

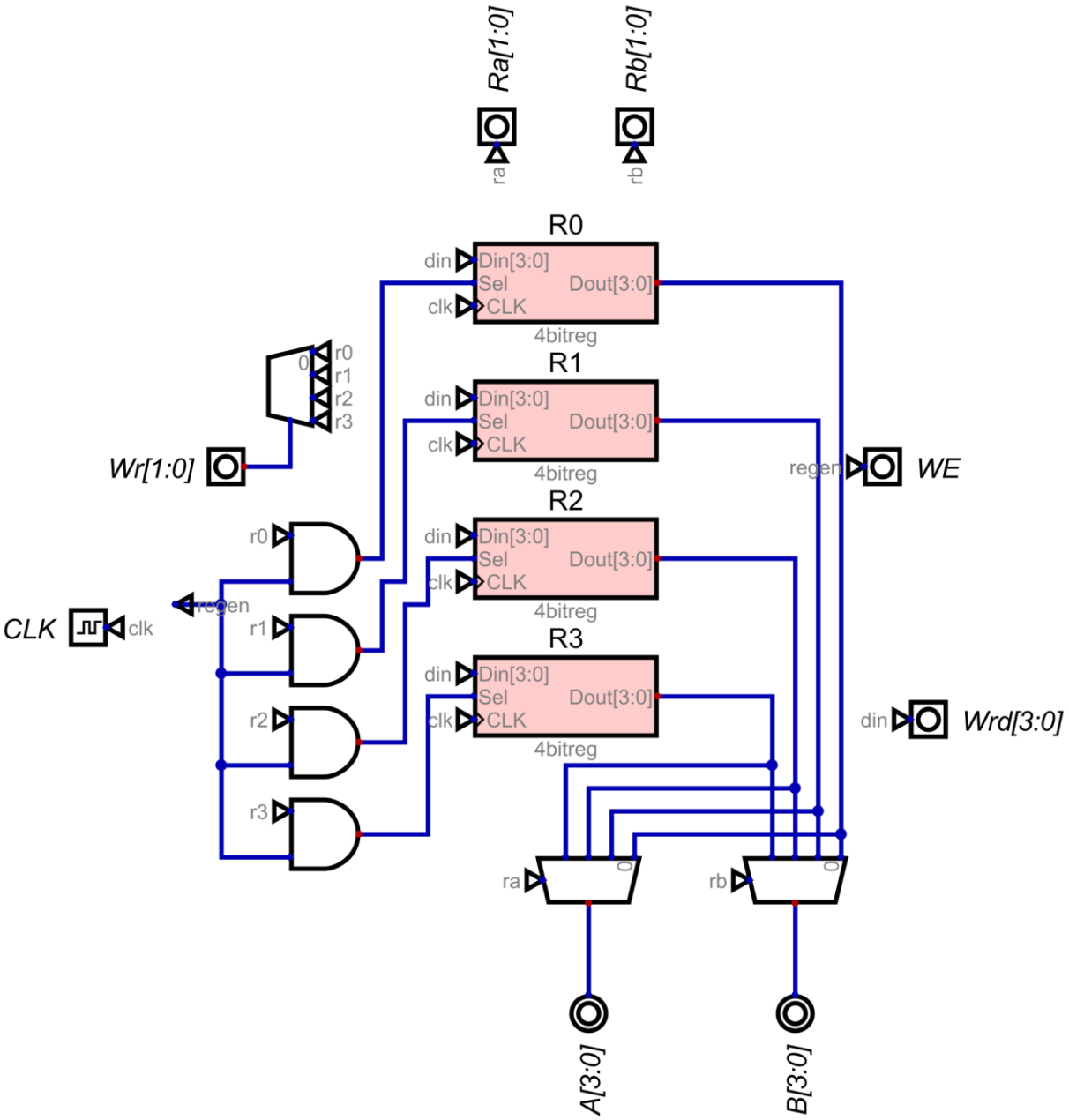


IV. 4 bit ROL

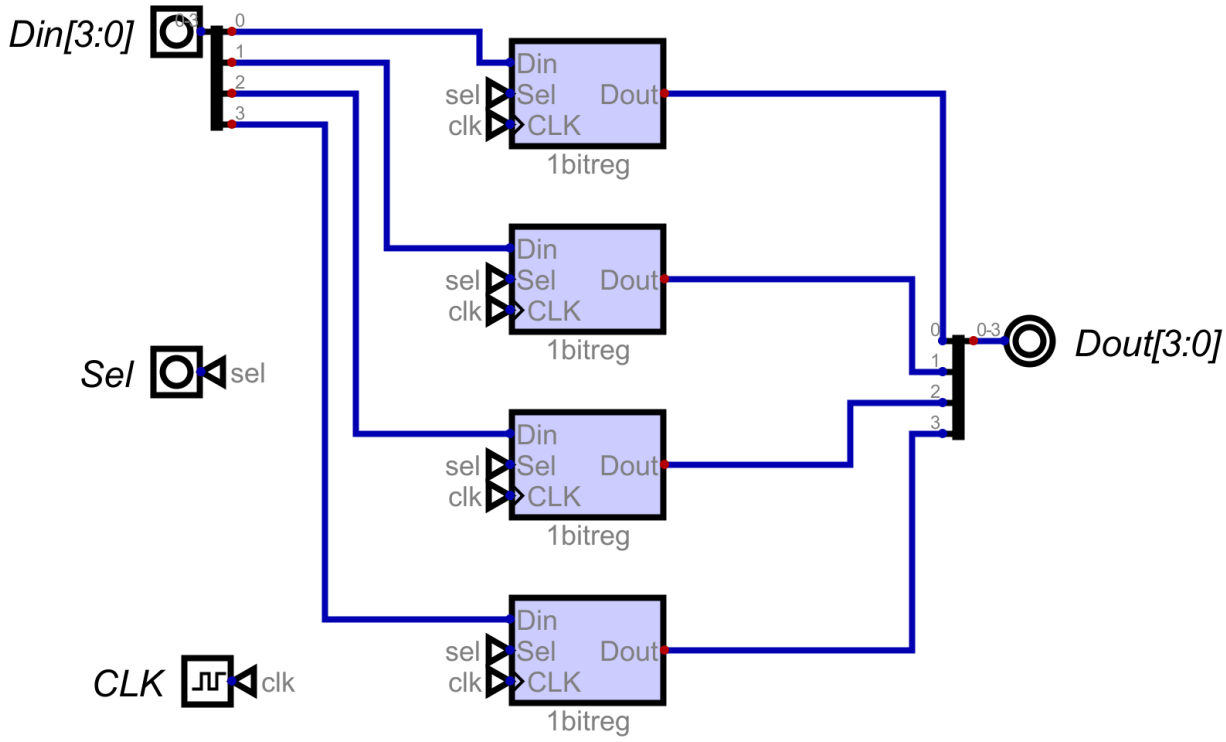


2. Register Set Circuit (Top to Bottom all circuits):

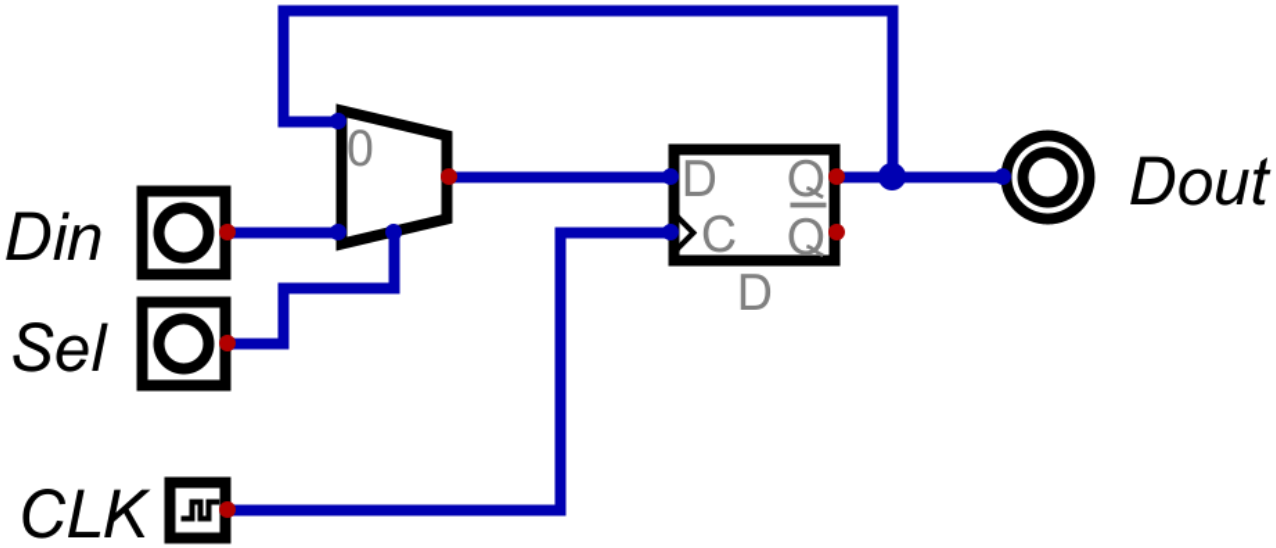
I. 4 bit Register Set


Ra[1:0]
Rb[1:0]
ra
rb
R0
din
Din[3:0]
Sel
Dout[3:0]
clk
CLK
4bitreg
R1
R2
R3
0
r0
r1
r2
r3
Wr[1:0]
regen
WE
CLK
clk
Wrd[3:0]
A[3:0]
B[3:0]

II. 4 bit Register

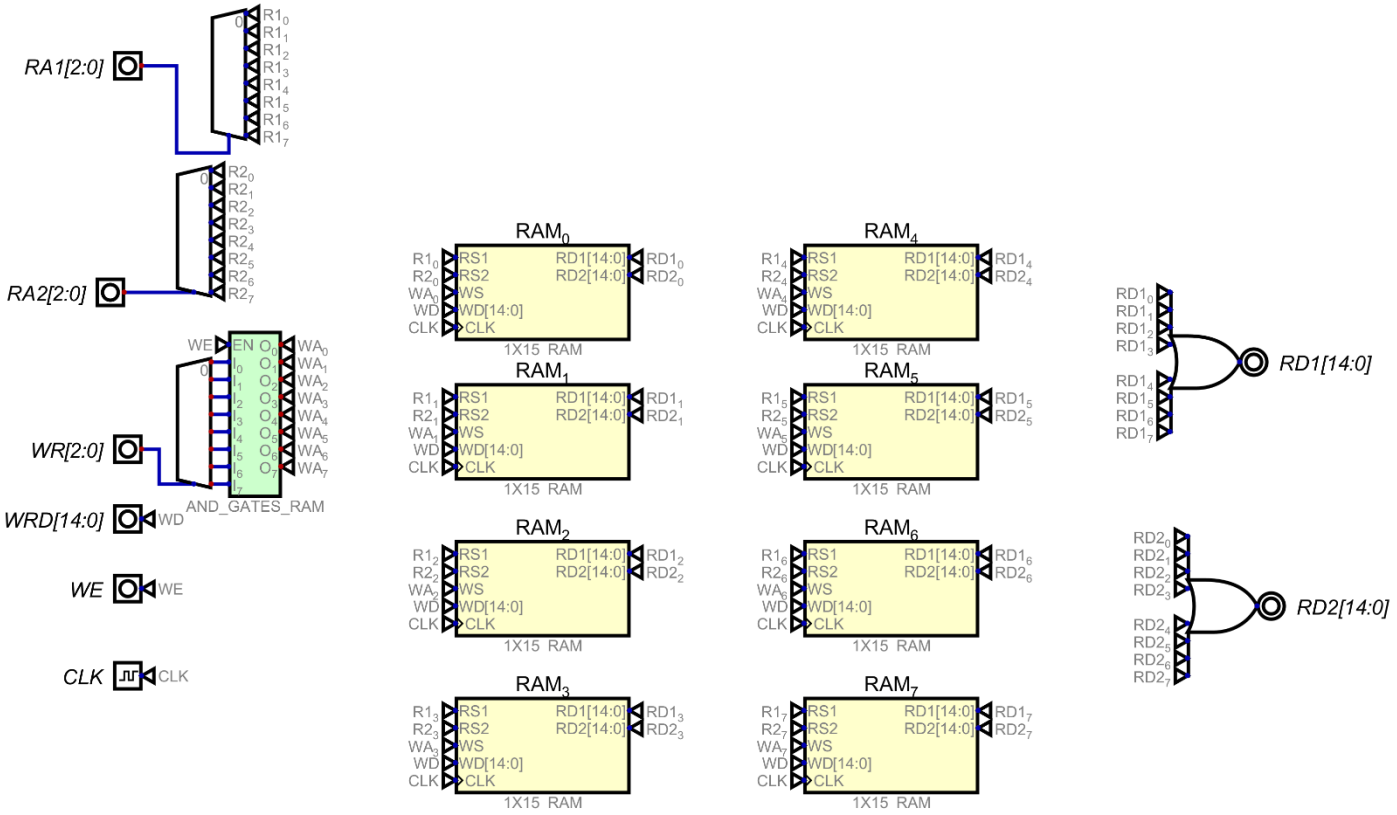


III. 1 bit Register

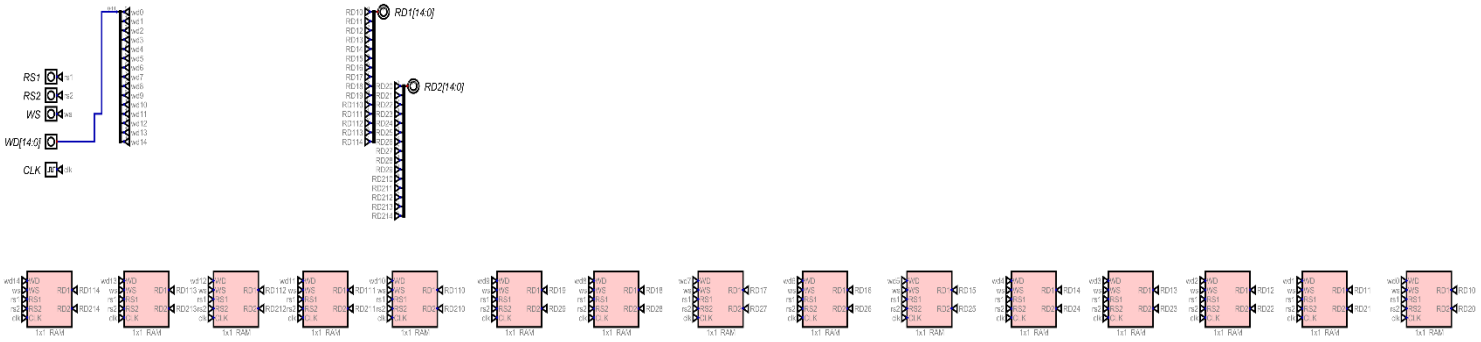


3. RAM Circuit (Top to Bottom all circuits):

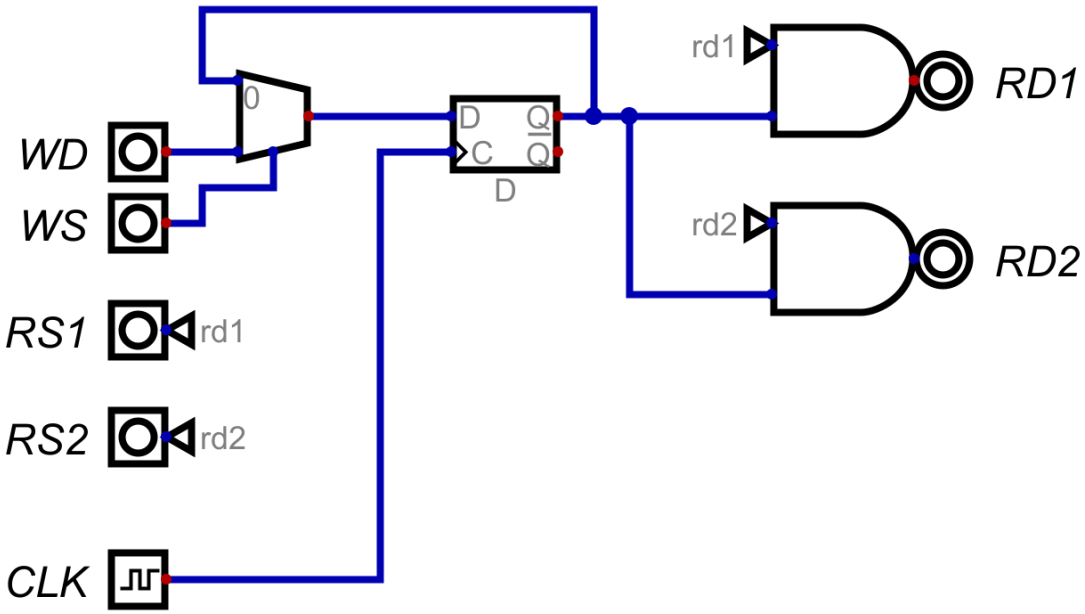
I. 8 x 15 RAM



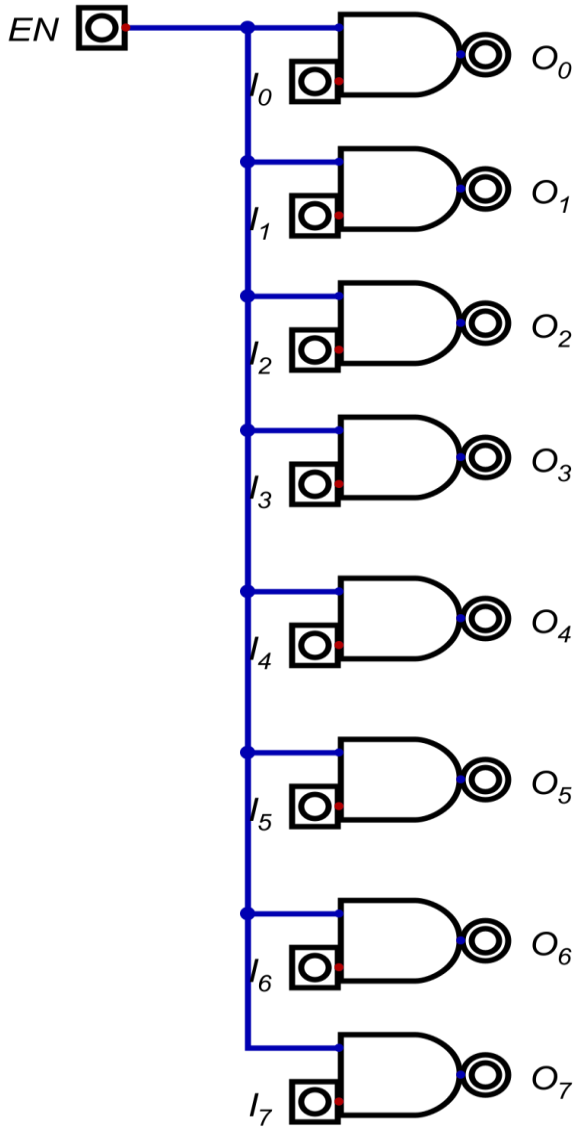
II. 1x15 RAM



III. 1x1 RAM



IV. AND_GATES_RAM



4. ISA

Register Mode(Type of OP 00) : 2 bit(type of OP)+2bit(OP)+2bit(Reg1)+2bit(Reg2) + 7bit (Don't Care)
Immidiate Mode(Type of OP 01) : 2 bit(type of OP)+2bit(OP)+2bit(Reg1)+4bit(Imm value) + 5bit (Don't Care)
Jump Mode(Type of OP 10) : 2 bit(type of OP)+2bit(OP)+3bit(Jump Address)+8 bit (Don't Care)
OP(00): NOT , OP(01):ADD , OP(11):ROL
OP(00): JMP , OP(01):JNE

JNE START
100100100000000

ADD R1,0101
010101010100000
JMP ADD1
100000100000000

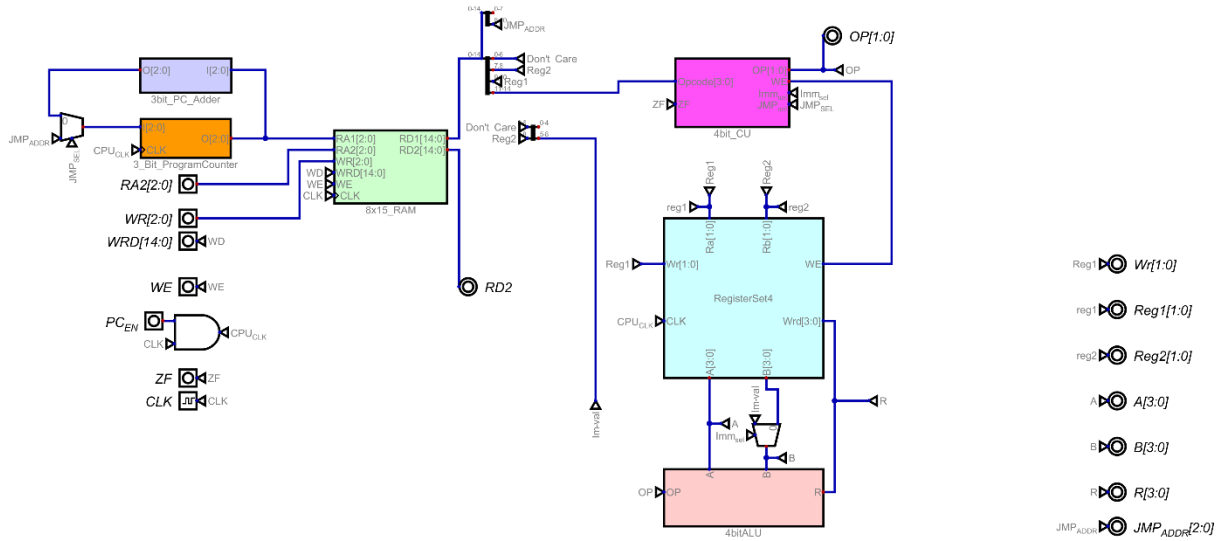
5. CPU (Top to Bottom all circuits):

I. CPU

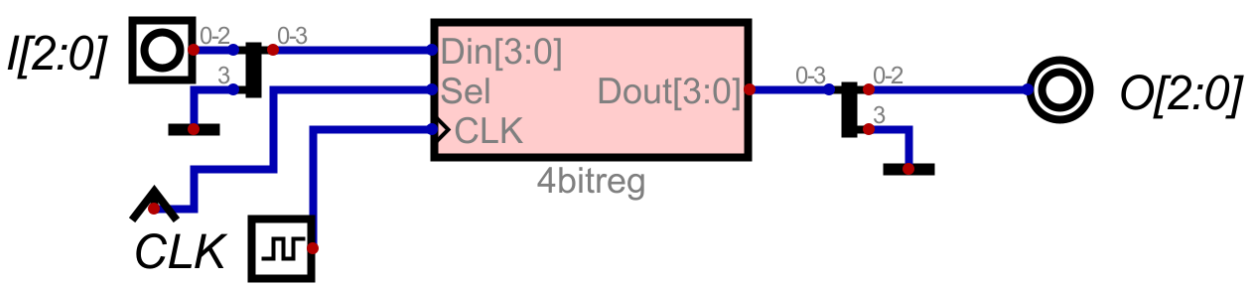
Register Mode(Type of OP 00) : 2 bit(type of OP)+2bit(OP)+2bit(Reg1)+2bit(Reg2) + 7bit (Don't Care)
Immidiate Mode(Type of OP 01) : 2 bit(type of OP)+2bit(OP)+2bit(Reg1)+4bit(Imm value) + 5bit (Don't Care)
Jump Mode(Type of OP 10) : 2 bit(type of OP)+2bit(OP)+3bit(Jump Address)+8 bit (Don't Care)
OP(00): NOT , OP(01):ADD , OP(11):ROL
OP(00): JMP , OP(01):JNE

JNE START
100100100000000

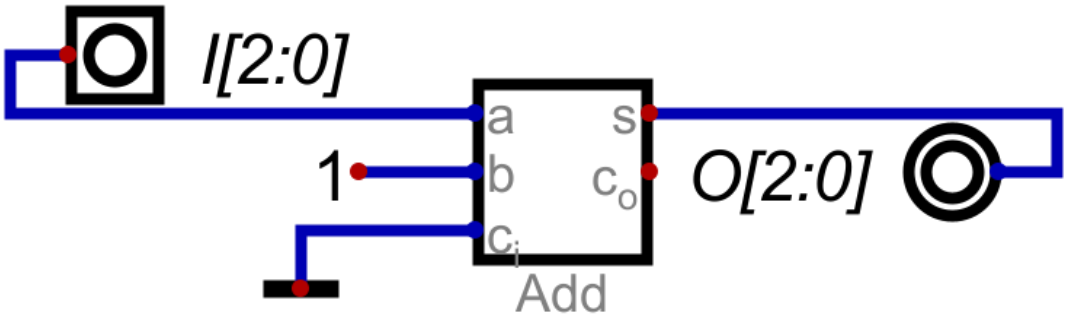
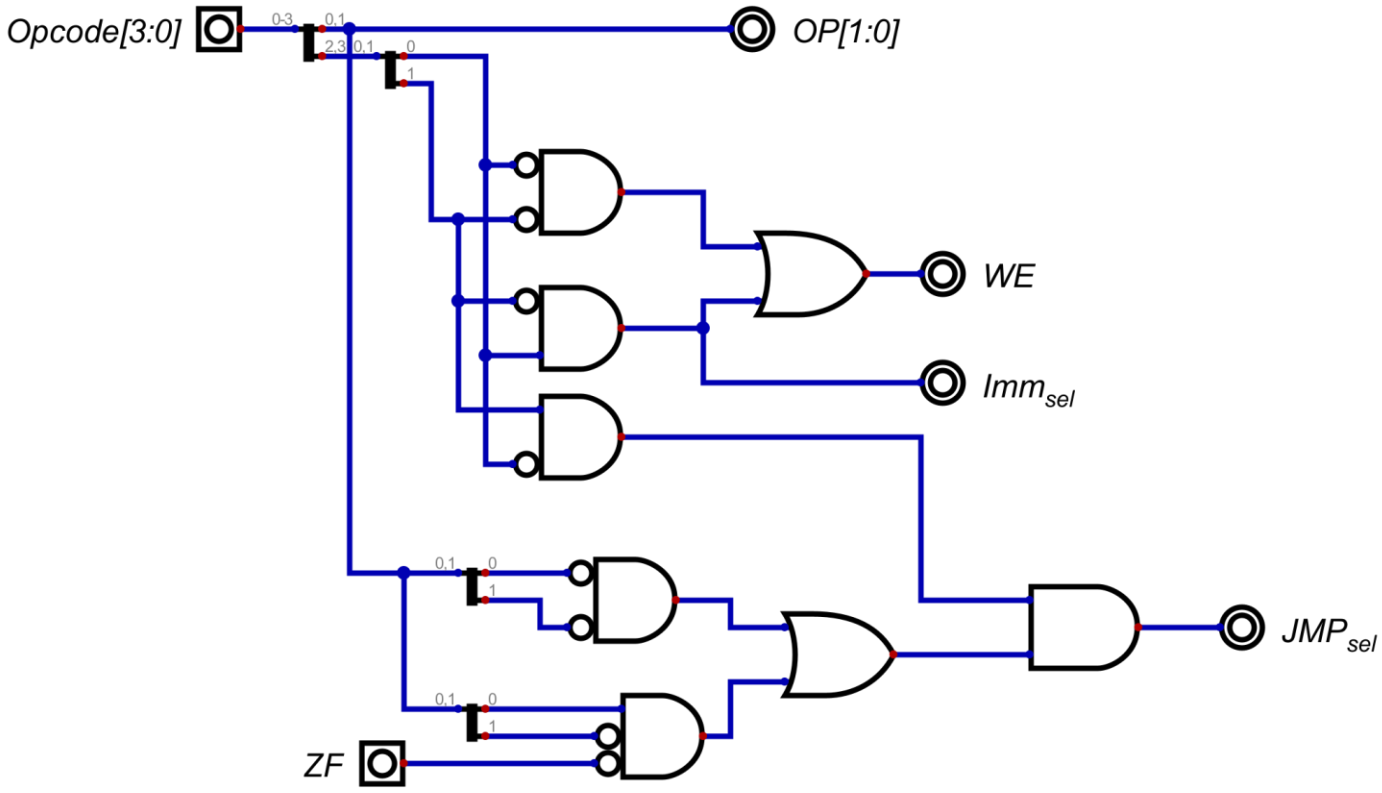
ADD R1,0101
010101010100000
JMP ADD1
100000100000000



II. 3 bit Program Counter



III. 3 bit PC Adder



IV. 4 bit CU