Notes
30/ 05/ 2021

R Type Instruction

32 bits instruction

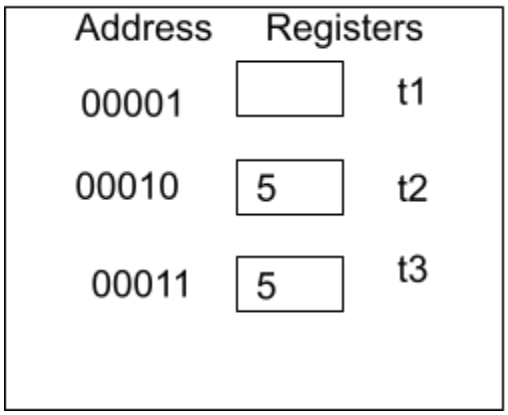
opcode	rs	rt	rd	shamt	funct
31: 26 6 bits	25:21 5 bits	20:16 5 bits	15:11 5 bits	10:6 5 bits	5:0 6 bits

Example:

add $t1, $t2, $t3

Each of registers t2 and t3 contains value 5. After add operation register t1 holds the value 10.

Consider the following register file



How is this instruction stored in the Instruction Memory?

000000	00010	00011	00001	00000	100000

Opcode for R type is 0

Highlights:
In this class we learned the operation of datapath for implementing an R-type instruction as shown in Figure 4.19.
We talked about 3 components of the datapath in details: PC, Instruction Memory, Register file
Reference: Section 4.1 - 4.4

Notes
31/ 05/ 2021

Memory Reference Instructions: lw and sw

lw or sw

opcode	rs	rt	offset

31: 26	25:21	20:16	15:0
6 bits	5 bits	5 bits	16 bits

Opcode for lw is 35 and for sw is 43

Example:
lw $t1, 8 ($t2) // Register t2 holds the memory's base address and 8 is an offset value. 32 bit Data from the Memory location specified by the address ($t2 + 8) is loaded to register t1.

100011	00010	00001	0000000000001000

add $t1, $t3, $t1 // Value of register t1 is added to the value of register t3 and the output is stored in register t1.

000000	00011	00001	00001	00000	100000

sw $t1, 6 ($t2) // // Register t2 holds the memory's base address and 8 is an offset value. 32 bit Data from register t1 is stored to the Memory location specified by the address($t2 + 8) .

101011	00010	00001	0000000000001000

Highlights:
In this class we learned the operation of datapath for implementing an memory reference (I-type) instruction as shown in Figure 4.20.
Also we looked at the control unit and discussed the clock cycle requirement of the execution.

Reference: Section 4.1 - 4.4