CSE 315: Bonus Assignment

Submitted by:

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Question:

Interface 80486 in such a way that there is 32k x 16 EPROMs starting from 80045H, 64k x 16 RAMs starting from 40045H, and 8 I/O devices connected at consecutive ports starting from 100458H.

EPROM Interfacing:

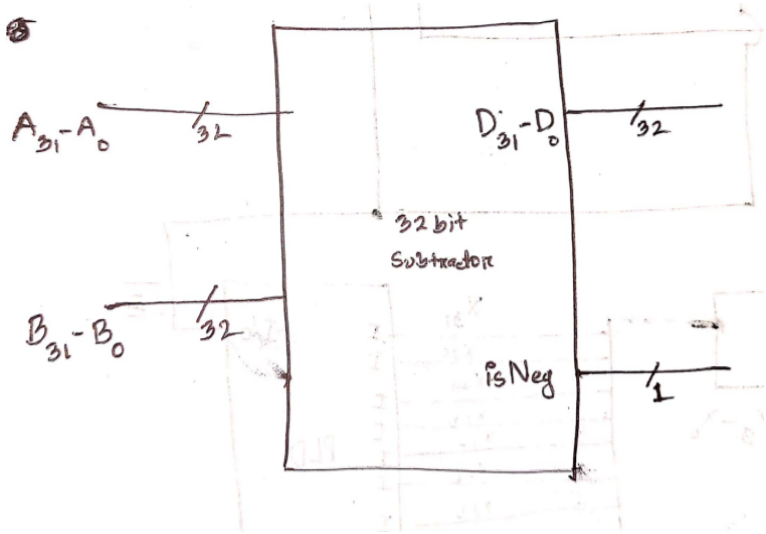
We will use 32k x 16 EPROMs. As 80486 has 32 data pins, we need to use 2 EPROMS.

80486 has 32 address pins and our selected EPROM has 15 address pins.

EPROMs address space is, [00080045H, 000A0044H].

However, to scale it properly, we will use a subtractor circuit (32 bit). The idea is to subtract 00000045H from the address.

Subtractor circuits block diagram is,



Here D=A-B;
isNeg=1, if A < B (in unsigned interpretation)
isNeg=0, if A ≥ B.
We need to use 2 EPROMs. As EPROM is read-only, we do not need to do banking. All 32 data pins will be read, and we may extract this later for reading certain bits.
Here X equals the result after subtracting 00000045H from the address. So, its valid range is [00080000H, 0009FFFFH].

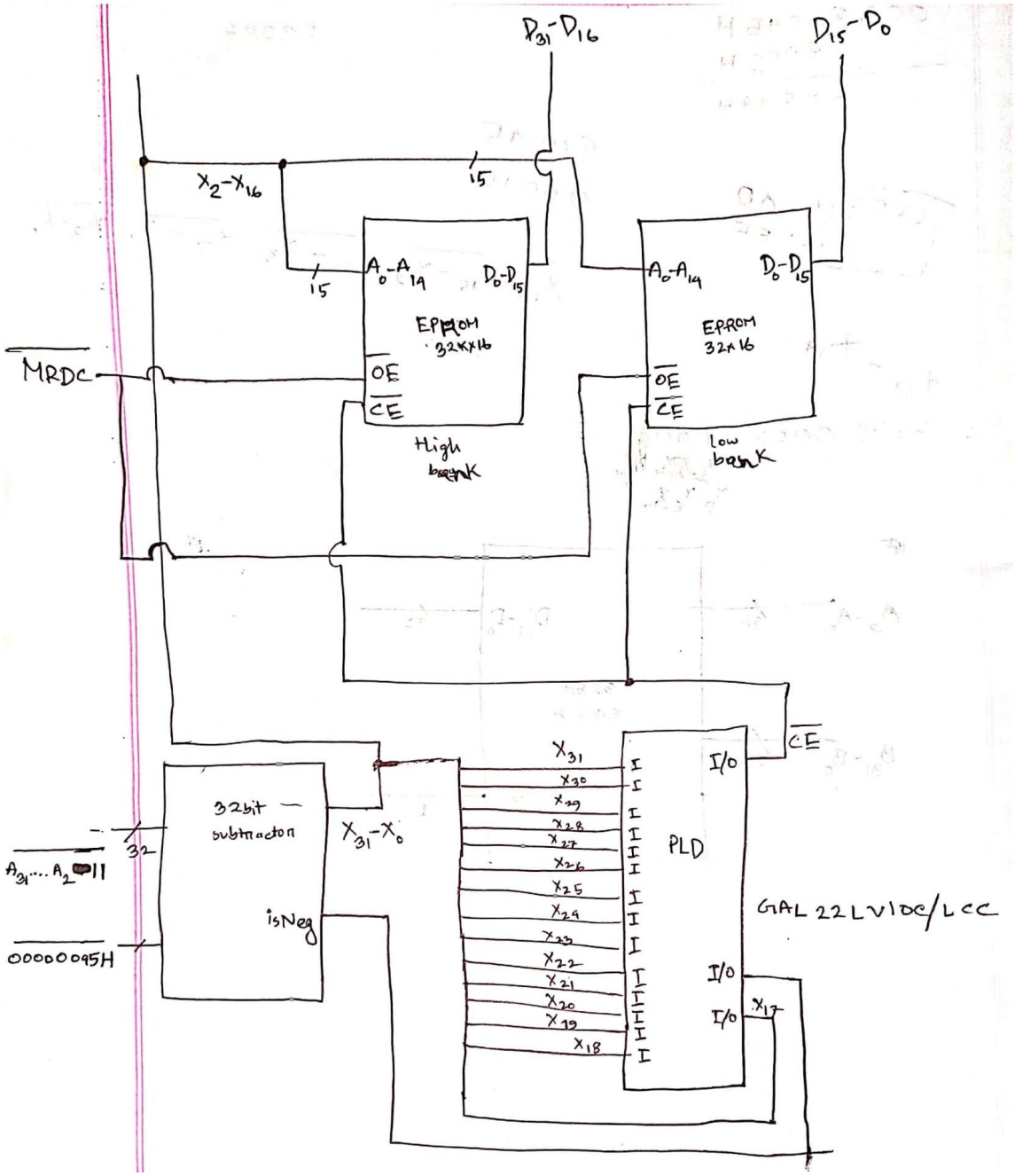


Figure: 32k*16 EPROM interfacing with 80486

X31 - X20, X18, X17 must be 0.
X19 must be 1.
X16-X2 can be anything.
X must be non-negative too, after subtracting. So, isNeg should be 0.
This checking will be done by PLD to generate Chip Enable.
Here, PLD logic is,
CE' = X31 or X30 or X29 or X28 or X27 or X26 or X25 or X24 or X23 or X22 or X21 or (not X19) or X18 or X17 or isNeg

SRAM Interfacing:
We will use 64k x 16 RAMs. We need to use 2 such devices.
Its address space will be [00040045H, 00080044H].
Just like before, we will scale it by subtracting 00040045H from the address. Let the result be X. So, the valid range of X is [00000000H, 0003FFFFH].

Here, X2-X17 can be anything, this will be fed to SRAMs address pins.
X18-X31 is fixed. All of them must be 0.
X must not be negative after subtracting.

64k*16 SRAM specification: It has 16 address pins, 16 data pins. It has chip enable, read enable. It has upper byte enable (UB') and lower byte enable (LB'), to specify which byte we want to write to.

PLD logic is,
CE' = X31 or X30 or X29 or X28 or X27 or X26 or X25 or X24 or X23 or X22 or X21 or X20 or X19 or X18 or (isNeg).
WR3 = BE3 or MWTC
WR2 = BE2 or MWTC
WR1 = BE1 or MWTC
WR0 = BE0 or MWTC

Note that,
WR3 will be fed to left (high bank) RAM's UB'.
WR2 will be fed to left (high bank) RAM's LB'.
WR1 will be fed to right (low bank) RAM's UB'.
WR0 will be fed to right (low bank) RAM's LB'.

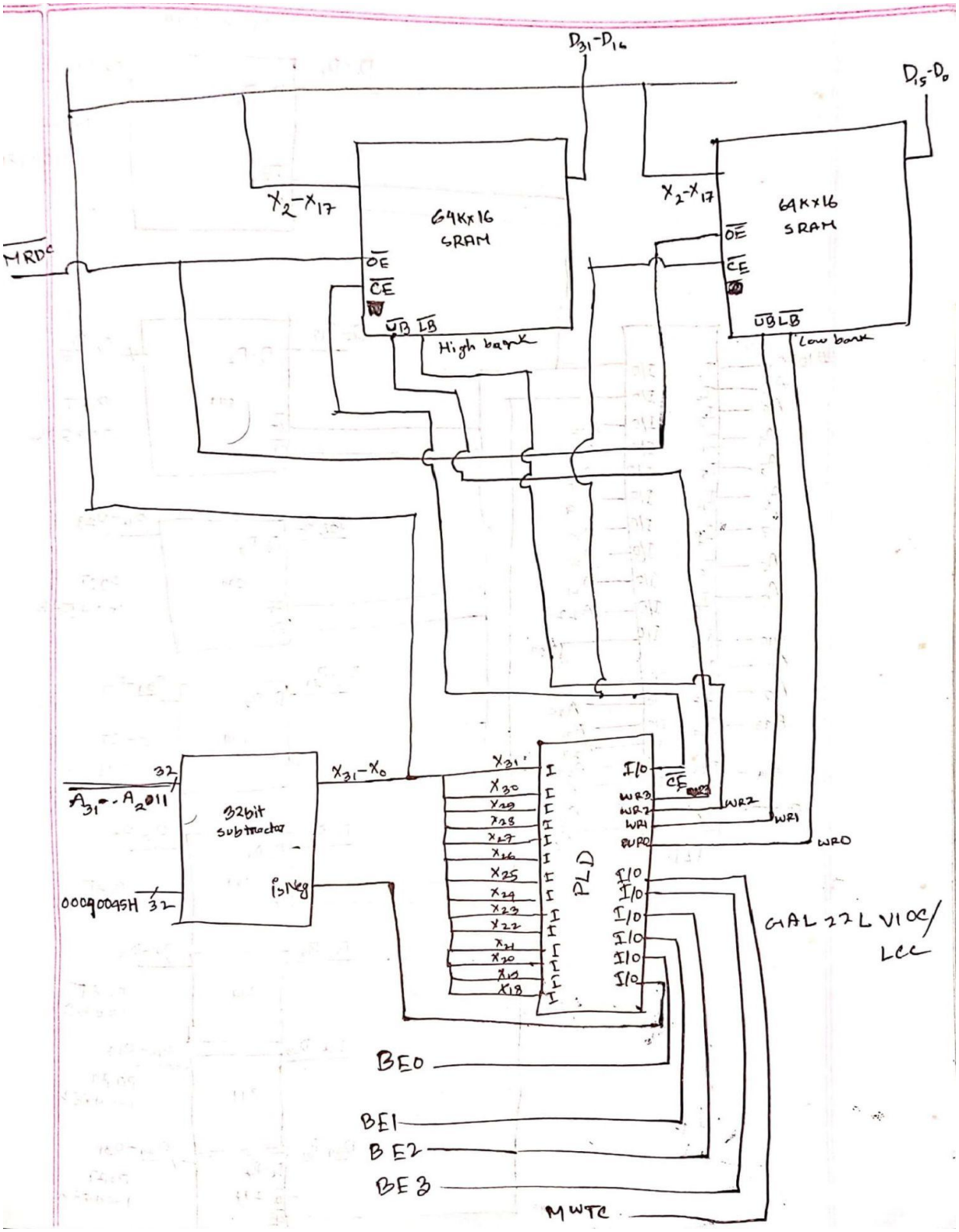


Figure: 64k*16 RAM interfacing with 80486

I/O interfacing:

8 I/O devices connected at consecutive ports starting from 100458H.

So, the range is [100458H,10045FH].

So, only A2 differs.

$\overline{A_{31}A_{30}\ldots A_3} = \overline{00000000000100000000010001011}$

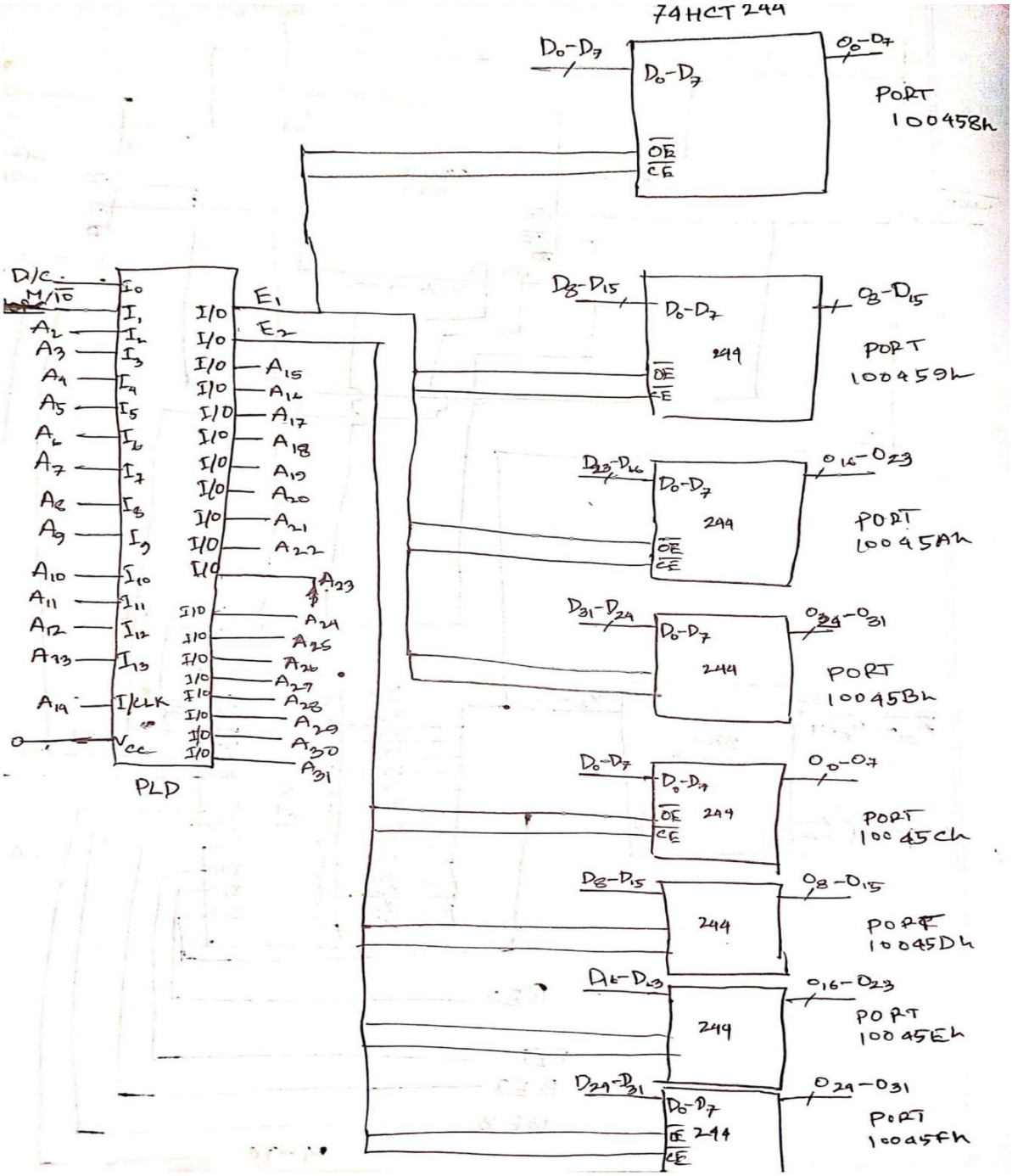


Figure: 8 I/O devices interfacing with 80486

PLD logic,

E1= M/IO’ or (not D/C’) or A31 or A30 or A29 or A28 or A27 or A26 or A25 or A24 or A23 or A22 or A21 or (not A20) or A19 or A18 or A17 or A16 or A15 or A14 or A13 or A12 or A11 or (not A10) or A9 or A8 or A7 or (not A6) or A5 or (not A4) or (not A3) or **A2**

E2= M/IO’ or (not D/C’) or A31 or A30 or A29 or A28 or A27 or A26 or A25 or A24 or A23 or A22 or A21 or (not A20) or A19 or A18 or A17 or A16 or A15 or A14 or A13 or A12 or A11 or (not A10) or A9 or A8 or A7 or (not A6) or A5 or (not A4) or (not A3) or **(not A2)**

[If PLD does not exist with 31 inputs and 2 outputs, we need to use 74LS32 to OR some of them first, then to feed the PLD]