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Q.

(a) YES

(b) We will get correct ADCH value. But may get wrong ADCL value. As a result, resulting adc value may be [corrected adc value-3, corrected adc value +3]. Because, in 2 bit, maximum decimal 3 can be represented, so,
resulting voltage is in range $[V - 3*\text{step size}, V + 3*\text{step size}]$ where V = voltage if we counted ADCL correctly.

Here are 2 worst case. One when resulting adc value has ~~LSBs~~ last two bit $\overline{00}$ and actual adc value has last two bits $\overline{11}$. Other one is opposite-vice-versa.

(c) Here, for this ADMUX value,
Reference voltage = 2.56 V, right adjusted.

As $\overline{ADMUX_{4\ldots0}} = 10000$

positive differential input = Input of ADC0 = 2V
negative differential input = Input of ADC1 = 1V
GAIN = 1

$$\therefore ADC = \left\lfloor \frac{(V_{pos} - V_{neg}) \times \text{Gain} \times 512}{V_{REF}} \right\rfloor = \left\lfloor \frac{(2-1) \times 1 \times 512}{2.56} \right\rfloor$$

$$= (200)_{10}$$

$$= (11001000)_2$$