RESEARCH ARTICLE

DC Series Arc Fault Detection and Self-Extinguishing Method With Power Stage Design of Module Level Power Electronics

HWA-PYEONG PARK[ID][1], **(Member, IEEE), MINA KIM**[2], **(Member, IEEE), AND SUYONG CHAE**[ID][3], **(Senior Member, IEEE)**

[1]School of Electronic Engineering, Kumoh National Institute of Technology (KIT), Gumi 39177, South Korea
[2]Department of Electrical Engineering, Hanbat National University, Daejeon 34158, South Korea
[3]Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang 37673, South Korea

Corresponding author: Suyong Chae (sychae@postech.ac.kr)

ABSTRACT A DC optimizer can achieve maximum power generation for each photovoltaic (PV) panel. However, it increases the possibility of arc fault between the PV panel and DC optimizer. This paper proposes the DC series arc fault detection and self-extinguishing method for the DC optimizer through the power stage design. The proposed method adopts the characteristics of series arc fault resistance according to the PV current. The relationship between the arc fault resistance and PV current is theoretically analyzed according to the parameter change of the passive components. The power stage analysis can determine the passive parameters, such as the inductor and capacitor, to detect faults and self-extinguish. The simulation and experimental results employing the boost-type DC optimizer verify the performance of the proposed arc fault detection and extinguishing method.

INDEX TERMS DC systems, arc fault, arc discharge, DC/DC converter, fault diagnosis, fault detection, photovoltaic, power filter.

I. INTRODUCTION

The power generation utilizing renewable energy sources, such as photovoltaics (PV) and wind turbines, has become a major trend in achieving carbon neutrality [1], [2], [3], [4], [5]. With the increase in the number of PV systems, various standards and requirements have been introduced with increasing interest in their safety and reliability owing to several electrical problems [6], [7], [8], [9], [10], [11]. PV systems exhibit DC series arc fault conditions caused by loose connectors, damaged cables, and cracked solder joints. The National Electrical Code (NEC) requires the installation of an arc-fault detection device (AFDD) in all PV systems over 80 V [12]. In addition, Underwriters Laboratories (UL) invented the UL 1699 B standards to guarantee

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the performance of AFDDs [13]. Therefore, a DC-arc fault detection device is necessary to guarantee the safety of PV systems.

DC arc faults can occur in both series and parallel fault conditions. A parallel- arc fault can easily be detected by a large change in the current [14], [15]. However, a series arc fault only has a small current variation because it operates as a small series resistance in a power line or connector. Therefore, a series-arc fault is more challenging than a parallel-arc fault. DC series arc fault detection devices require high precision and fast detection speed because the energy losses in the arc fault are converted into heat energy. Various DC arc fault detection methods have been introduced. In [16], [17], and [18], a DC series arc fault detection method based on time-domain analysis was evaluated by utilizing the voltage and current information, respectively. In [19], [20], and [21], frequency-domain analysis was
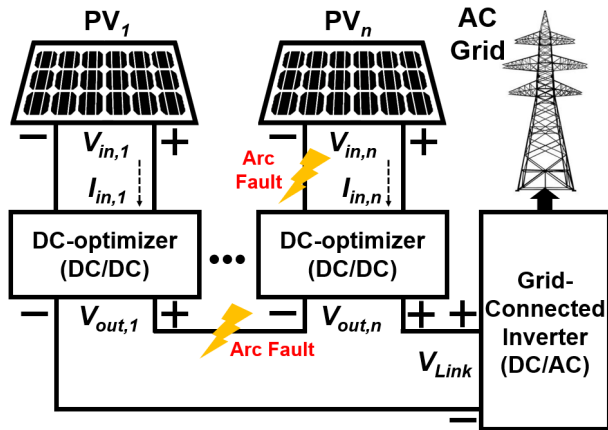
FIGURE 1. PV systems with series connected DC optimizers.

performed utilizing the measured PV current to determine the arc fault characteristics. In [22], [23], and [24], hybrid methods employing time- and frequency-domain analyses were introduced to improve detection precision. In [25], [26], and [27], fault detection methods adopting artificial intelligence were developed utilizing the fault data. Previous research has adopted measured current information through signal processing methods such as fast Fourier transform, wavelet transform, and artificial intelligence. These previous methods employed arc impedance variability but did not utilize the characteristics of arc resistance. The proposed concept is based on the operating characteristics of the arc resistance [28], [29], [30]. An arc fault operates as a negative resistance that induces an open-circuit condition with a small current. In [16], the control algorithm of power converter was introduced to maximize the arc resistance with small current flow to detect and extinguish the arc fault condition. It requires the power flow control of DC optimizer, which reduces the power generation of PV systems.

Recently, PV systems have focused on improving the power generation efficiency. A module level power electronics (MLPE) was employed to obtain the maximum power of each PV panel while overcoming partial shading, as presented in Fig. 1 [31], [32], [33]. The parallel connected MLPEs, such as micro-inverter and differential power processing units, require the isolated type DC/DC converter to transfer the DC power to AC grid [34], [35], [36], [37]. It can achieve the effective voltage conversion according to the turn ratio and electrical isolation, which can improve the reliability of converter with reduction of ground current issue. However, the transformer reduces the power conversion efficiency, power density, and cost-effectiveness compared with non-isolated converter. The series connected MLPEs are described as independent input source and output series connected systems with DC/DC converter, as shown in Fig. 1, which can use the isolated and non-isolated DC/DC converter. It increases the DC link voltage level with series connected output voltage of DC/DC converter. Also, it shares the output current of converter at the DC link side, such as DC current collector [38], [39], [40]. The non-isolated converters, such as non-inverting
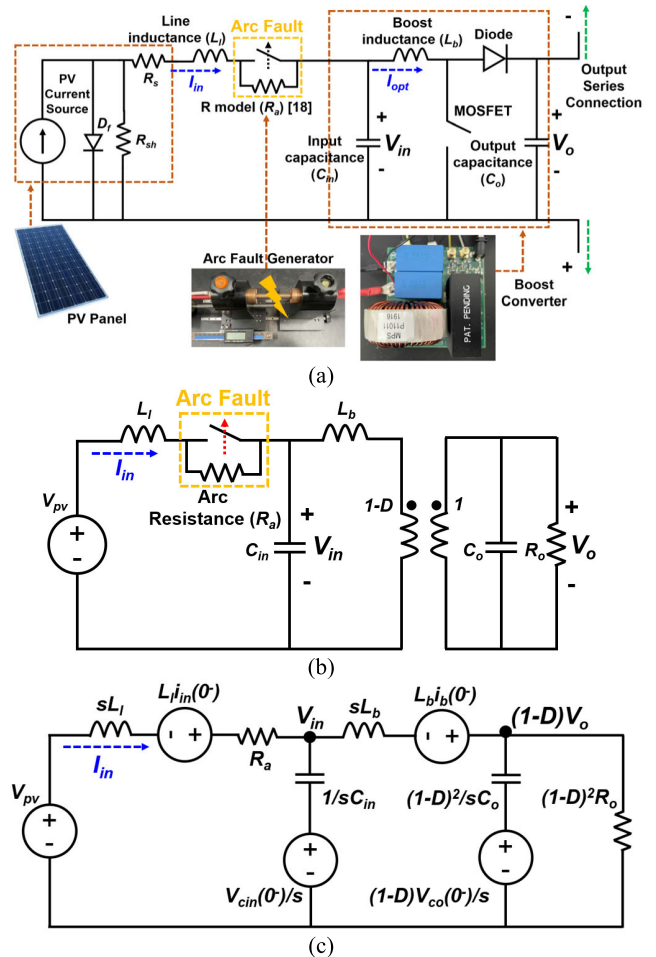

FIGURE 2. Configuration of PV panel and DC optimizer: (a) switching model, (b) average model, and (c) s-domain analysis.

buck-boost and boost, were widely used in the industrial fields, such as Solar-Edge. It has weakness in the current leakage to protective earth, since it has non-isolation between low voltage DC and AC grid. The target application of this paper is the PV systems using the series connected MLPEs. The PV systems with MLPEs increase the system complexity with an increase in the DC–DC converter. This structure increases the possibility of arc fault conditions between PV panel and the DC optimizer. This increases the number of AFDDs between the PV panel and the DC optimizer, which results in poor cost-effectiveness.

This paper investigates the design methodology of DC optimizer to achieve the series arc fault detection and natural fault extinguishing capability, which focused on the arc fault condition between PV panel and power converter. The series arc fault condition operates as the addition of arc resistance in the power line or connector, which causes a dynamic response of the power converter. The operational characteristics of power converter is analyzed according to the arc resistance and passive components. From those analysis, the proper power stage design can clarify the arc fault characteristics, which can detect the fault condition with simple algorithm. Also, it can naturally extinguish the arc fault condition.
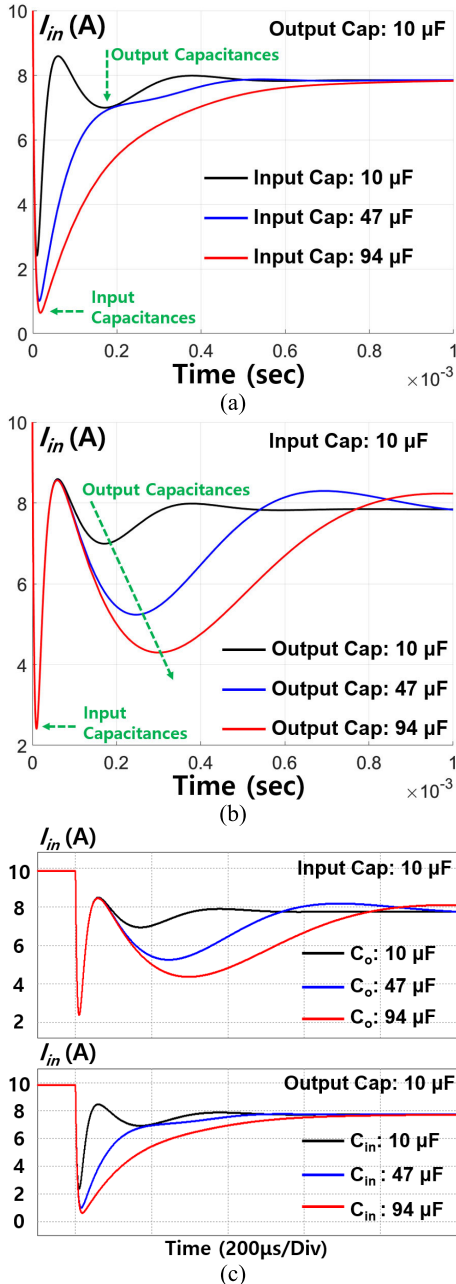
FIGURE 3. Analysis of dynamic operation: (a) C_{in} Variation, (b) C_o Variation, and (c) PSIM Simulation results.

This paper can achieve the series arc fault detection capability with only power stage design, which does not require the additional power control of converter. It minimizes the power loss for the series arc fault detection, which is the contribution of this paper. The experimental results using the 800-W prototype DC optimizer can verify the performance of arc fault detection and extinguishing with proposed power converter design methodology.

II. OPERATIONAL CHARACTERISTICS ACCORDING TO ARC FAULT CONDITION

The configuration of DC optimizer with considerations of arc fault condition is described in Fig. 2 (a). The boost
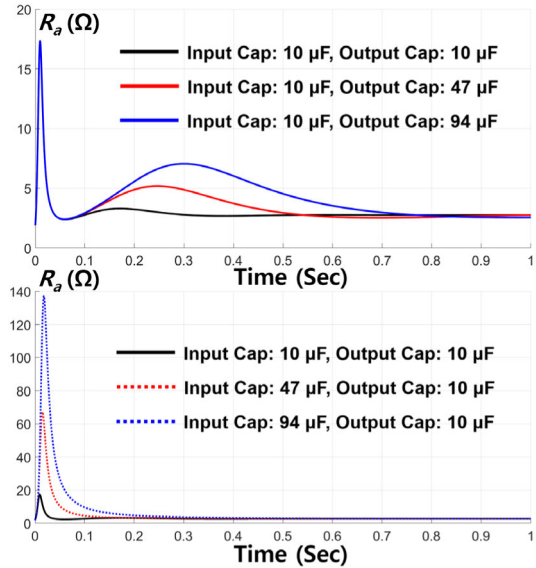

FIGURE 4. Arc resistance trajectory according to the input and output capacitance.

TABLE 1. Specification for dynamic analysis.

Parameter	Value
PV voltage (V_{pv})	80 V
Load (R_o)	8 Ω
Input Capacitor (C_{in})	10 μF, 47 μF, 94 μF
Output Capacitor (C_o)	10 μF, 47 μF, 94 μF
Line Inductor (L_l)	10 μH
Boost Inductor (L_b)	460 μH
Arc Resistance (R_a)	2.65 Ω

converter contains the line and boost inductance, input and output capacitance, single MOSFET, and diode. The series arc fault condition operates as the addition of arc resistance in the power line. In the previous research, the arc resistance models, such as Cassie, Mayr, and Stokes-Oppenlander models, have been derived with the V-I relationship at the fault condition. The arc resistance has the negative resistance characteristics. This paper uses Stokes-Oppenlander incident energy equation to analyze the arc resistance (R_a) [28].

$$R_a = \left(20 + 0.534 Z_g\right) / \left(I_{in}^{0.88}\right) \quad (1)$$

where Z_g is the arc gap (mm) and I_{in} is the input current value. From (1), the small current can increase the arc resistance, which can induce the open circuit condition.

A. ANALYSIS OF DYNAMIC OPERATION

The series arc fault condition operates as the addition of arc resistance in the power line or connector, which induces the transient operation in the current. The average model of boost converter can describe the transient operation without the considerations of switching effect, as shown in Fig. 2 (b) [36]. Also, the average model can be converted to s-domain circuit to analyze the fault transient condition, as shown in Fig. 2 (c).
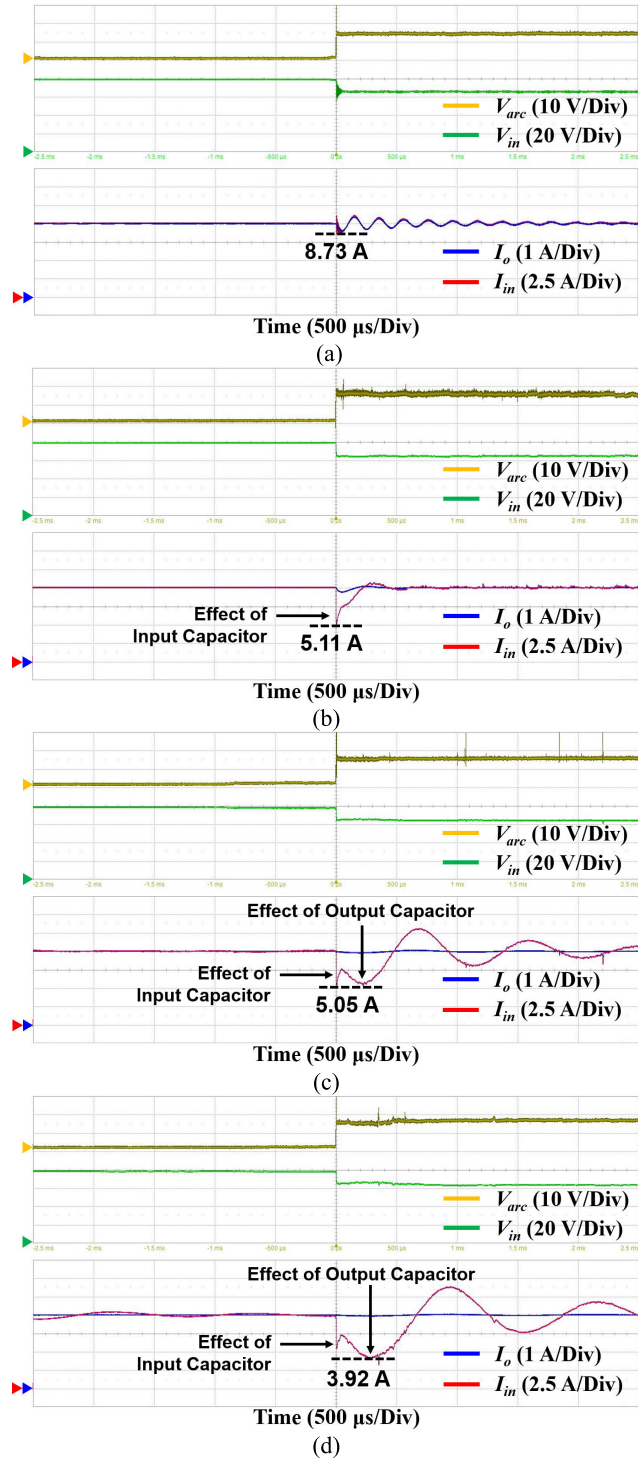
FIGURE 5. Minimum input current according to C_O: (a) 1 μF of C_{in} and C_O, (b) 10 μF of C_O and 10 μF of C_{in}, (c) 47 μF of C_O and 10 μF of C_{in}, (d) 94 μF of C_O and 10 μF of C_{in}.

Assuming R_a is the fixed value, the node voltage of V_{in} and $V_o{'}(= V_o(1\text{-}D))$ can be obtained as follows:

$$\frac{V_{pv}/s + L_l i_{ini} - V_{in}}{sL_l + R_a} - \frac{V_{in} - V_{cini}/s}{1/sC_{in}} - \frac{V_{in} + L_b i_{bi} - V_o{'}}{sL_b} = 0 \quad (2)$$
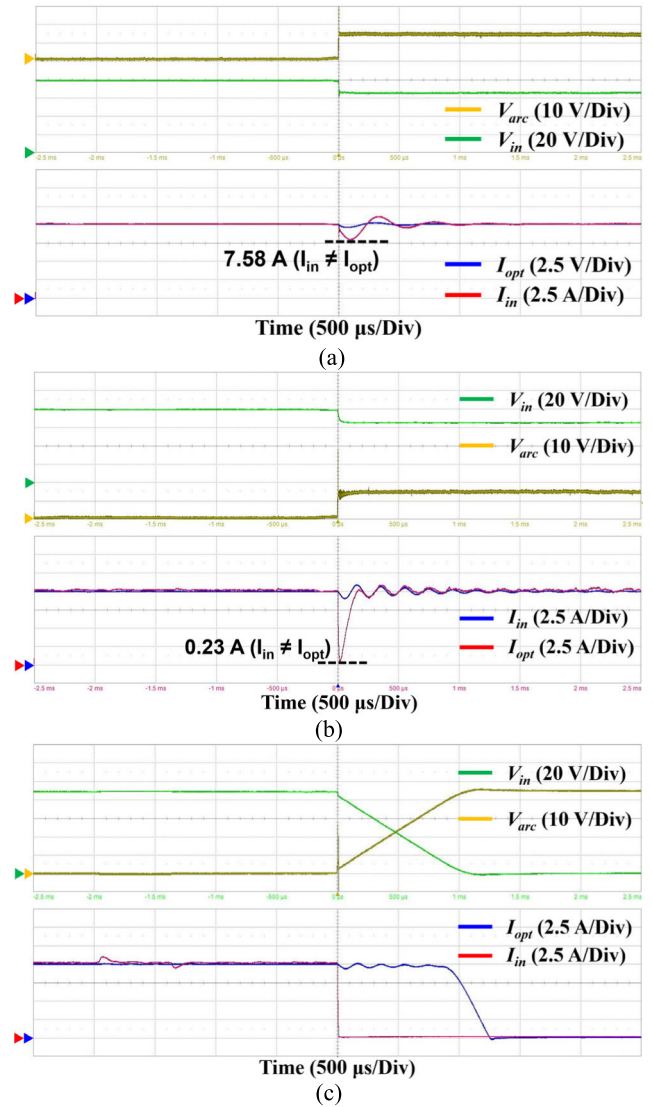

FIGURE 6. Minimum input current with C_{in}: (a) 10 μF of C_O and 1 μF of C_{in}, (b) 10 μF of C_O and 47 μF of C_{in}, (c) 10 μF of C_O and 94 μF of C_{in}.

$$\frac{V_{in} - L_b i_{bi} - V_o{'}}{sL_b} - \frac{V_o - V_{coi}'/s}{1/sC_o} - \frac{V_o{'}}{R_o{'}} = 0 \quad (3)$$

where V_{pv} is the PV panel voltage, L_l and L_b are the inductance of line and boost converter, C_{in} and $C_o{'}$ $(= C_o/(1-D)^2)$ are the input and output capacitance, R_a is the arc resistance, i_{ini} and i_{bi} are the initial current of L_l and L_b, and V_{cini} and V_{coi}' $(= V_{coi}(1-D))$ are the initial voltage of C_{in} and $C_o{'}$. From (2) and (3), V_{in} are calculated as follows:

$$V_{in} = A/B \quad (4)$$

$$A = \frac{sL_b}{sL_l + R_a} + s^2 C_{in} L_b + \frac{sL_b + s^2 L_b C_o{'} R_o{'}}{R_o{'} + sL_b + s^2 L_b C_o{'} R_o{'}} \quad (5)$$

$$B = \frac{R_o{'} L_b i_{bi} + sL_b R_o{'} C_o{'} V_{coi}'}{R_o + sL_b + s^2 L_b C_o R_o{'}} + \frac{sL_b \left[V_{pv}/s + L_s i_{ini} \right]}{sL_l + R_a}$$
$$+ sC_{in} L_b V_{cin}\left(0^-\right) + L_b i_b \left(0^-\right) \quad (6)$$
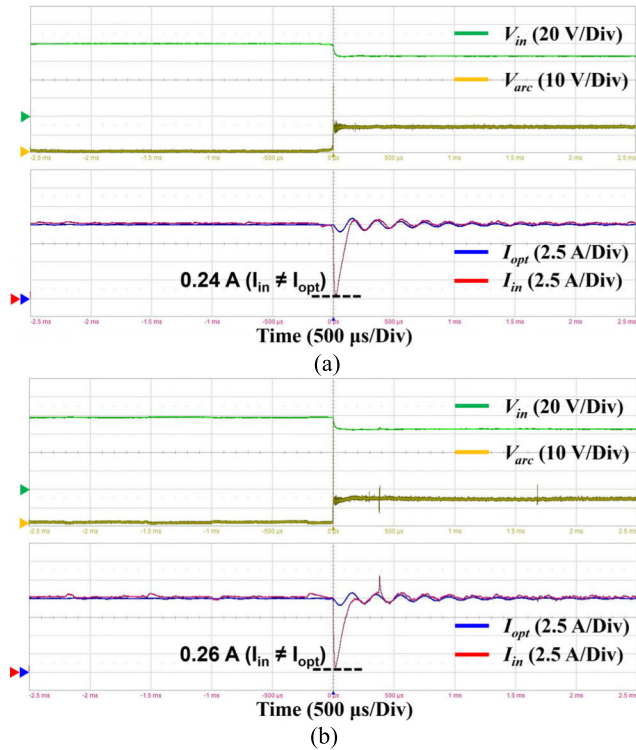
FIGURE 7. Arc fault according to arc gap length at 10 μF of C_o and 47 μF of C_{in}: (a) 0.8 mm and (b) 2.5 mm.

TABLE 2. Simulation specification.

Case	Pulling Speed	Arc Gap	Mechanical Transient Duration	Electrical Transient Duration
1		0.8 mm	160 ms	
2	5 mm/s	1.1 mm	220 ms	Below 2 ms
3		2.5 mm	500 ms	

The input current can be derived as follows:

$$i_{in} = \frac{V_{pv}/s - L_l i_{in}\left(0^-\right) - V_{in}}{sL_l + R_a} \quad (7)$$

Table 1 shows the specification for theoretical analysis. Fig. 3 (a) and (b) shows the theoretical waveforms using MATLAB according to C_{in} and C_o, respectively. The increase of C_{in} and C_o reduces the input current at arc fault transient duration. Fig. 3 (c) shows the simulation results to verify the theoretical analysis. The increase of C_{in} is effective to reduce the input current compared with C_o. The trajectory of arc resistance is described in Fig. 4 for the fault transient duration. The large C_{in} and C_o increases the R_a. Also, C_{in} is more effective to achieve the high R_a compared with C_o. When the R_a is high enough, the fault condition can be naturally extinguished.

B. POWER STAGE DESIGN FOR FAULT DETECTION

In this paper, the C_{in} is designed to detect and extinguish the arc fault condition. To design C_{in} value, the voltage and
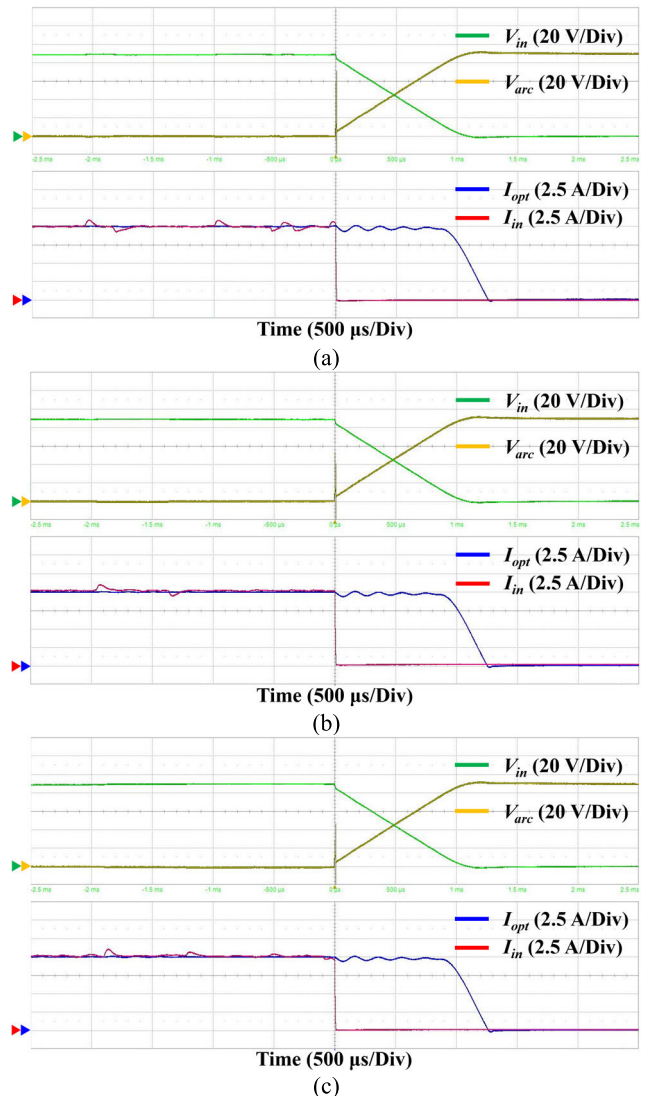

FIGURE 8. Arc fault characteristics according to the repeated tests at the same operating points: (a) Test #1, (b) Test #2, and (c) Test #3.

current equations using the time domain analysis can be derived, as follows:

$$v_{pv}\left(t\right) = L_l\left[di_{in}\left(t\right)/dt\right] + i_{in}\left(t\right)R_a + v_{in}\left(t\right) \quad (8)$$

$$i_{in}\left(t\right) = C_{in}\left[dv_{in}\left(t\right)/dt\right] + v_{in}\left(t\right)/R_o \quad (9)$$

From (8) and (9), the transient operation of $v_{in}(t)$ and $i_{in}(t)$ can be derived, as follows:

$$v_{in}\left(t\right) = A_1 e^{\left(\alpha_1 t\right)} + A_2 e^{\left(\alpha_2 t\right)} + V_{in,f} \quad (10)$$

$$i_{in}\left(t\right) = C_{in}\left(\alpha_1 A_1 e^{\left(\alpha_1 t\right)} + \alpha_2 A_2 e^{\left(\alpha_2 t\right)}\right) + v_{in}\left(t\right)/R_o \quad (11)$$

$$A_1 = V_d - A_2, \quad A_2 = -\alpha_1 V_d/\left(\alpha_2 - \alpha_1\right) \quad (12)$$

where α_1 and α_2 are the solution of (8) and (9), respectively, $V_{in,f}$ and $V_{in,i}$ are the final and initial input voltage, respectively, and V_d is $V_{in,i} - V_{in,f}$. From (11), the minimum input current for the arc fault transient duration can be derived,
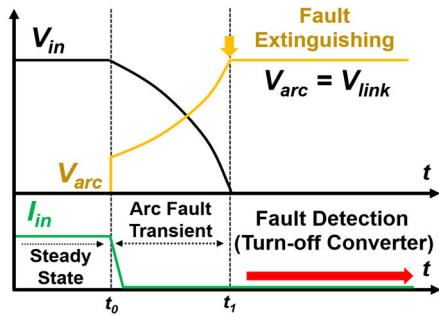
FIGURE 9. Theoretical operation of DC optimizer according to arc fault condition.
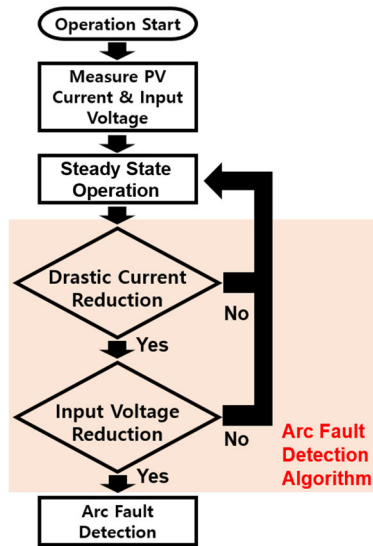

FIGURE 10. Flow chart for DC series arc fault detection and extinguishing.

as follows:

$$i_{in,\min} = C_{in}\left(\alpha_1 A_1 e^{(\alpha_1 \beta)} + \alpha_2 A_2 e^{(\alpha_2 \beta)}\right) + v_{in,\min}/R_o \quad (13)$$

$$\beta = -\log\left[(-T_1/T_2)/(\alpha_1 - \alpha_2)\right] \quad (14)$$

$$T_1 = C_{in}\alpha_1^2 A_1 + (\alpha_1 A_1)/R_o, \quad T_2 = C_{in}\alpha_2^2 A_2 + (\alpha_2 A_2)/R_o \quad (15)$$

From (13), the C_{in} can be derived to obtain the desired minimum input current, as follows:

$$C_{in} \geq \left(i_{in,\min} - v_{in,\min}/R_o\right)/\left(\alpha_1 A_1 e^{(\alpha_1 \beta)} + \alpha_2 A_2 e^{(\alpha_2 \beta)}\right) \quad (16)$$

From the desired minimum input current, the proper C_{in} can be determined with (16).

The input capacitance design is significant to detect the arc fault condition. Also, the large input capacitance is proper to achieve the fault detection capability, which required the minimum input capacitance design. In terms of power quality, the increase of input capacitance can be designed to minimize the input voltage ripple for improving the maximum power
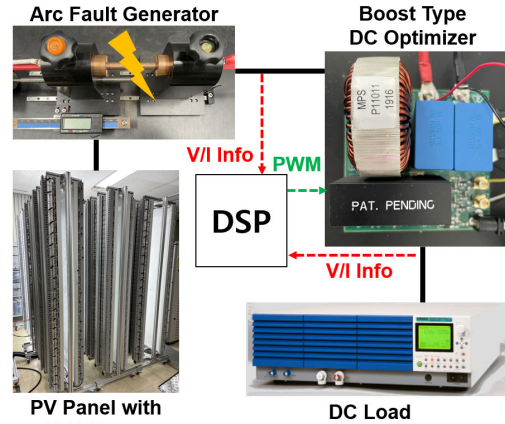

FIGURE 11. Experimental setup using prototype converter.

point tracking (MPPT), which can be derived as follows:

$$C_{in} \geq \frac{i_{cap}}{\Delta V_{ripple} 2\pi f_s} \quad (17)$$

However, the large capacitance increases the size of capacitor. Therefore, the minimum input capacitance should satisfy (16) and (17) to guarantee the series arc fault detection capability and input voltage ripple. The maximum capacitance is designed with considerations of the power density.

Fig. 5 and Fig. 6 show the experimental verification of input current variation according to the C_{in} and C_o. The arc fault generator makes various fault conditions with motor pulling. In this experiment, Table 2 shows the designed moving speed of electrode and its gap length. Fig. 5 shows the effectiveness of C_o for the fault transient duration. The increase of C_o reduces the input current to obtain the high R_a. However, the input current reduction is limited, which is difficult to achieve the open circuit condition. Fig. 6 shows the current variation to verify the effectiveness of C_{in}. It reduces the input current to zero value with increase of capacitance. Also, the large C_{in} can achieve the open circuit condition. The capacitance selection induces the magnitude difference between the optimizer current (I_{opt}) and I_{in}.

In terms of arc gap length, Fig. 5 and Fig. 6 are measured at 1.1 mm arc gap. Fig. 7 shows the experimental results with various arc gap lengths, such as 0.8 mm and 2.5 mm. The operational waveforms and minimum current are similar according to arc gap lengths. Therefore, the C_{in} is dominant to change the voltage and current characteristics compared with arc gap lengths. The arc fault generator makes the mechanical transient with falling two electrodes and electrical transient with addition of arc resistance in the power line. The electrical transient that is measured with experimental results is faster than the mechanical transient, as shown in Table 2. Therefore, the arc fault detection and extinguishing based on the arc resistance is decoupled with mechanical operation. Fig. 8 shows the consistency of arc fault extinguishing through the repeated tests. The proposed C_{in} design can achieve the natural arc fault extinguishing.
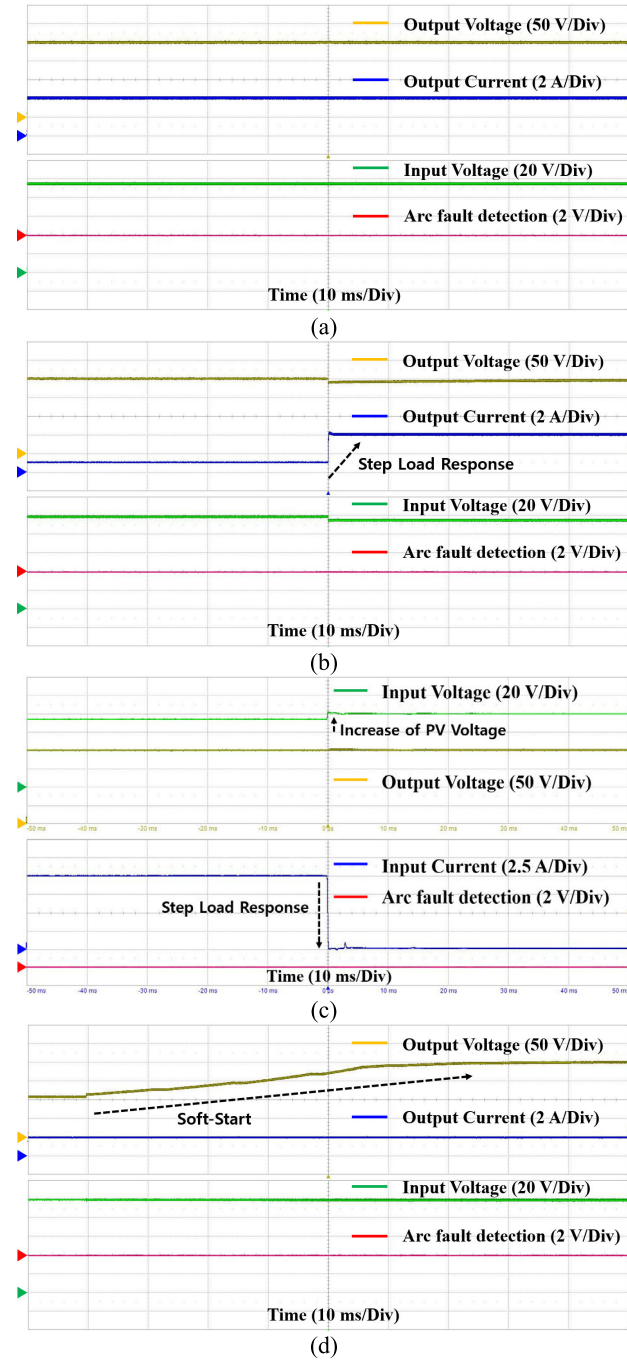
FIGURE 12. Experimental results for normal operating condition: (a) steady state operation, (b) load increase condition, (c) load reduction condition, and (d) soft-start.

FIGURE 13. Performance of arc fault detection and extinguishing method: (a) Irradiance variation and (b) arc fault condition.

fully discharges energy of C_{in}. After t_1, the DC/DC converter has no power conversion.

Fig. 10 shows the designed arc fault detection algorithm. The proposed arc fault detection algorithm utilizes the input voltage and current sensors. In the steady state condition, the digital signal processor monitors the input current and voltage to find the drastic magnitude drop. When the arc fault is occurred, the input current and voltage is reduced to zero value according to the proper input capacitor design. The fault detection criteria for input current and voltage can be derived as follows:

$$I_{in,a} - i_{in}(t) > I_{th} \tag{18}$$

$$v_{in}(t) < V_{th} \tag{19}$$

where $I_{in,a}$ is the average value of DC current, I_{th} is the threshold of DC current drop, which is smaller than $I_{in,a}$, and V_{th} is the threshold value of open circuit condition.

III. EXPERIMENTAL VERIFICATION

An experimental setup was designed to verify the performance of the proposed arc-fault detection and extinguishing methods under an arc-fault transient duration. Fig. 11 shows the experimental setup, which employed two PV modules (LG, LG420QAK-A6), a boost-type DC optimizer, an arc-fault generator based on the UL 1699 B standard, and an electric load (KIKUSUI, PLZ1205 W). The specification of DC optimizer is same as Table 1. The C_{in} and C_o are 94 μF and 10 μF, respectively. Fig. 12 shows the experimental

C. ARC FAULT DETECTION ALGORITHM

Fig. 9 shows the theoretical operation of boost converter to detect and extinguish the fault condition. When the arc fault occurs at t_0, the input current reduces to zero value with C_{in} design. The negative resistance characteristics increases the arc resistance from t_0 to t_1. The large arc resistance induces the open circuit condition between DC link and converter. It makes naturally arc fault extinguishing. Also, this condition
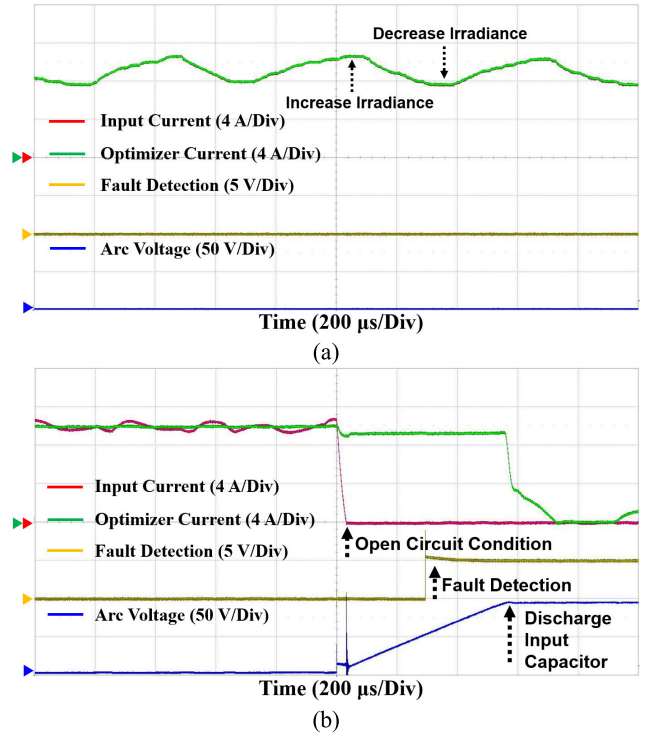
results for the normal conditions, which includes the steady state, soft-start, load variation conditions. The proposed method designs C_{in} to classify the arc fault and normal conditions with input current and voltage relationship. In Fig. 12 (a), the steady state condition shows no variation in the input voltage and current. In Fig. 12 (b) and (c), the load variation condition shows the increase and decrease of input current without the input voltage change. In Fig. 12 (d), the soft-start condition shows the increase of output voltage. The normal condition cannot satisfy the fault detection condition.

Fig. 13 (a) shows the experimental result of irradiance variation, which induces the input current variation. However, it cannot satisfy the arc fault detection condition, since it does not change the input voltage of converter. Fig. 13 (b) verifies the series arc fault detection and natural fault extinguishing capability. The designed input capacitance using (16) has input current reduction to zero value, which increases the arc resistance. Also, the large arc resistance induces the open circuit condition, which reduces the input voltage to zero value. Therefore, experimental results can verify the validity of proper C_{in} design. In this experiment, the controller (TI, TMS320F28379D) implements 200 kHz sampling speed. It is proper to detect the input current and voltage change, since the fault transient duration (5 ms) is 1000 times longer than sampling period ($5\mu s$). From Fig. 13 (b), the designed algorithm can detect the fault condition within 600 μs. The conventional fault detection using the power flow control requires the long fault detection time over 150 ms [16]. However, the proposed method can achieve the fast fault detection capability.

IV. CONCLUSION

This paper proposed DC series arc fault detection based on a DC optimizer design, focusing on the arc fault between the PV panel and the DC optimizer. The characteristics of the arc fault were analyzed to maximize arc fault resistance. Moreover, input and output capacitor designs have been investigated to effectively reduce the input current, which can achieve open-circuit conditions with a high arc resistance. The designed arc fault detection flowchart can classify faults and normal conditions. The experimental results verify the validity of the proposed arc fault detection methods.

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HWA-PYEONG PARK (Member, IEEE) was born in Gimcheon, South Korea, in 1991. He received the Ph.D. degree in electrical engineering from Ulsan National Institute of Science and Technology (UNIST), Ulsan, South Korea, in 2019. From 2019 to 2022, he was a Senior Researcher with Korea Institute Energy Research. He is currently with the Kumoh National Institute of Technology. His main research interests include high-power-density dc–dc converters, power control algorithm for power converters, and battery management systems.

MINA KIM (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Ulsan National Institute of Science and Technology, Ulsan, South Korea, in 2015 and 2021, respectively. From 2021 to 2023, she was a Senior Researcher with Korea Electronics Technology Institute (KETI). Since 2023, she has been an Assistant Professor of electrical engineering with Hanbat National University. Her research interests include high efficiency power conversion technology, control and power management algorithms, and reliability enhancement for next-generation low-voltage dc power systems and photovoltaic systems.

SUYONG CHAE (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 1998 and 2000, respectively, and the Ph.D. degree from Seoul National University, Seoul, South Korea, in 2009. From 2000 to 2010, he was a Research Engineer with Samsung SDI. From 2010 to 2022, he was a Principle Researcher with Korea Institute of Energy Research. Since 2022, he has been a Faculty Member in electrical engineering with Pohang University of Science and Technology (POSTECH), Pohang, South Korea, where he is currently an Associate Professor. His research interests include power electronics, and modeling and control of distributed power systems.

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