MOTORVEHICLE
UNIVERSITY OF
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CASCADE H-BRIDGE SEVEN-LEVEL THREE-PHASE INVERTER ANALYSIS

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INTRODUCTION

Inverters are static electric machines that convert DC voltages in AC ones. Inverters are paramount devices because they are used in crucial applications: photovoltaic installations, electric power system (like SACOI), electric vehicles and so on.
In the more general case, they are built by using solid-state switches (like IGBTs or MOSFETs and diodes), capacitors and the driver circuit.
There exist many types of inverters with different topologies (both single-phase and three-phase), features and prices.
Inverters aim to reconstruct AC waves by commutating switches. Switches commutate in a way such that the voltage across the output inverter terminals is a composition of constant voltages which values are multiple of the DC source voltage. The type of inverter that is characterized by few levels approximates the output wave roughly. Therefore, to get more precise AC waves it is necessary to increase the number of levels by choosing the suitable inverter topology.
More relevant inverter quantities are the output voltage and the output current. It is paramount to provide AC voltages and AC currents to the AC circuits in order to avoid the injection of distorted quantities. The amount of distortion is evaluated through the THD (Total Harmonic Distortion) that takes into account the actual wave and the desired one. Therefore, the goal is to keep the THDs as low as possible.

SCHEMATIC AND WORKING PRINCIPLE

The considered topology is the Cascade H-bridge seven-level three-phase. This type of inverter can be controlled by using two possible modulation techniques: Phase-Shift PWM and Level-Shift PWM. The schematics of this inverter controlled by the two different techniques are shown in the figure 1.1 and 1.2:

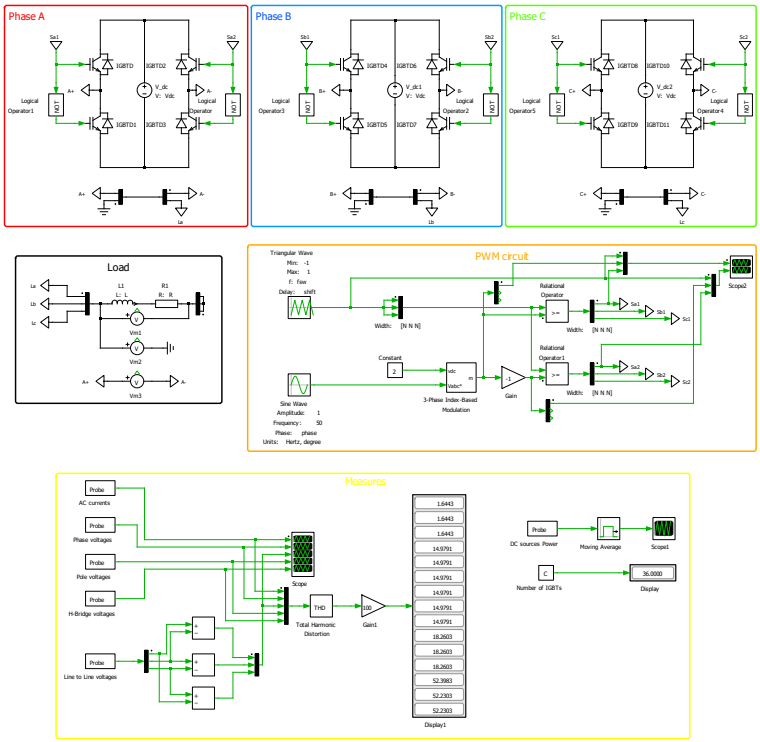

Figure 1.1 Cascade H-bridge seven-level three-phase inverter – Phase Shift PWM

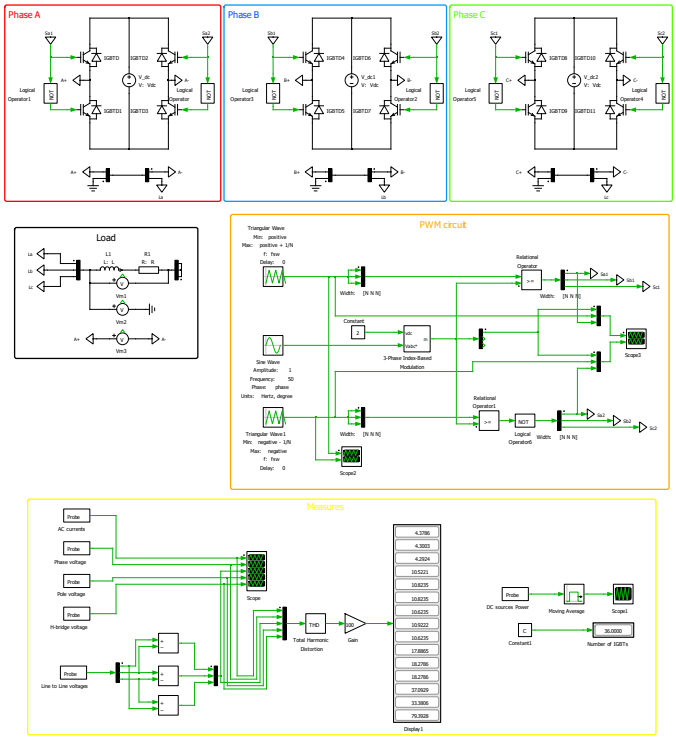

Figure 1.2 Cascade H-bridge seven-level three-phase inverter – Level Shift PWM

The two schemes differ only for the driver circuits because the only difference is the modulation technique that drives the same inverter.
The considered inverter is characterized by the connection of nine H-bridge modules. Each H-bridge refers to a specific phase (Phase A, Phase B and Phase C) and has an isolated DC source, four IGBTs and four diodes.
One of the main advantages of the Cascade H-bridge is the modularity. As more H-bridge modules are connected in cascade to each other for each phase, the number of levels increases, and the output waves are more sinusoidal. The modularity of CHB inverters gives more reliability than NPC inverters (like a redundancy).
If the cascade-connected modules are four, the scheme for a phase is the one represented in Figure 2:

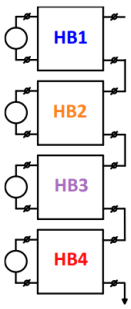

Figure 2 Four H-bridges connected in cascade for a phase

The cascade connection is performed in PLECS by means of electric labels, wire multiplexers and the ground.
The three-phase inverter supplies a three-phase star-connected inductive load.
The working principle of the Cascade H-bridge seven-level three-phase inverter depends on the modulation techniques. It is described in the next paragraph by considering only one H-bridge of the phase A, for the sake of simplicity.

Phase-Shift PWM modulation

It is generated a carrier signal that is a triangular wave that varies from 0 to +1 and comes back to 0 symmetrically according to the switching frequency. Moreover, each leg of the H-bridge module is associated with a sinusoidal modulating signal. For one leg, the modulating signal has a unit amplitude, a frequency equals 50 Hz (the desired frequency for the output waves) and a phase delay that depends on the associated phase among A, B and C. The modulating signal of the other leg is the same of the previous one but with an additional delay equals 180°.

By considering the nomenclature used in PLECS, and calling the modulating signal of the left leg v_{o1}^* and the one of the right leg v_{o2}^*, the switches commutate according to the following conditions and generate the output voltage v_o::

$$\begin{gathered} v_{o1}^* > carrier \implies IGBTD\ ON \\ v_{o2}^* < carrier \implies IGBTD3\ ON \\ v_o = V_{dc} \end{gathered}$$

Equation 1.1

$$\begin{gathered} v_{o1}^* < carrier \implies IGBTD1\ ON \\ v_{o2}^* > carrier \implies IGBTD2\ ON \\ v_o = -V_{dc} \end{gathered}$$

Equation 1.2

$$\begin{gathered} v_{o1}^* > carrier \implies IGBTD\ ON \\ v_{o2}^* > carrier \implies IGBTD2\ ON \\ v_o = 0 \end{gathered}$$

Equation 1.3

$$\begin{gathered} v_{o1}^* < carrier \implies IGBTD1\ ON \\ v_{o2}^* < carrier \implies IGBTD3\ ON \\ v_o = 0 \end{gathered}$$

Equation 1.4

In the equations 1.1, 1.2, 1.3 and 1.4 only one switch of a certain leg has been considered because the other one has the opposite logic status to avoid the leg short circuit.

By comparing the modulating signals with the carrier signal, PWM signals are generated to drive the switches of the related legs. In figure 3, gate signals Sa1 and Sa2 of all H-bridges of the Phase A are shown:

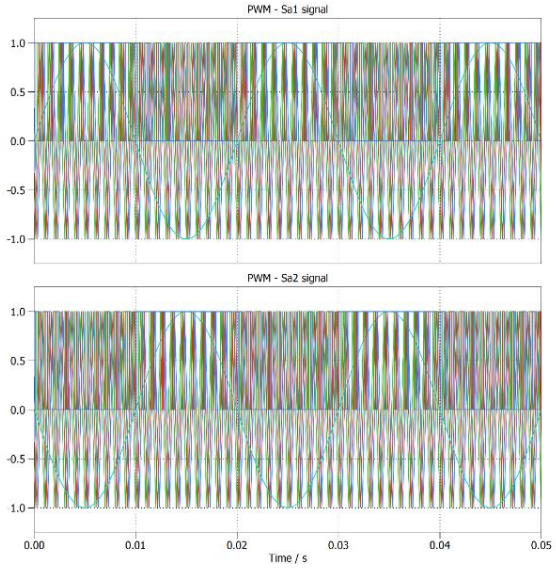

Figure 3 Modulating, carrier and PWM signals for the Phase A H-bridges in Phase Shift PWM modulation case

Level-Shift PWM modulation

It is generated a modulating signal v_{A0}^* that has a unit amplitude, a frequency equals 50 Hz (the desired frequency for the output waves) and a phase delay that depends on the associated phase among A, B and C. Moreover, each H-bridge is associated with two carrier signals that are triangular waves. The "carrier 2" varies from 0 to +1 and comes back to 0 symmetrically according to the switching frequency. The "carrier 1" varies from -1 to 0 and comes back to -1 symmetrically according to the same switching frequency.

By considering the nomenclature used in PLECS, the switches commutate according to the following conditions and generate the output voltage v_o:

$$v_{A0}^* \geq 0 \cup v_{A0}^* > carrier\ 2 \implies IGBTD, IGBTD3\ ON$$
$$v_o = V_{dc}$$

Equation 2.1

$$v_{A0}^* \geq 0 \cup v_{A0}^* < carrier\ 2 \implies IGBTD1, IGBTD3\ ON$$
$$v_o = 0$$

Equation 2.2

$$v_{A0}^* \leq 0 \cup v_{A0}^* < carrier\ 1 \implies IGBTD1, IGBTD2\ ON$$
$$v_o = -V_{dc}$$

Equation 2.3

$$v_{A0}^* \leq 0 \cup v_{A0}^* > carrier\ 1 \implies IGBTD1, IGBTD3\ ON$$
$$v_o = 0$$

Equation 2.4

As in the Phase-Shift PWM modulation, only one switch of a certain leg can conduct.

By comparing the modulating signal with the carrier signals, PWM signals are generated to drive the switches of the related legs. In figure 4, gate signals Sa1 and Sa2 of all H-bridges of the Phase A are shown:

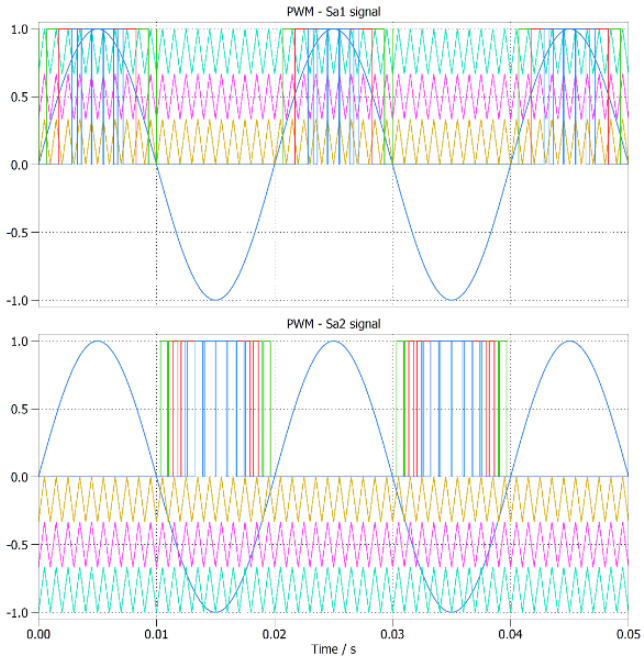

Figure 4 Modulating, carrier and PWM signals for the Phase A H-bridges in Level Shift PWM modulation case

PLECS SIMULATION 1

In the first PLECS simulation the Phase-Shift PWM modulation technique has been adopted. The data used for the simulation are reported in the Table 1:

Table 1 PLECS simulation 1 data

Data	Symbol	Value	Measurement Unit
Number of cascade-connected H-bridges per phase	N	3	dimensionless
Input Voltage	V_{dc}	100	V
Switching frequency	f_{sw}	1000	Hz
Modulating frequency	None	50	Hz
Load Inductance	L	1e-3	H
Load Resistance	R	5	Ω

Moreover, to cope with the three-phase system and the flexibility of adding more H-bridges, some vectors must be defined in the "Model initialization commands" section to set in the proper way the signal generator blocks.
The carrier signals must be equally shifted in their half time period. The related code is given by the equation 3.1:

```
shift = [0:1:N-1]/N/fsw/2;
```

Equation 3.1

The modulating signals must make a symmetric three-phase system and each signal must refer to a specific inverter phase. In the equations 3.2 and 3.3 the implementing code is shown:

```
U = ones(1, N);
```

Equation 3.2

```
phase = [0*u -120*u 120*u];
```

Equation 3.3

The modulation index is set by the block "3-Phase Index-Based Modulation" which modulation strategy is the Sinusoidal PWM. The block gets as inputs the sinusoidal signals and a constant. As the modulating signals have been set with an amplitude of 1, the input constant of the block equals the peak-to-peak amplitude of the modulating signals, thus two.
In the figure 5 the load currents, the phase load voltages, the line-to-line load voltages, the pole voltages and the output Phase A H-bridges voltages are shown:

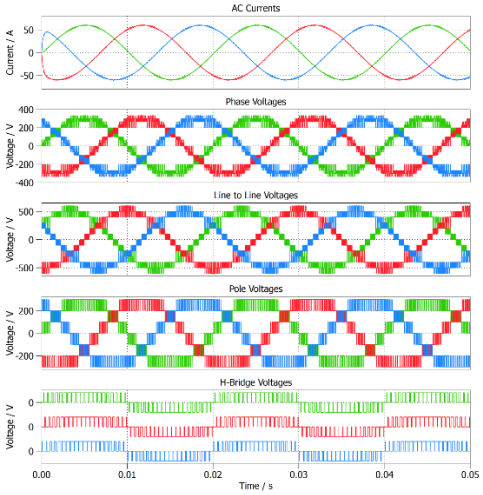

Figure 5 Main quantities in the CHB inverter controlled by Phase-Shift PWM modulation

The load currents are almost sinusoidal, their THD is about 1.6% (low).
The load phase voltages and the load line-to-line voltages are not perfectly sinusoidal as their THD values equal about 15%.
The pole voltages are characterized by seven levels, as expected due to the topology, with a THD of 18%.
The output H-bridges voltages have 3 levels. Therefore, the THD is very high, it equals 52%.
The FFT diagrams of these quantities are shown in the Figure 6:

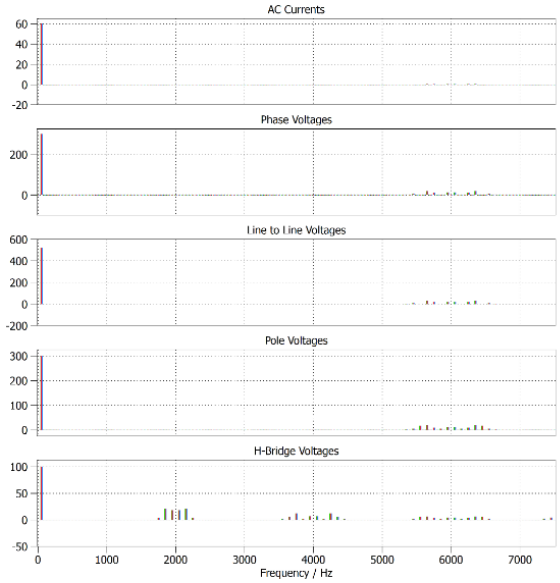

Figure 6 FFT of the quantities reported in the figure 5

The load currents, the phase load voltages, the line-to-line load voltages and the pole voltages have a relevant fundamental component and smaller components at higher frequencies. The components at higher frequencies are centred at the frequency calculated in the equation 4:

$$f_{PS} = 2 \cdot N \cdot f_{sw} = 2 \cdot 3 \cdot 1000 = 6000\ Hz$$

Equation 4

In the Figure 7, the powers provided by DC sources are shown:

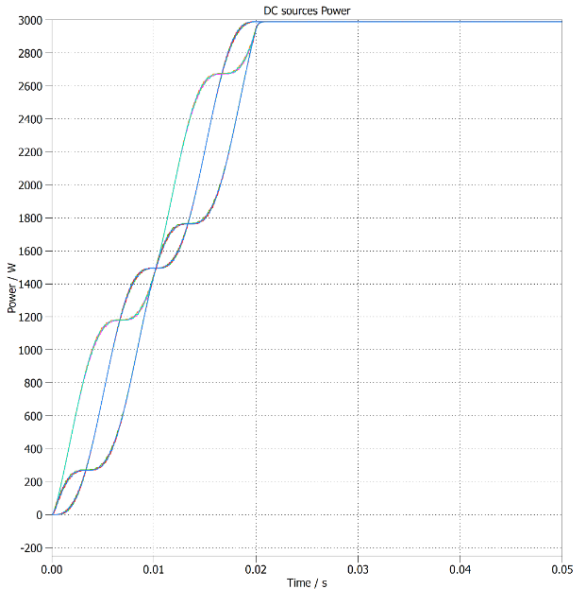

Figure 7 Powers provided by DC sources in Phase Shift PWM modulation case

PLECS SIMULATION 2

In the second PLECS simulation the Level-Shift PWM modulation technique has been adopted. The data used for the simulation are the same reported in the Table 1.
As in the previous simulation, some vectors are defined in the "Model initialization commands" section to set in the proper way the signal generator blocks.
The carrier signals must be distributed along the y-axis. The related code is given by the equations 5.1 and 5.2:

positive = [0:1:N-1]/N

Equation 5.1

negative = [0:-1:-N+1]/N

Equation 5.2

The vector "positive" lets to generate triangular waves in the positive y half-axis. On the contrary, the vector "negative" lets to generates triangular waves in the negative y half-axis.
The modulating signals must make a symmetric three-phase system and each signal must refer to a specific inverter phase. The codes reported in the equations 3.2 and 3.3 are rewritten for this case as well.
The modulation index is set by the block "3-Phase Index-Based Modulation" in the same way done for the simulation 1.
In the figure 8 the load currents, the phase load voltages, the line-to-line load voltages, the pole voltages and the output Phase A H-bridges voltages are shown:

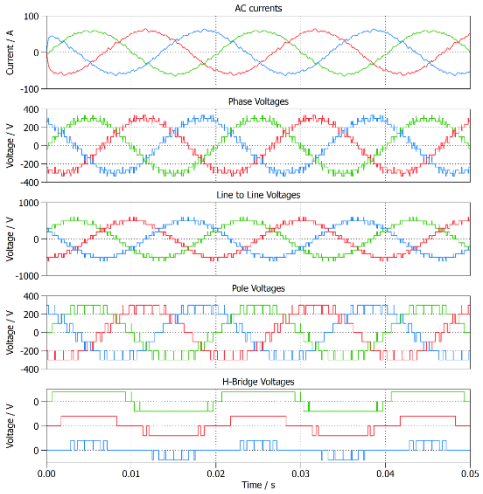

Figure 8 Main quantities in the CHB inverter controlled by Level-Shift PWM modulation

The load currents are almost sinusoidal with a visible ripple, their THD is about 4% (low).
The load phase voltages and the load line-to-line voltages are not perfectly sinusoidal as their THD values equal about 11%.
The pole voltages are characterized by seven levels, as expected by the topology, with a THD of 18%.
The output H-bridges voltages have 3 levels. However, the waveforms are not the same. In fact, THDs of these voltages are very different (33% for the green one, 37% for the red one and 80% for the blue one).
H-bridges for each phase are characterized by a varying switching frequency averaging to fsw/N. Legs switch according to the (too low) effective switching frequency calculated in the equation 6:

$$\frac{f_{SW}}{2 \cdot N} = \frac{1000}{2 \cdot 3} = 166.7\ Hz$$

Equation 6

The FFT diagrams of these quantities are shown in the Figure 9:

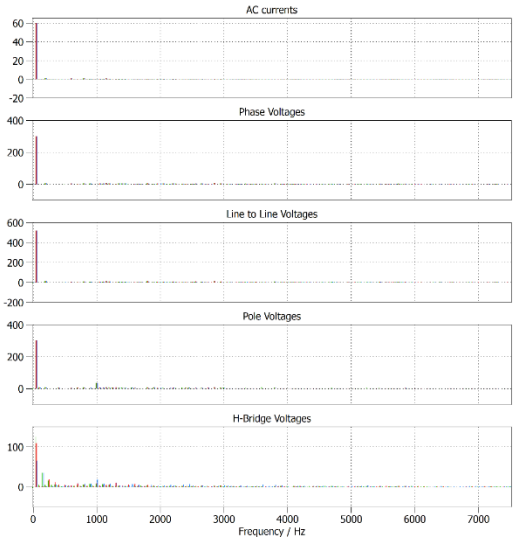

Figure 9 FFT of the quantities reported in the figure 8

The load currents, the phase load voltages, the line-to-line load voltages and the pole voltages have a relevant fundamental component and smaller components at (not so very) high frequencies. The components at higher frequencies than the fundamental one are centred at the switching frequency.

In the Figure 10, the powers provided by DC sources are shown:

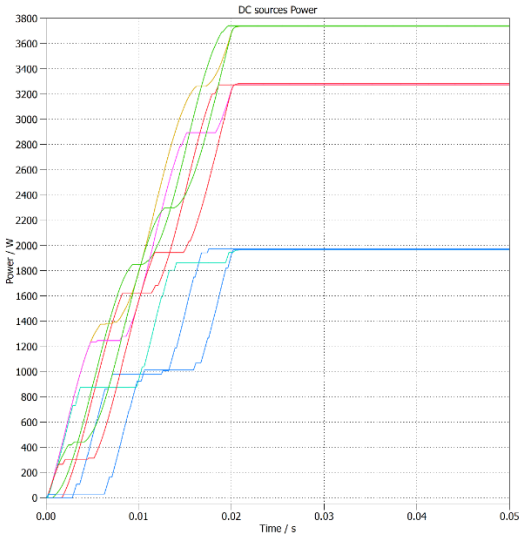

Figure 10 Powers provided by DC sources in the Level-Shift PWM modulation

H-bridges share the same power (so, the same voltage) in groups of three ones.

CONCLUSIONS

Both Phase-Shift PWM modulation technique and Level-Shift one lead to get almost sinusoidal waveforms but with different quality. The first technique can generate better waveforms than the ones got by using the second technique. Furthermore, the “distorted components” of the waveforms generated by the first technique are characterized by higher frequencies than the ones of the waveforms generated by the second technique. The first ones are easier to filter out thankful to the effective switching frequency multiplication. Therefore, the first ones are subject to an AC harmonic cancellation.

To have the components at the same high frequencies, by using Level-Shift PWM modulation technique, it is necessary to increase the switching frequency.
By using the Phase-Shift PWM modulation, each DC power source provides to each H-bridge the same power at steady state (capacitor balancing) unlike the other modulation technique.
However, the power losses are less in the Level-Shift PWM modulation case.
The last advantage of the Phase-Shift PWM modulation is the association of a particular carrier signal to a specific H-bridge module over the time.
Nevertheless, CHB inverters need of several isolated DC supply ports to avoid short-circuits.
Therefore, Level-Shit PWM modulation technique is not recommended.

It is obvious that by increasing the number of H-bridges per phase the waveforms improve. In the figures 11 and 12 the main quantities described in the previous paragraphs are shown by considering N=149:

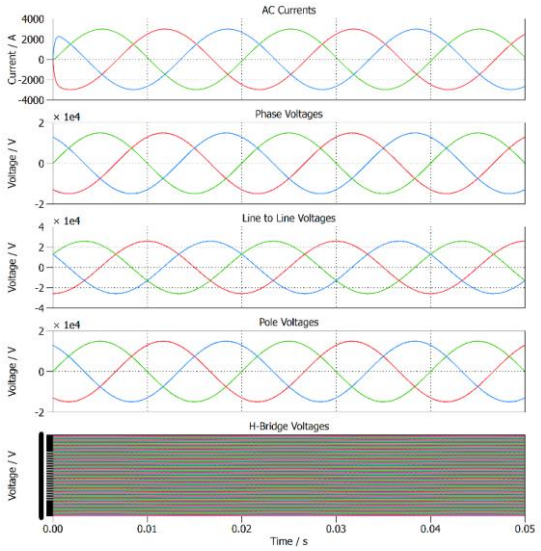

Figure 11 Main quantities in the CHB inverter controlled by Phase-Shift PWM modulation for N=149

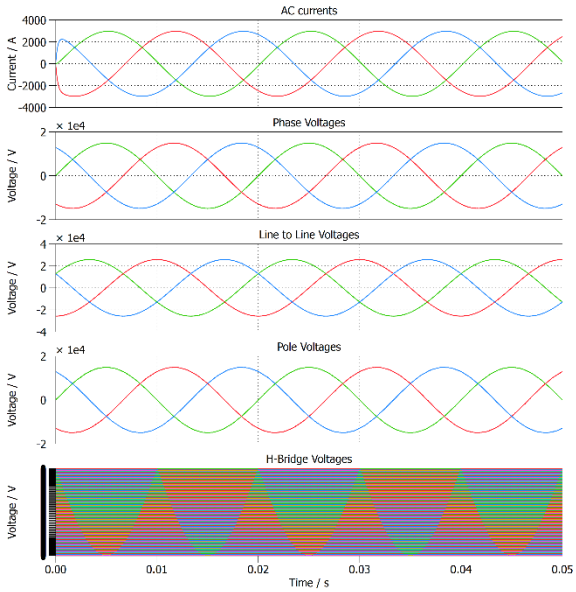

Figure 12 Main quantities in the CHB inverter controlled by Level-Shift PWM modulation for N=149

Regardless of H-bridge voltages, the THDs of represented quantities are less than 1%. Therefore, these electrical quantities are almost perfect sinusoids. However, the number of IGBTs rises from 36 to 1788.