74AHC257; 74AHCT257

Quad 2-input multiplexer; 3-state Rev. 02 — 9 May 2008

Product data sheet

General description 1.

The 74AHC257; 74AHCT257 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC257; 74AHCT257 has four identical 2-input multiplexers with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S). The data inputs from source 0 (110 to 410) are selected when input S is LOW and the data inputs from source 1 (111 to 411) are selected when input S is HIGH. Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the selected inputs. The 74AHC257; 74AHCT257 is the logic implementation of a 4-pole 2-position switch, where the position of the switch is determined by the logic levels applied to input S. The outputs are forced to a high-impedance OFF-state when \overline{OE} is HIGH.

The logic equations for the outputs are:

$$1Y = \overline{OE} \times (1I1 \times S + 1I0 \times \overline{S})$$

$$2Y = \overline{OE} \times (2I1 \times S + 2I0 \times \overline{S})$$

$$3Y = \overline{OE} \times (311 \times S + 310 \times \overline{S})$$

$$4Y = \overline{OE} \times (4I1 \times S + 4I0 \times \overline{S})$$

The 74AHC257; 74AHCT257 is identical to the 74AHC258; 74AHCT258, but has non-inverting (true) outputs.

2. **Features**

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Non-inverting data path
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - For 74AHC257: CMOS level
 - ◆ For 74AHCT257: TTL level
- ESD protection:
 - HBM EIA/JESD22-A114E exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V
 - CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

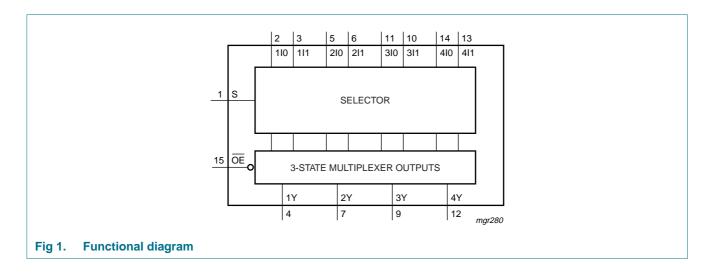


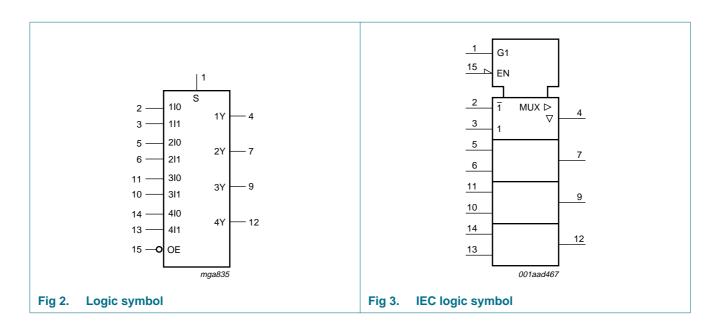
3. Ordering information

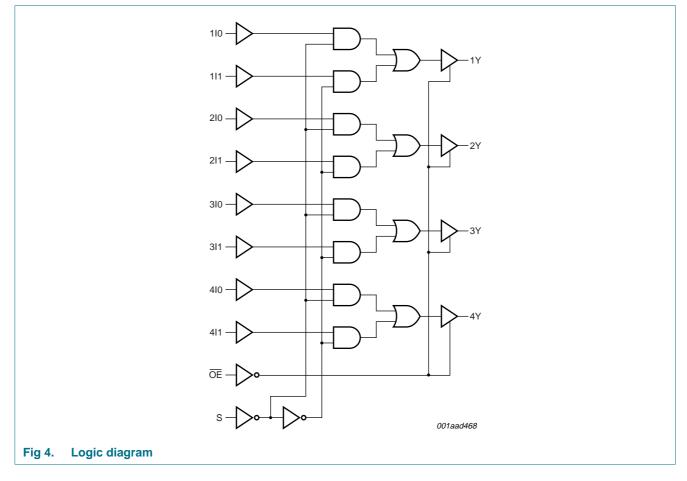
Table 1. Ordering information

Type number	Package									
	Temperature range	Name	Description	Version						
74AHC257										
74AHC257D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1						
74AHC257PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1						
74AHCT257										
74AHCT257D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1						
74AHCT257PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1						

4. Functional diagram

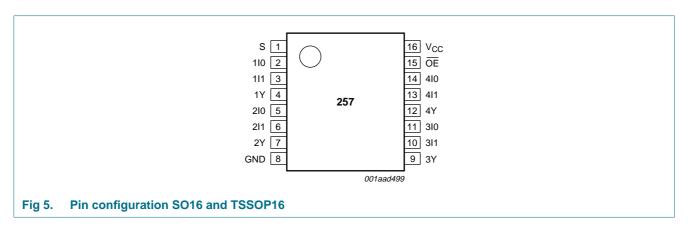






5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol Pin Description S 1 common data select input 110 2 data input from source 0 111 3 data input from source 1 1Y 4 multiplexer output 210 5 data input from source 0 211 6 data input from source 1 2Y 7 multiplexer output GND 8 ground (0 V) 3Y 9 multiplexer output 3I1 10 data input from source 1 3I0 11 data input from source 0 4Y 12 multiplexer output 4I1 13 data input from source 1 4I0 14 data input from source 0 OE 15 output enable input (active LOW) Vcc 16 supply voltage		<u> </u>	
110 2 data input from source 0 111 3 data input from source 1 1Y 4 multiplexer output 2I0 5 data input from source 0 2I1 6 data input from source 1 2Y 7 multiplexer output GND 8 ground (0 V) 3Y 9 multiplexer output 3I1 10 data input from source 1 3I0 11 data input from source 0 4Y 12 multiplexer output 4I1 13 data input from source 1 4I0 14 data input from source 0 OE 15 output enable input (active LOW)	Symbol	Pin	Description
111 3 data input from source 1 1Y 4 multiplexer output 2I0 5 data input from source 0 2I1 6 data input from source 1 2Y 7 multiplexer output GND 8 ground (0 V) 3Y 9 multiplexer output 3I1 10 data input from source 1 3I0 11 data input from source 0 4Y 12 multiplexer output 4I1 13 data input from source 1 4I0 14 data input from source 0 OE 15 output enable input (active LOW)	S	1	common data select input
1Y 4 multiplexer output 2I0 5 data input from source 0 2I1 6 data input from source 1 2Y 7 multiplexer output GND 8 ground (0 V) 3Y 9 multiplexer output 3I1 10 data input from source 1 3I0 11 data input from source 0 4Y 12 multiplexer output 4I1 13 data input from source 1 4I0 14 data input from source 0 OE 15 output enable input (active LOW)	110	2	data input from source 0
2I0 5 data input from source 0 2I1 6 data input from source 1 2Y 7 multiplexer output GND 8 ground (0 V) 3Y 9 multiplexer output 3I1 10 data input from source 1 3I0 11 data input from source 0 4Y 12 multiplexer output 4I1 13 data input from source 1 4I0 14 data input from source 0 OE 15 output enable input (active LOW)	111	3	data input from source 1
2I1 6 data input from source 1 2Y 7 multiplexer output GND 8 ground (0 V) 3Y 9 multiplexer output 3I1 10 data input from source 1 3I0 11 data input from source 0 4Y 12 multiplexer output 4I1 13 data input from source 1 4I0 14 data input from source 0 OE 15 output enable input (active LOW)	1Y	4	multiplexer output
2Y 7 multiplexer output GND 8 ground (0 V) 3Y 9 multiplexer output 3I1 10 data input from source 1 3I0 11 data input from source 0 4Y 12 multiplexer output 4I1 13 data input from source 1 4I0 14 data input from source 0 OE 15 output enable input (active LOW)	210	5	data input from source 0
GND 8 ground (0 V) 3Y 9 multiplexer output 3I1 10 data input from source 1 3I0 11 data input from source 0 4Y 12 multiplexer output 4I1 13 data input from source 1 4I0 14 data input from source 0 OE 15 output enable input (active LOW)	211	6	data input from source 1
3Y 9 multiplexer output 3I1 10 data input from source 1 3I0 11 data input from source 0 4Y 12 multiplexer output 4I1 13 data input from source 1 4I0 14 data input from source 0 OE 15 output enable input (active LOW)	2Y	7	multiplexer output
3I1 10 data input from source 1 3I0 11 data input from source 0 4Y 12 multiplexer output 4I1 13 data input from source 1 4I0 14 data input from source 0 OE 15 output enable input (active LOW)	GND	8	ground (0 V)
3IO 11 data input from source 0 4Y 12 multiplexer output 4I1 13 data input from source 1 4I0 14 data input from source 0 OE 15 output enable input (active LOW)	3Y	9	multiplexer output
4Y 12 multiplexer output 4I1 13 data input from source 1 4I0 14 data input from source 0 OE 15 output enable input (active LOW)	3I1	10	data input from source 1
4I1 13 data input from source 1 4I0 14 data input from source 0 OE 15 output enable input (active LOW)	310	11	data input from source 0
4I0 14 data input from source 0 OE 15 output enable input (active LOW)	4Y	12	multiplexer output
OE 15 output enable input (active LOW)	411	13	data input from source 1
	410	14	data input from source 0
V _{CC} 16 supply voltage	ŌĒ	15	output enable input (active LOW)
	V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table [1]

Control		Input		Output
ŌĒ	S	nI0	nl1	nY
Н	X	X	X	Z
L	Н	X	L	L
		Χ	Н	Н
	L	L	X	L
		Н	X	Н

^[1] H = HIGH voltage level;

L = LOW voltage level;

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_{I}	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_{I} < -0.5 V$	<u>[1]</u> –20	-	mA
I_{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	<u>[1]</u> –20	+20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-25	+25	mA
I _{CC}	supply current		-	+75	mA
I_{GND}	ground current		-75	-	mA
T_{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	[2] _	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

X = don't care;

Z = high-impedance OFF-state.

^[2] For SO16 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K. For TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
74AHC257	•					
V_{CC}	supply voltage		2.0	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	100	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	20	ns/V
74AHCT2	57					
V_{CC}	supply voltage		4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C 1	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74AHC2	57	'								
V_{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH} HIGH-level		$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = -50 \mu A$; $V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50 \mu A; V_{CC} = 3.0 \text{ V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50 \mu A$; $V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.40	-	V
		$I_{O} = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = 50 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 3.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		I_{O} = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C ¹	to +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
II	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IH} \text{ or } V_{IL};$ $V_O = V_{CC} \text{ or GND};$ $V_{CC} = 5.5 \text{ V}$	-	-	±0.25	-	±2.5	-	±10.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μΑ
C _I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
Co	output capacitance		-	4	-	-	-	-	-	pF
74AHCT	257									
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.8	-	8.0	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	$I_{O} = -50 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		$I_0 = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	$V_I = 5.5 \text{ V or GND};$ $V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	-	0.1	-	1.0	-	2.0	μΑ
loz	OFF-state output current	$\begin{split} &V_{I} = V_{IH} \text{ or } V_{IL}; \\ &V_{O} = V_{CC} \text{ or GND per input} \\ &\text{pin; other inputs at} \\ &V_{CC} \text{ or GND; } I_{O} = 0 \text{ A;} \\ &V_{CC} = 5.5 \text{ V} \end{split}$	-	-	±0.25	-	±2.5	-	±10.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μΑ
ΔI_{CC}	additional supply current	per input pin; $V_{I} = V_{CC} - 2.1 \text{ V};$ other pins at V_{CC} or GND; $I_{O} = 0 \text{ A}; V_{CC} = 4.5 \text{ V} \text{ to } 5.5 \text{ V}$	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
C _O	output capacitance		-	4	-	-	-	-	-	pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions			25 °C		-40 °C	to +85 °C	–40 °C to	o +125 °C	Unit	
				Min	Typ[1]	Max	Min	Max	Min	Max		
74AHC2	57	'										
t _{pd}	propagation	nI0, nI1 to nY; see Figure 6	[2]									
	delay	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$										
		C _L = 15 pF		-	4.2	9.3	1.0	11.0	1.0	12.0	ns	
		$C_L = 50 pF$		-	6.0	12.8	1.0	14.5	1.0	16.0	ns	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$										
		C _L = 15 pF		-	2.9	5.9	1.0	7.0	1.0	7.5	ns	
		C _L = 50 pF		-	4.2	7.9	1.0	9.0	1.0	11.5	ns	
		S to nY; see Figure 6	[2]									
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$										
		C _L = 15 pF		-	5.2	11.0	1.0	13.0	1.0	14.0	ns	
		C _L = 50 pF		-	7.4	14.5	1.0	16.5	1.0	18.5	ns	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$										
		C _L = 15 pF		-	3.5	6.8	1.0	8.0	1.0	8.5	ns	
		C _L = 50 pF		-	5.0	8.8	1.0	10.0	1.0	12.5	ns	
t _{en}	enable time	OE to nY; see Figure 7	[3]									
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$										
		$C_L = 15 pF$		-	4.5	10.5	1.0	12.5	1.0	13.5	ns	
		$C_L = 50 pF$		-	6.4	14.0	1.0	16.0	1.0	17.5	ns	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$										
		$C_L = 15 pF$		-	3.2	6.8	1.0	8.0	1.0	8.5	ns	
		$C_L = 50 pF$		-	4.5	8.8	1.0	10.0	1.0	12.5	ns	
t_{dis}	disable time	OE to nY; see Figure 7	<u>[4]</u>									
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$										
		$C_L = 15 pF$		-	5.1	9.5	1.0	11.0	1.0	11.5	ns	
		$C_L = 50 pF$		-	7.2	12.0	1.0	13.5	1.0	14.5	ns	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$										
		$C_{L} = 15 \text{ pF}$		-	3.4	6.5	1.0	7.0	1.0	8.5	ns	
		$C_L = 50 pF$		-	4.9	7.9	1.0	9.0	1.0	9.5	ns	
C _{PD}	power	f_i = 1 MHz; V_I = GND to V_{CC}	[5]									
	dissipation capacitance	4 outputs switching via input S		-	45	-	-	-	-	-	pF	
		1 output switching via input I		-	15	-	-	-	-	-	pF	

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 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions			25 °C		-40 °C 1	to +85 °C	–40 °C t	o +125 °C	Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
74AHCT	257; V _{CC} = 4.5	5 V to 5.5 V									
t _{pd}	propagation	nI0, nI1 to nY; see Figure 6	[2]								
	delay	$C_L = 15 pF$		-	3.7	6.5	1.0	8.0	1.0	9.0	ns
		$C_L = 50 \text{ pF}$		-	4.9	8.5	1.0	10.0	1.0	11.0	ns
		S to nY; see Figure 6	[2]								
		C _L = 15 pF		-	5.1	9.0	1.0	10.5	1.0	11.5	ns
		$C_L = 50 pF$		-	6.4	10.5	1.0	12.5	1.0	13.5	ns
t _{en} enable time	OE to nY; see Figure 7	[3]									
		C _L = 15 pF		-	3.9	8.0	1.0	9.0	1.0	10.0	ns
		$C_L = 50 pF$		-	5.1	10.0	1.0	11.0	1.0	12.0	ns
t _{dis}	disable time	OE to nY; see Figure 7	<u>[4]</u>								
		C _L = 15 pF		-	4.5	7.5	1.0	8.0	1.0	8.5	ns
		$C_{L} = 50 \text{ pF}$		-	6.5	9.5	1.0	10.5	1.0	11.5	ns
C_{PD}	power	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$	<u>[5]</u>								
	dissipation capacitance	4 outputs switching via input S		-	51	-	-	-	-	-	pF
		1 output switching via input I		-	15	-	-	-	-	-	pF

^[1] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3 \text{ V}$ and $V_{CC} = 5.0 \text{ V}$).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs.

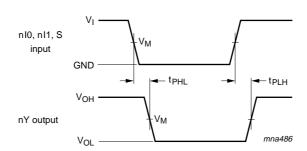
^[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

^[3] t_{en} is the same as t_{PZL} and t_{PZH} .

^[4] t_{dis} is the same as t_{PLZ} and t_{PHZ} .

^[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

11. Waveforms



Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Data inputs and common data select input to output propagation delays

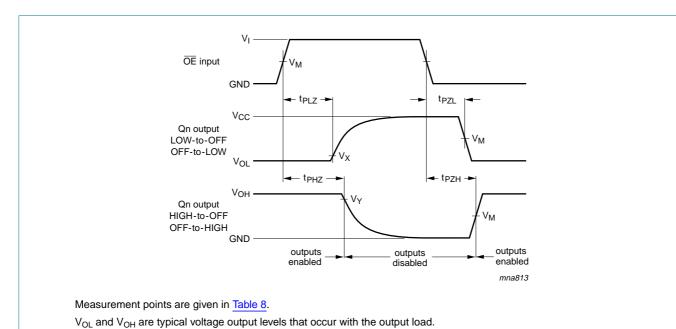
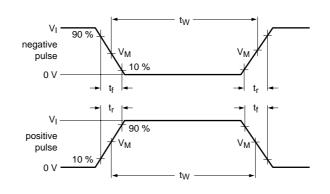


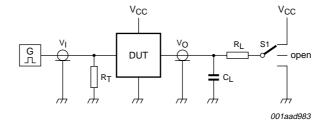
Fig 7. Enable and disable times

Table 8. Measurement points

Туре	Input	Output						
	V _M	V _M	V_X	V _Y				
74AHC257	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V _{OL} + 0.3 V	$V_{OH} - 0.3 V$				
74AHCT257	1.5 V	$0.5 \times V_{CC}$	V_{OL} + 0.3 V	$V_{OH} - 0.3 \ V$				

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Test data is given in Table 9.

Definitions test circuit:

 R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

S1 = test selection switch.

Fig 8. Test circuitry for measuring switching times

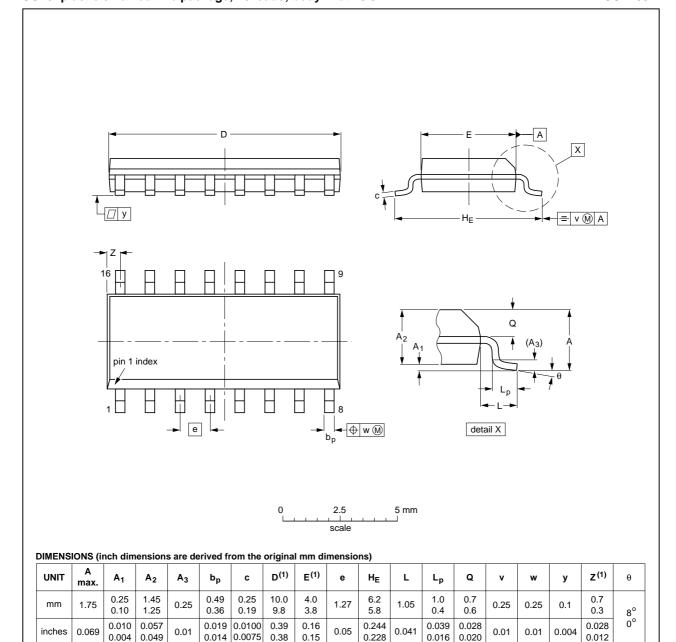
Table 9. Test data

Туре	Input		Load	Load		S1 position		
	VI	t _r , t _f	CL	R _L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}	
74AHC257	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}	
74AHCT257	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}	

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Note

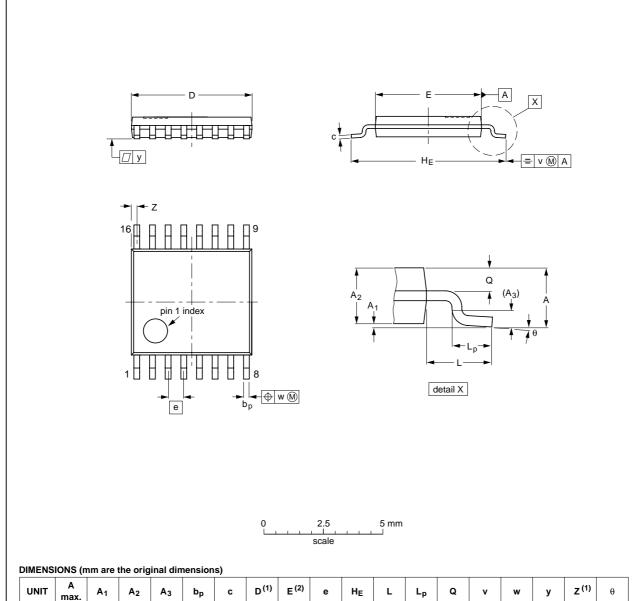
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT109-1	076E07	MS-012			99-12-27 03-02-19

Fig 9. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



 						-,												
UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT403-1		MO-153				99-12-27 03-02-18	

Fig 10. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes			
74AHC_AHCT257_2	20080509	Product data sheet	-	74AHC_AHCT257_1			
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. 						
	 Legal texts l 	nave been adapted to the n	ew company name whe	re appropriate.			
	• <u>Table 6</u> : the	conditions for input leakage	e current have been cha	nged.			
74AHC_AHCT257_1	20000403	Product specification	-	-			

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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