

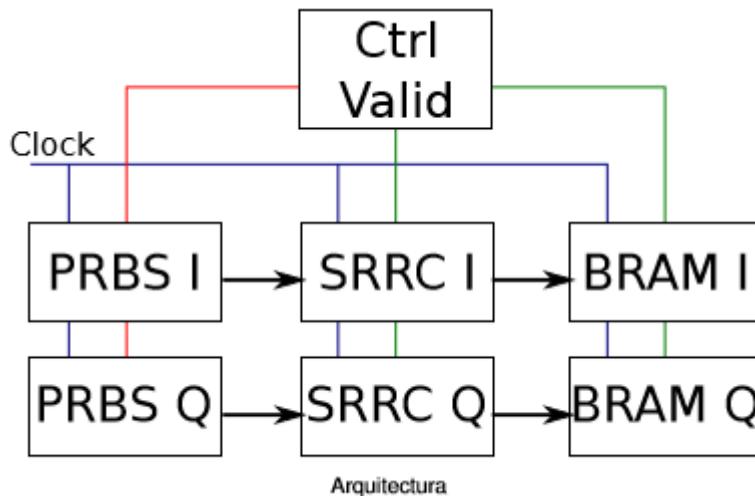
Trabajo de Laboratorio N°3

DISEÑO DIGITAL AVANZADO

Ignacio Balbo

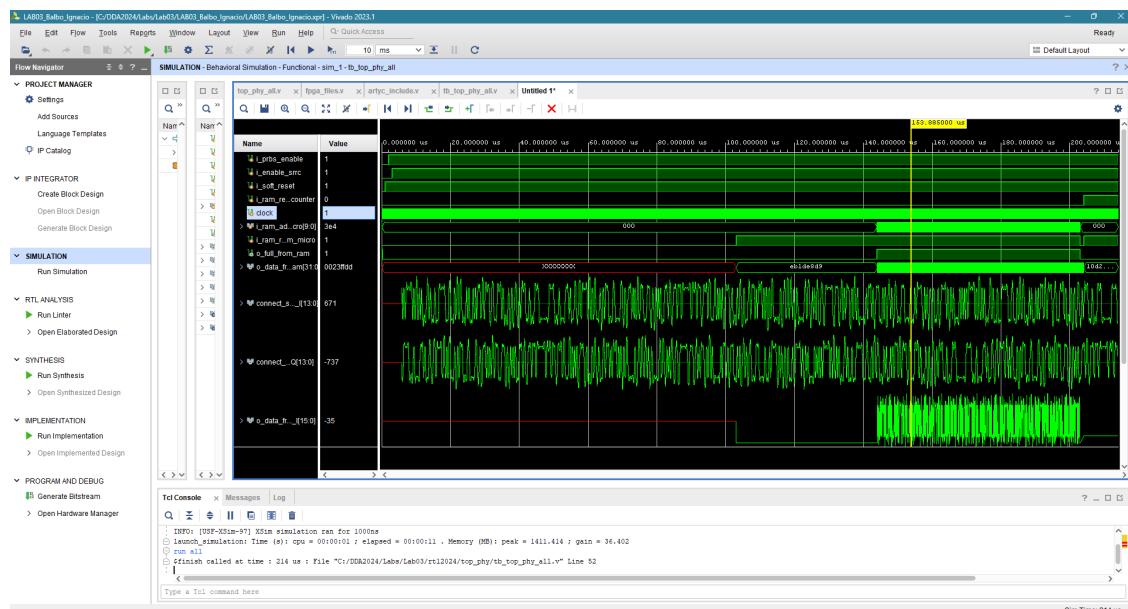
Objetivos

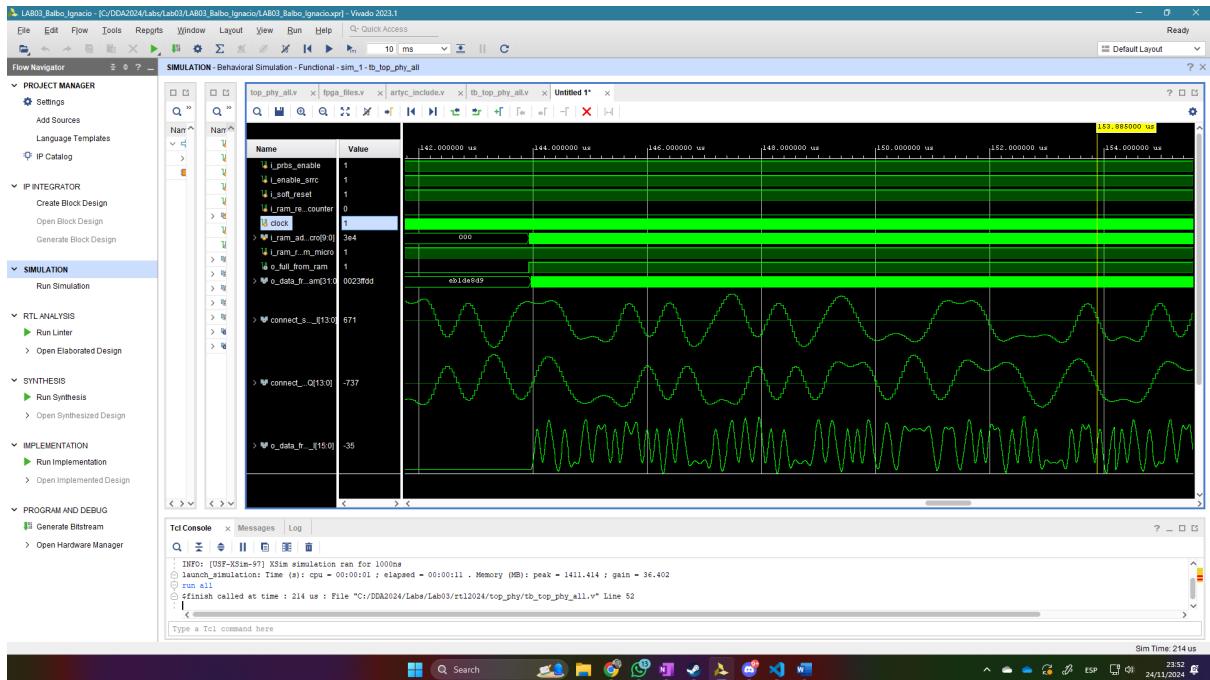
- Obtener elementos de análisis de eficiencia de la arquitectura implementada



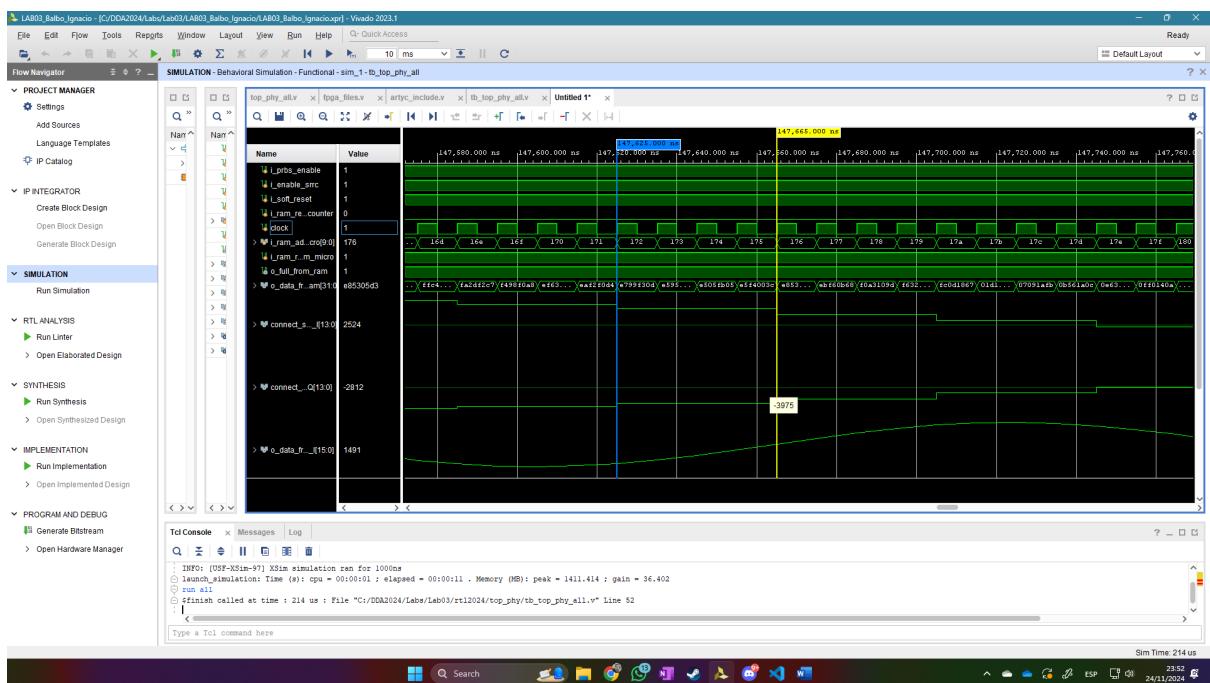
SIMULACIONES

El resultado de la simulación comportamental:

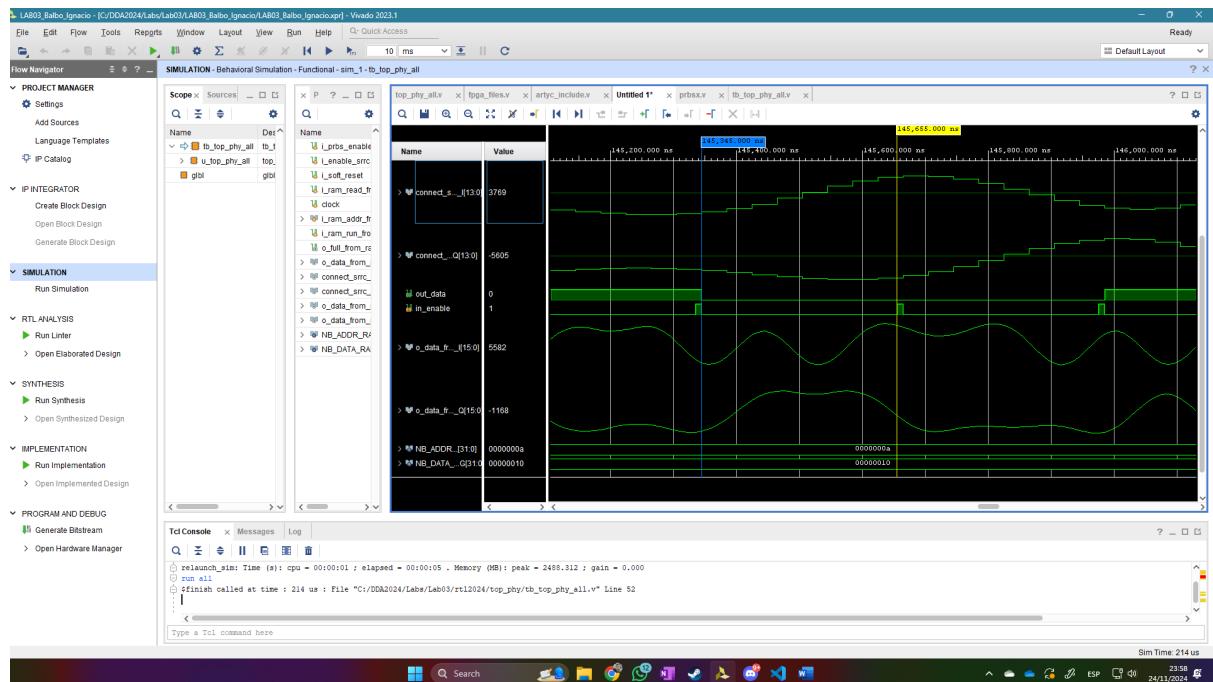




Observamos la cantidad de ciclos que tarda en cambiar el dato por el oversampling de 4 que posee el sistema de cada muestra respecto al reloj



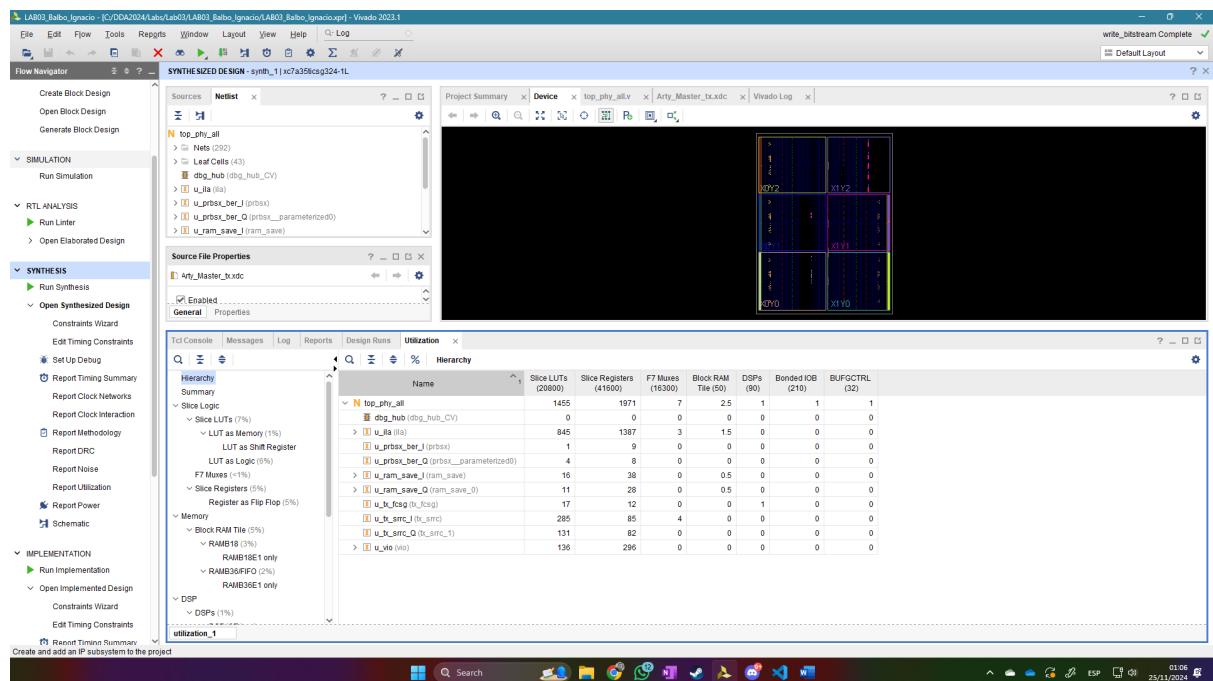
Y la salida de la PRBS, que se puede observar el oversampling de 8 entre los pulsos y las muestras, que por cada pulso tengo 8 muestras diferentes. Con respecto al reloj, los pulsos tienen una relación de 16



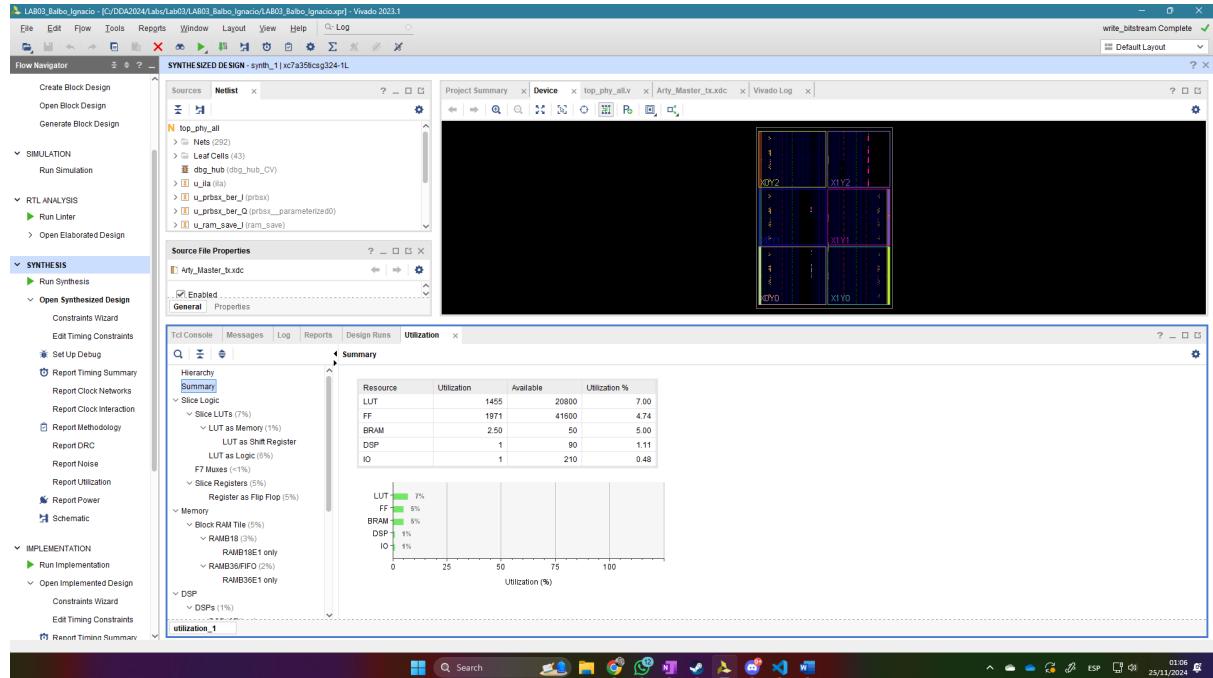
Synthesis: REPORT UTILIZATION

Al correr la síntesis del sistema, incluyendo las instancias de vio e ila, obtenemos el siguiente resultado:

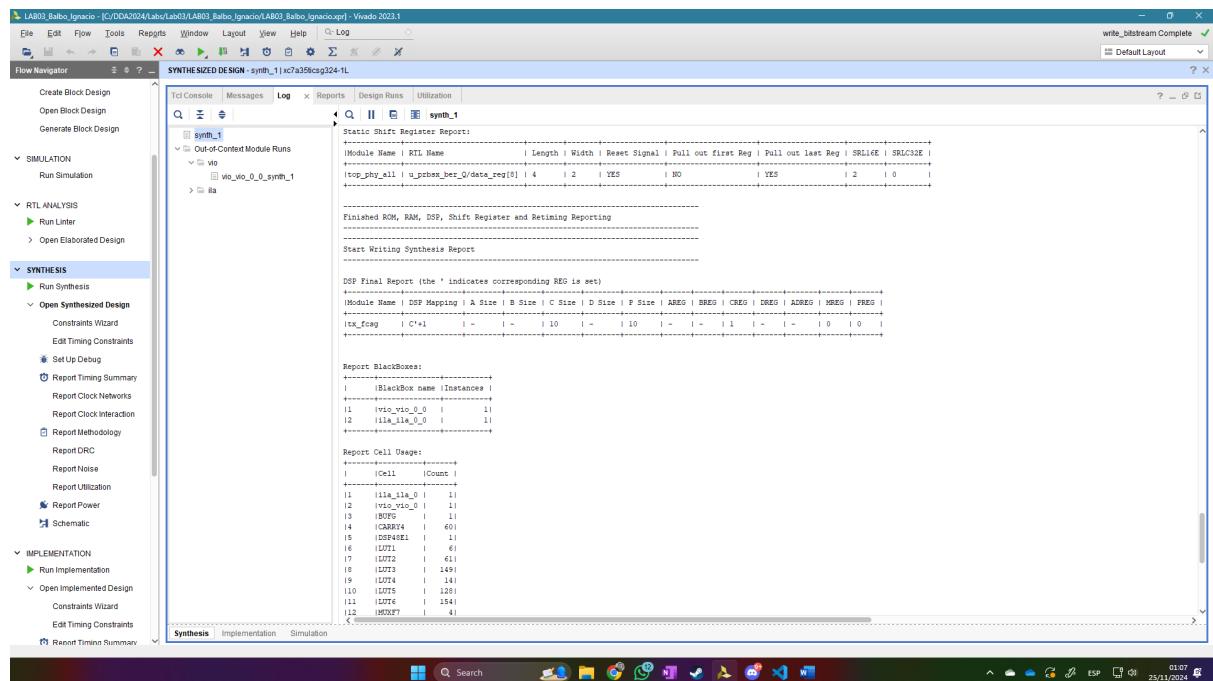
Entre algunos datos, se utilizan 1455 LUTs (mayormente debido al bloque ila), 2.5 block RAM (1.58 del ILA y 0.5 de ram para datos I y 0.5 de ram Q), 1971 slice registers (nuevamente debido al bloque ila en su mayoría). Un solo DSP es utilizado por el modulo u_tx_fcsg.



En la ventana de resumen, podemos ver el % de utilización de cada componente. Solamente un 7% de las LUTs, los demás valores tienen un % bajo respecto a las disponibilidades totales del equipo.



En la siguiente ventanas tenemos tablas que nos detallan: Static shift register report, DSP final report, black boxes (vio e ila) y cell usage.



The screenshot shows the Quartus Prime software interface with the following details:

- Project Path:** LAB03_Balbo_Ignacio | C:/ODA2024/Labs/Lab03/LAB03_Balbo_Ignacio/LAB03_Balbo_Ignacio.prj | Vivado 2023.1
- File Navigator:** Shows sections for Create Block Design, Open Block Design, Generate Block Design, SIMULATION (Run Simulation), RTL ANALYSIS (Run Linter, Open Elaborated Design), SYNTHESIS (Run Synthesis, Open Synthesized Design, Constraints Wizard, Edit Timing Constraints, Set Up Debug, Report Timing Summary, Report Clock Networks, Report Clock Interaction, Report Methodology, Report DRC, Report Noise, Report Utilization, Report Power, Schematic), and IMPLEMENTATION (Run Implementation, Open Implemented Design, Constraints Wizard, Edit Timing Constraints, Report Timing Summary).
- Flow Navigator:** Displays the synthesis flow: Create Block Design → Open Block Design → Generate Block Design → SIMULATION → RTL ANALYSIS → SYNTHESIS → IMPLEMENTATION.
- Tcl Console:** The main window displays the synthesized design flow:
 - synth_1**:
 - Out-Of-Context Module Runs
 - vio
 - vio_vio_0_0_synth_1
 - ila
 - Report BlackBoxes:**

Name	Instances
!vio_vio_0_0	1
!ila_ilia_0_0	1
!ila_ilia_0_0	1
 - Report Cell Usage:**

Cell	Count
!ila_ilia_0	1
!vio_vio_0_0	1
(BDFG)	1
(CARRY4)	601
(LUT2)	1
(LUT3)	8
(LUT4)	61
(LUT5)	149
(LUT6)	144
(LUT7)	1281
(LUT8)	1541
(MUX2)	41
(MUX4)	21
(SRL16E)	2
(TFFCE)	2781
(TFSE)	101
(UBUF)	1
 - Report completed: Finished Writing Synthesis Report : Time (s): cpu = 00:00:01.8 ; elapsed = 00:00:02.0 , Memory (MB): peak = 1516.895 ; gain = 617.219
 - Synthesis finished with 0 errors, 0 critical warnings and 1 warnings.
 - Synthesis Optimization Runtime : Time (s): cpu = 00:00:01.27 ; elapsed = 00:00:01.27 , Memory (MB): peak = 1516.895 ; gain = 50.506
 - Synthesis Optimization Complete : Time (s): cpu = 00:00:01.28 ; elapsed = 00:00:01.28 , Memory (MB): peak = 1516.895 ; gain = 417.219
 - INFO: [Netlist 1-1] Translating synthesized netlist
 - INFO: [Netlist 1-1] Total time (s) = 00:00:00.010 ; elapsed = 00:00:00.010 . Memory (MB): peak = 1516.895 ; gain = 0.000
 - INFO: [Netlist 28-17] Analyzing U1m1m1m1 elements for replacement
 - INFO: [Netlist 28-28] Unisim Transformation completed in 0 CPU seconds
 - INFO: [Project 1-1] Preparing netlist for logic optimization
 - INFO: [Netlist 1-1] Preparing netlist for logic optimization
 - INFO: [Netlist 1-1] Netlist sorting complete. Time (s): cpu = 00:00:00.001 . Memory (MB): peak = 1516.895 ; gain = 0.000
 - INFO: [Project 1-1] Unisim Transformation Summary:
No Unisim elements were transformed.

Implementacion: UTILIZATION

Si implementamos el proyecto, obtenemos el siguiente resultado:

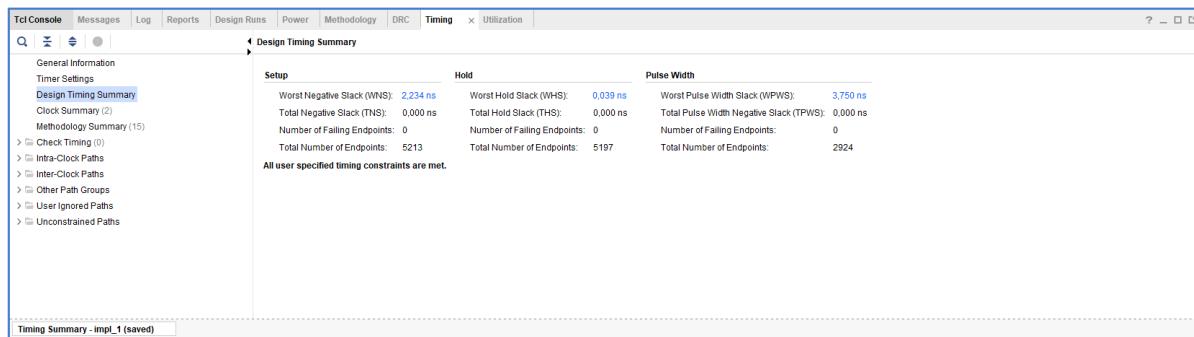
En la primer imagen vemos la distribución del proyecto dentro de la FPGA y tenemos nuevamente los datos de la cantidad de LUTs, Slice registers, RAMs y memorias.

The screenshot shows the Xilinx Vivado 2023.1 software interface. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, Help, and Log. The title bar indicates the project is 'LAB03_Balbo_Ignacio - [C:/DDA2024/Labs/Lab03/LAB03_Balbo_Ignacio/LAB03_Balbo_Ignacio.prj] - Vivado 2023.1'. The left sidebar has sections for SYNTHESIS (Run Synthesis, Open Synthesized Design, Constraints Wizard, Edit Timing Constraints, Set Up Debug, Report Timing Summary, Report Clock Networks, Report Clock Interaction, Report Methodology, Report DRC, Report Noise, Report Utilization, Report Power, Schematic), IMPLEMENTATION (Run Implementation, Open Implemented Design, Constraints Wizard, Edit Timing Constraints, Report Timing Summary, Report Clock Networks, Report Clock Interaction, Report Methodology, Report DRC, Report Noise, Report Utilization, Report Power, Schematic), and FLOW NAVIGATOR (IMPLEMENTED DESIGN - xc7z035bg3g224-1L). The main workspace displays the Project Summary (Device: Arty_Master_tx.xdc, Vivado Log: vivado.log) and the Design Hierarchy (utilization_1). A detailed hierarchy tree under 'top_phy_all' is shown, along with a Source File Properties panel and a Utilization Report table.

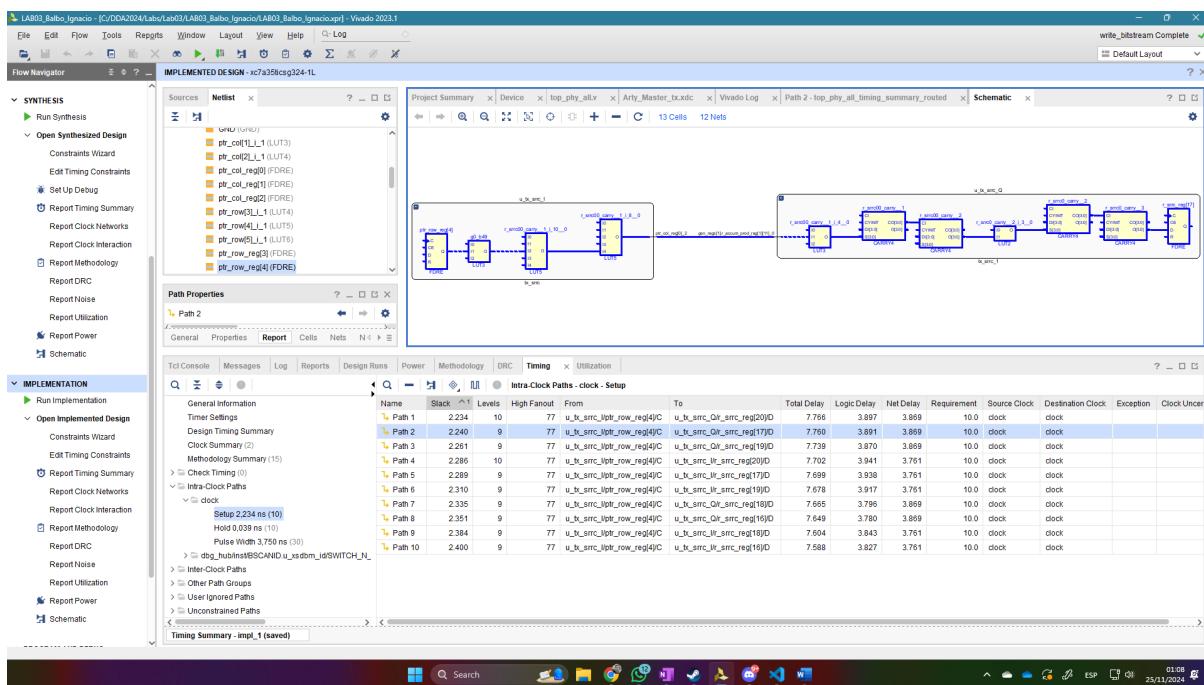
Name	Slice LUTS (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	Block-RAM (50)	DSPs (90)	Bonded I/OB (210)	BUFGCTRL (32)	BSCAN2 (4)
top_phy_all	1817	2678	7	873	1681	136	2.5	1	1	2	1
> dbg_hub (dbg_hub)	472	753	0	239	448	24	0	0	0	1	1
> u_il2_il2 (ila)	792	1341	3	427	682	110	1.5	0	0	0	0
> u_prbsx_ber_Q (prbsx)	1	9	0	2	1	0	0	0	0	0	0
> u_prbsx_ber_Q (prbsx_parameterized0)	4	8	0	2	2	2	0	0	0	0	0
> u_ram_save_Q (ram_save)	16	38	0	17	16	0	0.5	0	0	0	0
> u_ram_save_Q (ram_save_0)	11	28	0	11	11	0	0.5	0	0	0	0
> u_tfcfg (tfcfg)	17	12	0	7	17	0	0	1	0	0	0
> u_t_arcc (t_arcc)	235	85	4	73	235	0	0	0	0	0	0
> u_t_arcc_Q (t_arcc_1)	129	82	0	44	129	0	0	0	0	0	0
> u_vio (vio)	135	296	0	89	135	0	0	0	0	0	0

En el reporte de timing vemos:

Worst negative slack: -2.234ns



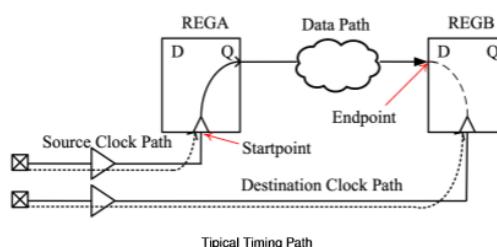
Podemos ver el camino de este tiempo de peor slack, que es el que se muestra en la siguiente imagen.

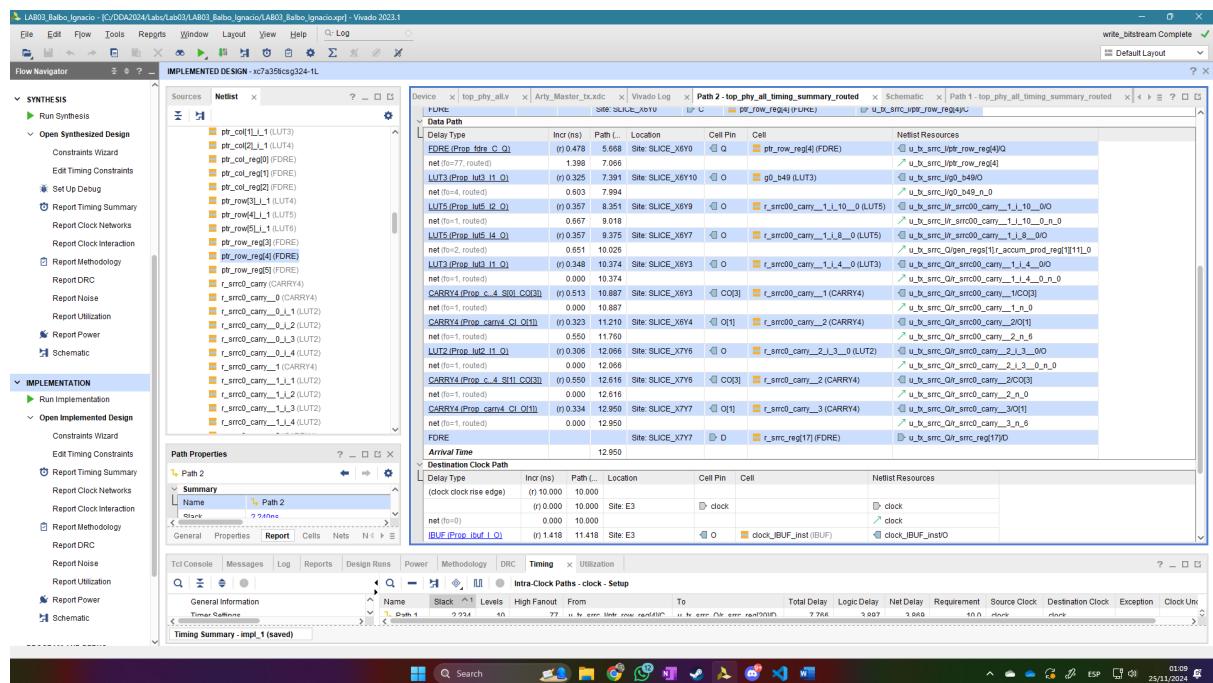
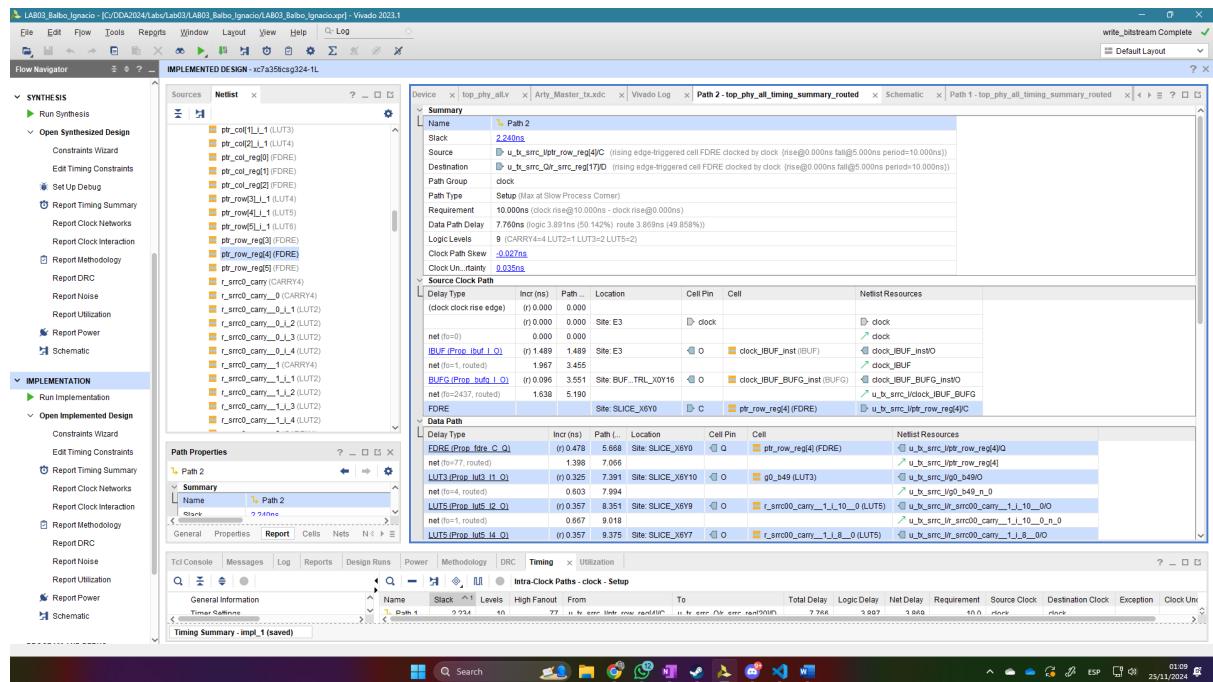


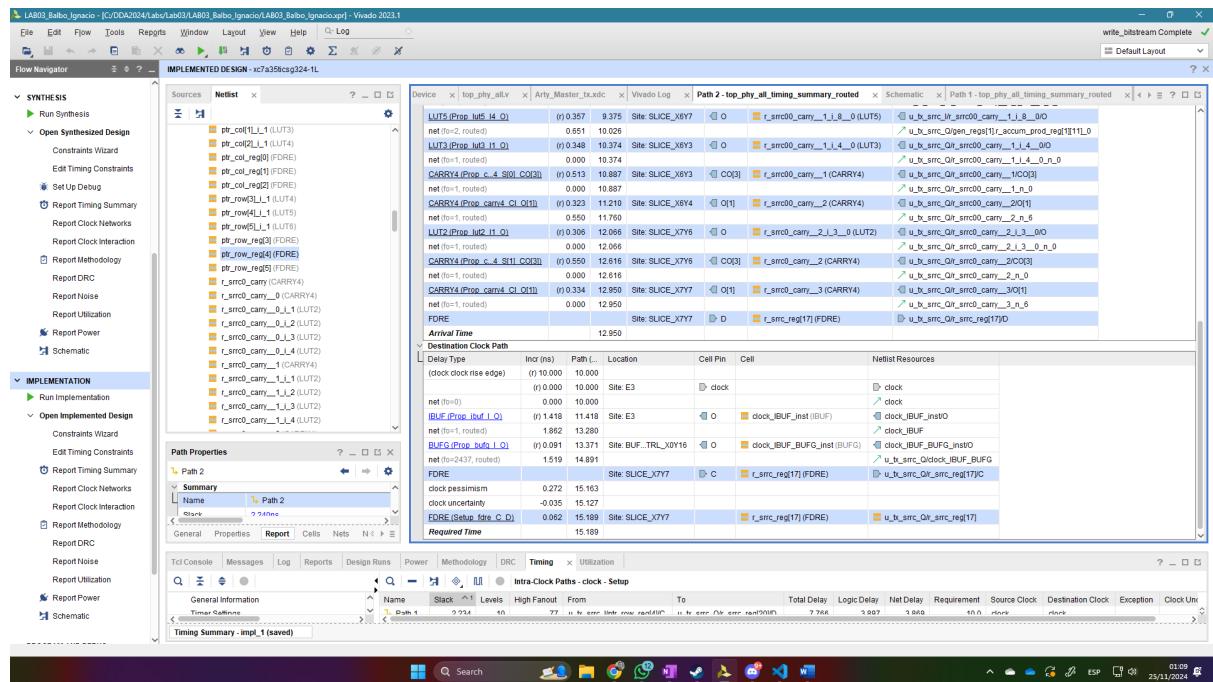
En las siguientes imágenes, tenemos detallado en cada camino los modulos o componentes que atraviesa y también da indicaciones del tiempo que le toma.

Podemos ver las siguientes secciones de interés:

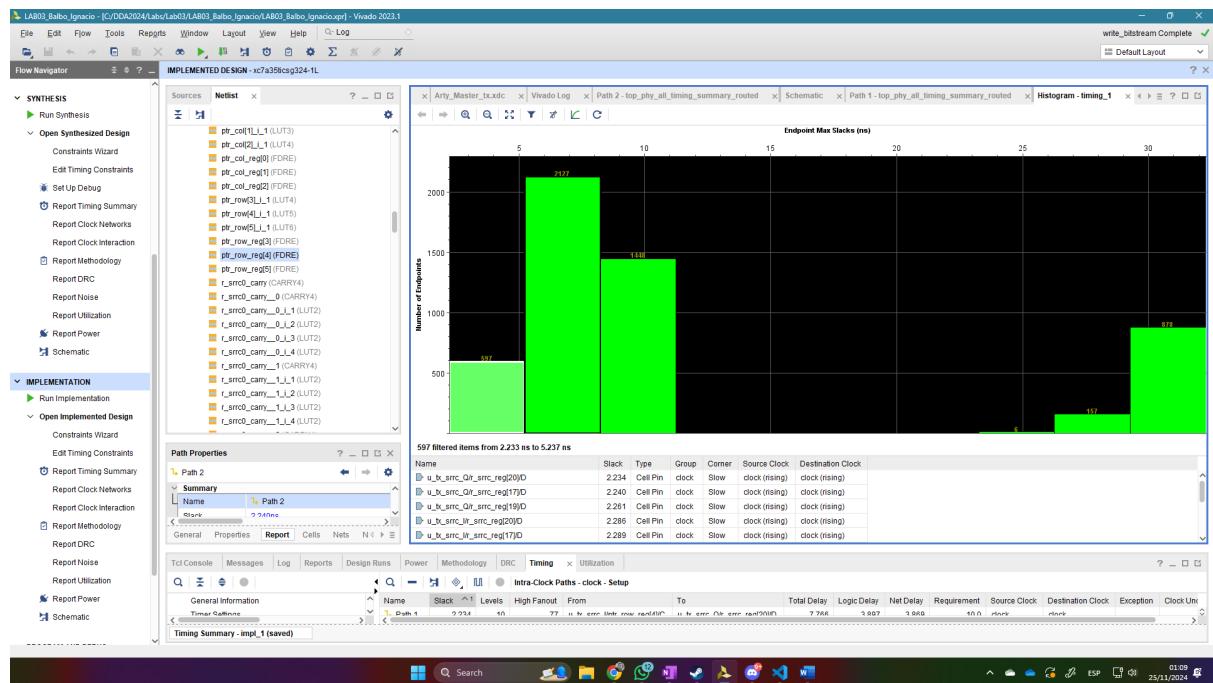
- Source clock path: Puerto de entrada del clock hasta el pin de clock del registro.
- Data Path: camino en el que se propagan los datos
- Destination clock path: origen del reloj hasta el pin del reloj del registro (si es que no termina en un puerto de salida)





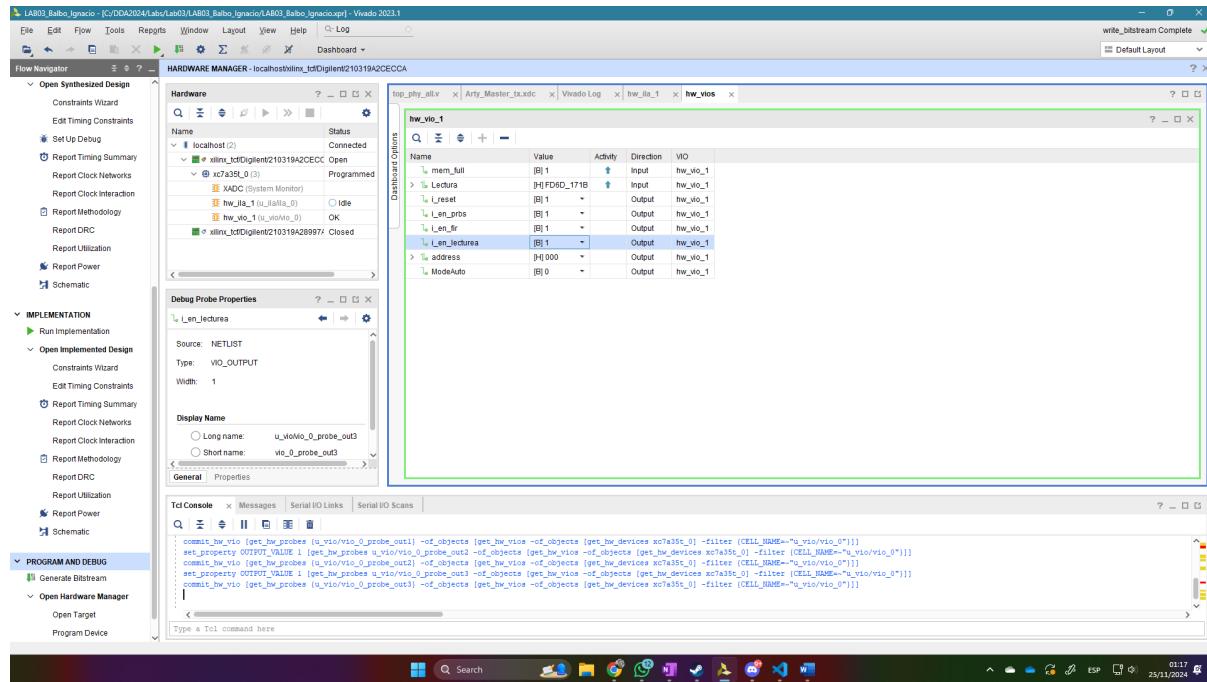


Podemos corroborar el histograma generado:

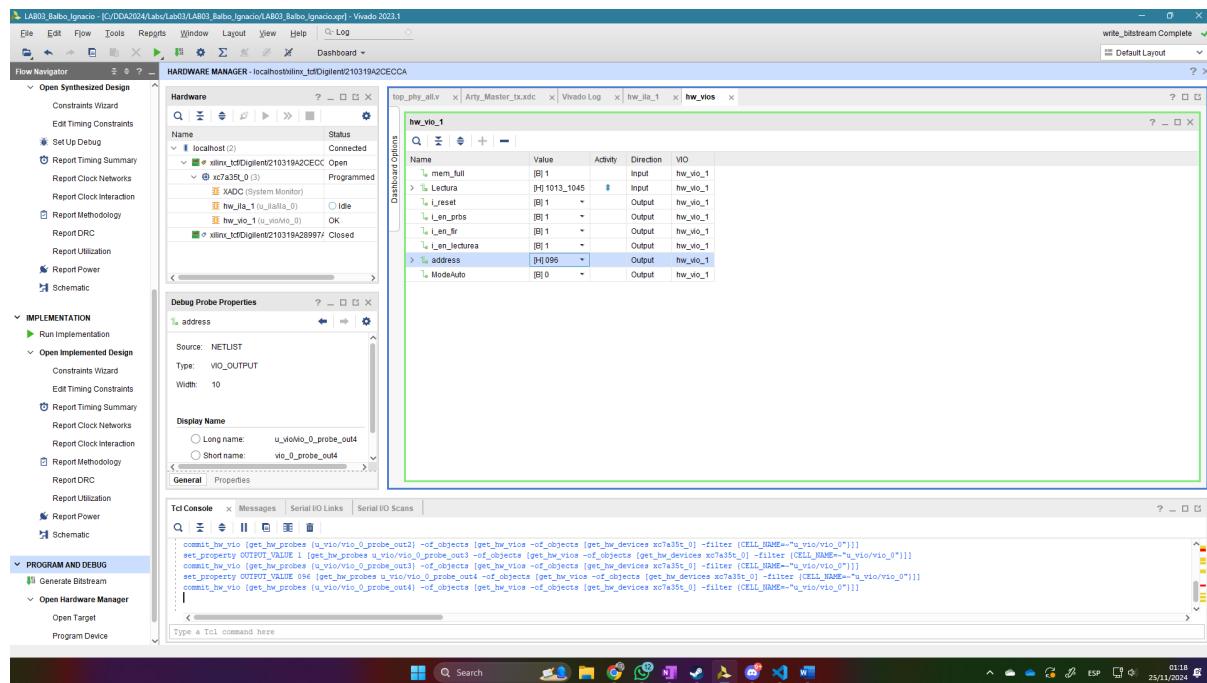


Implementación en FPGA

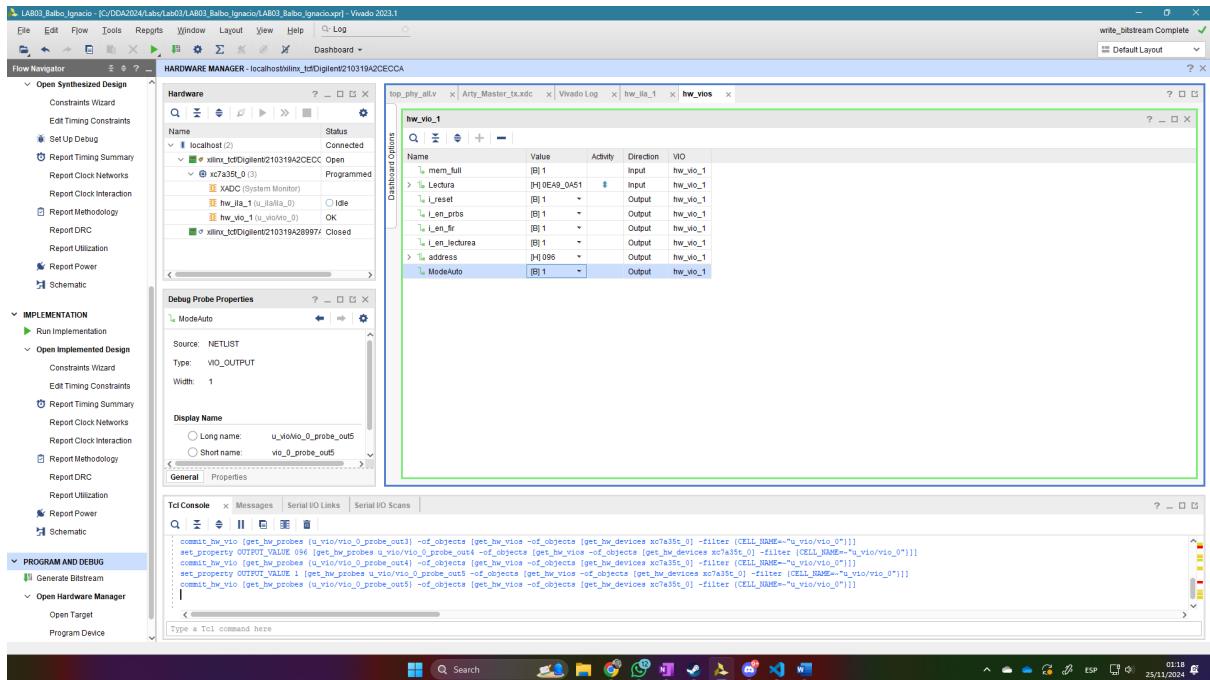
Implementamos y realizamos una lectura individual de cada dato con el bloque de vio.



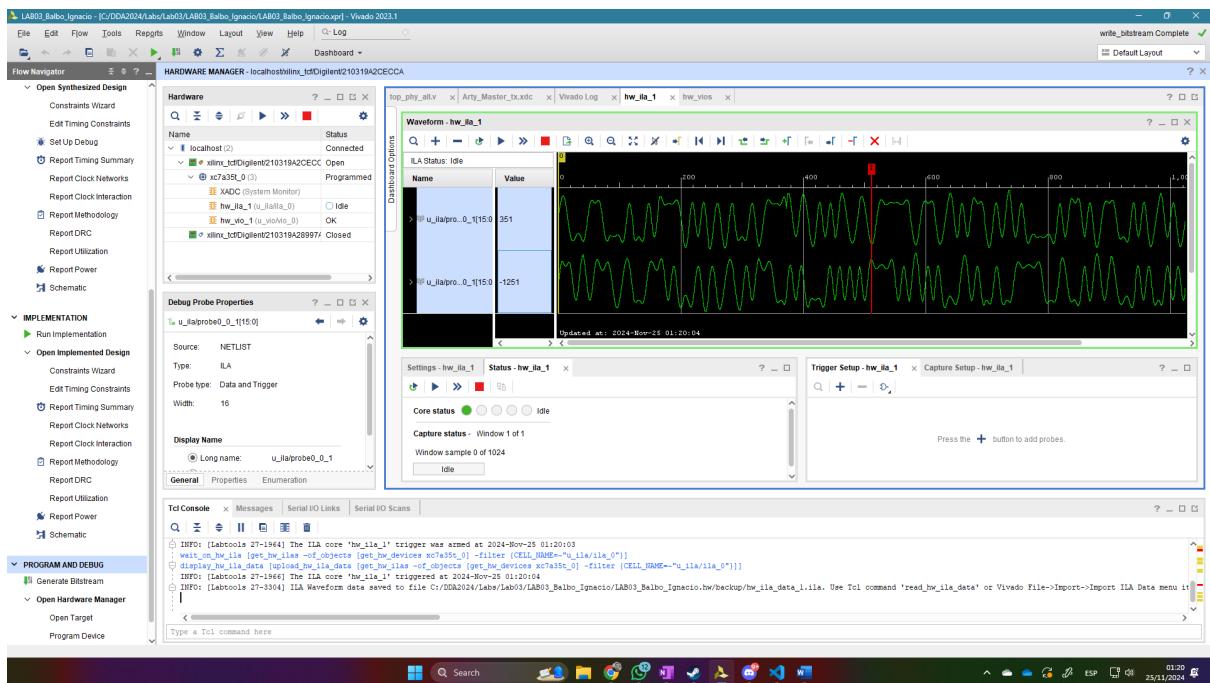
Podemos indicar una dirección de la ram que queremos leer:



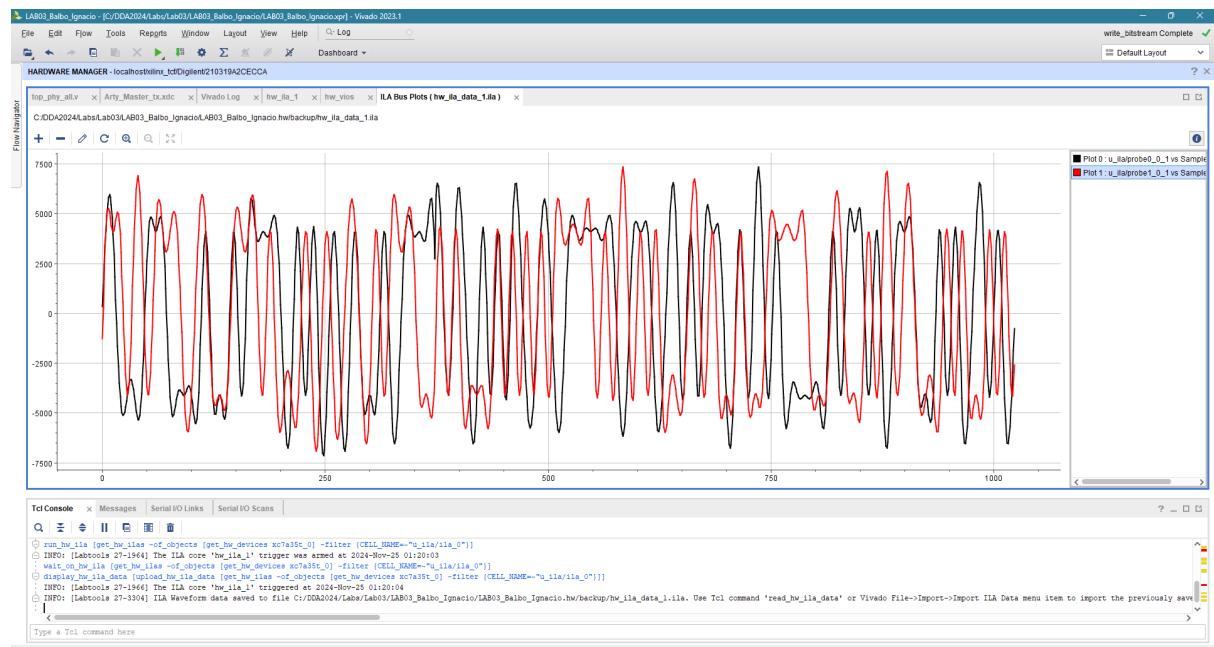
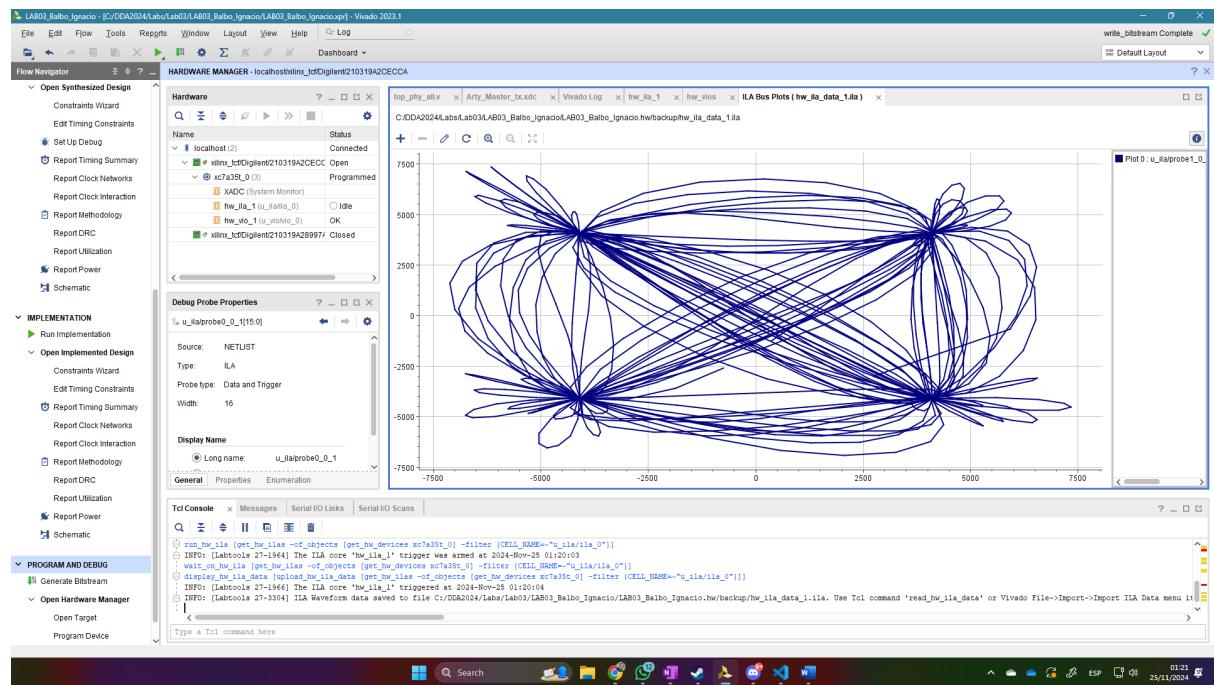
Tambien podemos hacer una lectura automática de los datos:



Utilizando el bloque ila, podemos analizar la generación de los pulsos:



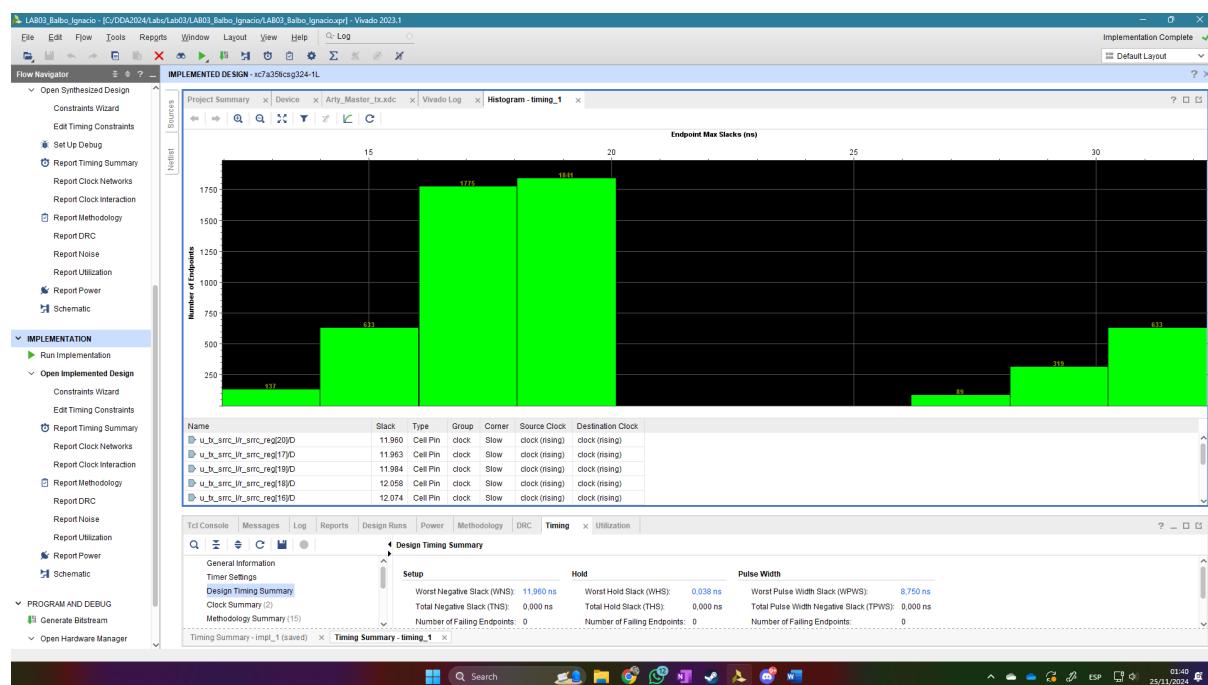
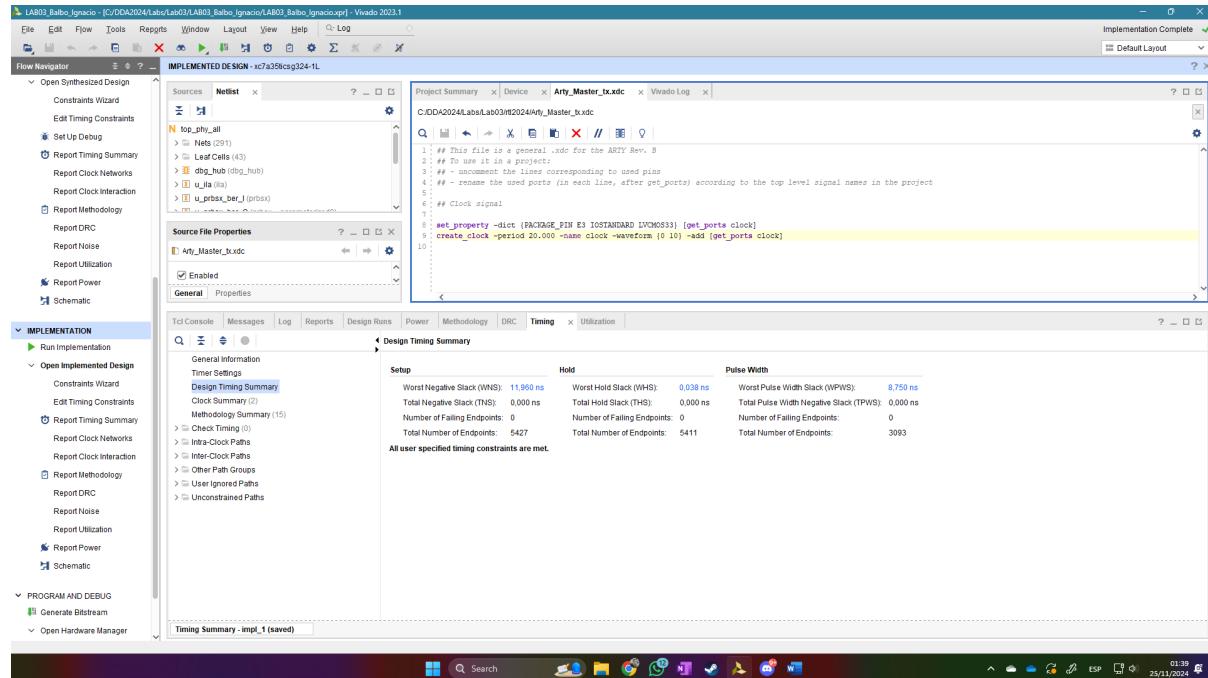
Y también su ploteos.



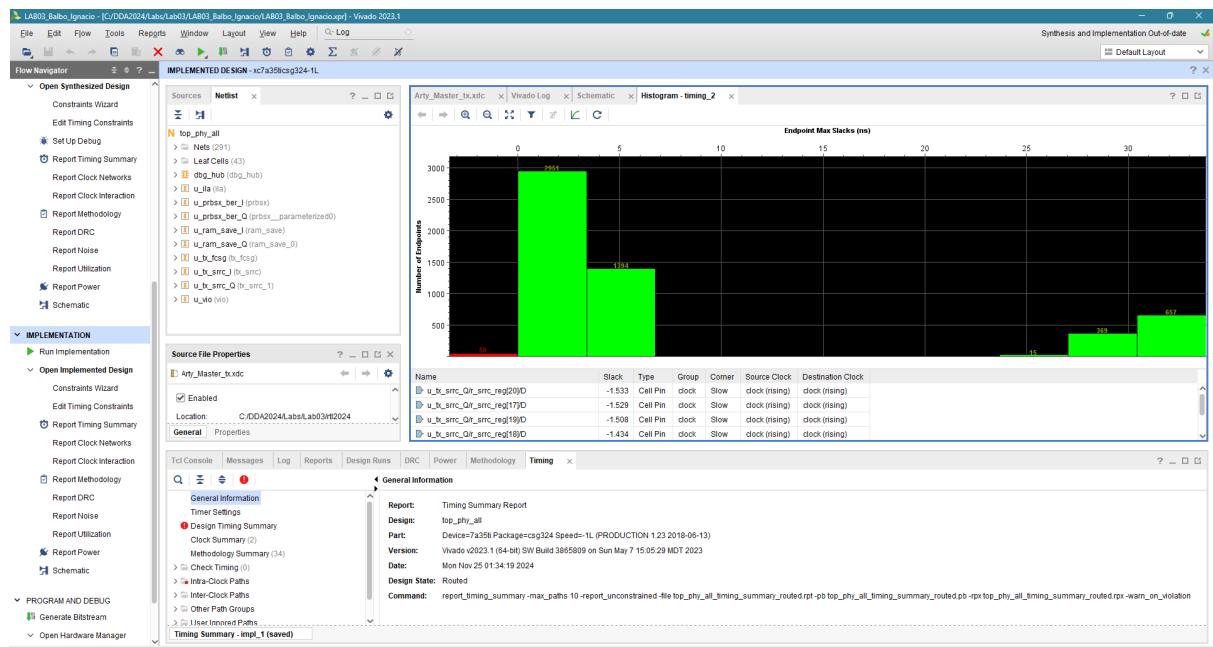
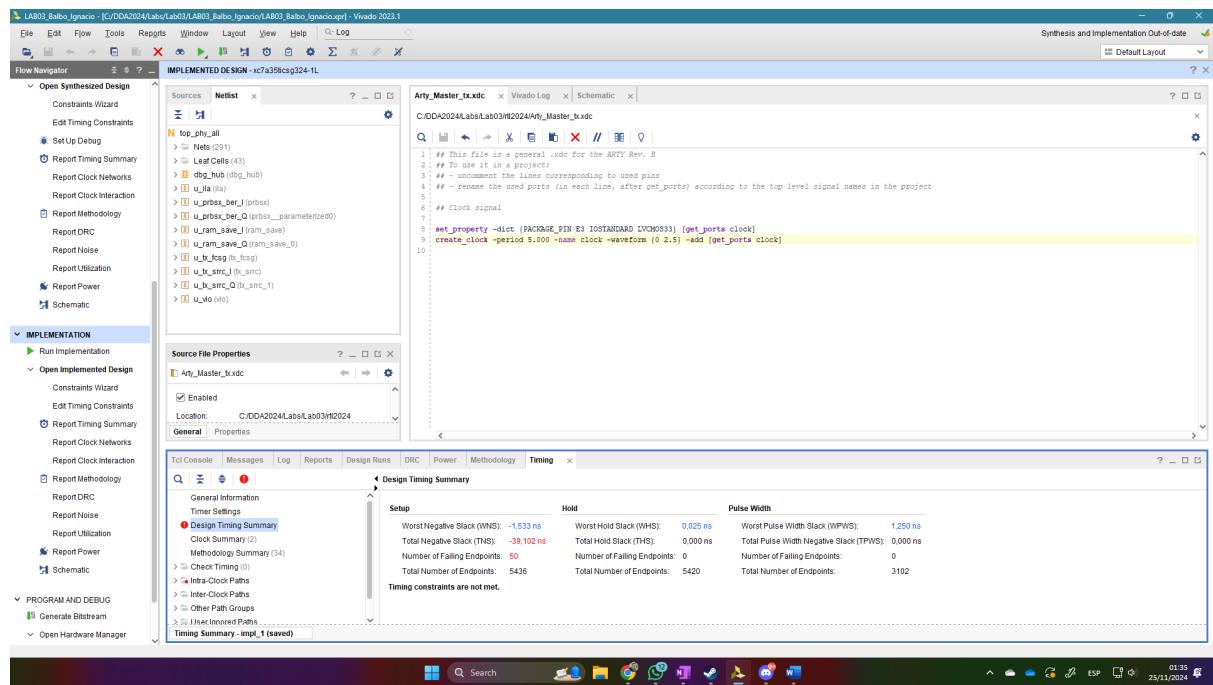
Implementación: variación de clock

Ahora realizamos la implementación nuevamente del sistema y analizamos los resultados obtenidos.

Para un reloj de 50 MHz obtenemos:



Para 200 MHz:



Comparando los slacks

Worst negative slack		
50 MHz	100 MHz	200 MHz
11.96 nS	2.234 ns	-1.533 ns