

Question No. 1

a)	<div><div>Description</div><div>Makes extensive use of general purpose registers</div><div>Many addressing modes are available</div><div>Has a simplified instruction set</div></div> <div><div>Type of processor</div><div>RISC</div><div>CISC</div></div>	3																																																												
b) i)	<div><div>Time Interval</div><table><tr><td>stage</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td></tr><tr><td>Fetch instruction</td><td>A</td><td>B</td><td>C</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>Decode instruction</td><td></td><td>A</td><td>B</td><td>C</td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>Execute instruction</td><td></td><td></td><td>A</td><td>B</td><td>C</td><td></td><td></td><td></td><td></td></tr><tr><td>Access operand in memory</td><td></td><td></td><td></td><td>A</td><td>B</td><td>C</td><td></td><td></td><td></td></tr><tr><td>Write result to register</td><td></td><td></td><td></td><td></td><td>A</td><td>B</td><td>C</td><td></td><td></td></tr></table><div>Completing the As (1 Mark)</div><div>B in column 2, Row 1 (1 Mark)</div><div>Remainder completed (1 Mark)</div></div>	stage	1	2	3	4	5	6	7	8	9	Fetch instruction	A	B	C							Decode instruction		A	B	C						Execute instruction			A	B	C					Access operand in memory				A	B	C				Write result to register					A	B	C			3
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b) ii)	<div>With pipelining no of cycles = 7</div> <div>Without pipelining no of cycles = 3 * 5 = 15</div> <div>No of cycles saved = 8</div>	3																																																												

Question No. 2

a)	1 mark for correct arrow from each description	4										
	<table><thead><tr><th>Description</th><th>Computer Architecture</th></tr></thead><tbody><tr><td>A computer that does not have the ability for parallel processing</td><td>SIMD</td></tr><tr><td>The processor has several ALUs. Each ALU executes the same instruction but on different data.</td><td>MISD</td></tr><tr><td>There are several processors. Each processor executes different instructions drawn from a common pool. Each processor operates on different data drawn from a common pool.</td><td>SISD</td></tr><tr><td>There is only one processor executing one set of instructions on a single set of data.</td><td>MIMD</td></tr></tbody></table>		Description	Computer Architecture	A computer that does not have the ability for parallel processing	SIMD	The processor has several ALUs. Each ALU executes the same instruction but on different data.	MISD	There are several processors. Each processor executes different instructions drawn from a common pool. Each processor operates on different data drawn from a common pool.	SISD	There is only one processor executing one set of instructions on a single set of data.	MIMD
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b) i)	Massive: many/large number of processors // hundreds/thousands of processors	1										
b) ii)	Parallel: to perform a set of coordinated computations in parallel/simultaneously	1										
(c)	<p>processors need to be able to communicate ... so that processed data can be transferred from one processor to another</p> <p>suitable algorithm/program/software/design // appropriate programming language which allows data to be processed by multiple processors simultaneously</p>	4										

Question No. 3

a)	<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>Description</p> <div style="border: 1px solid black; padding: 5px; margin-bottom: 10px;">Most parallel computer systems use this architecture.</div> <div style="border: 1px solid black; padding: 5px; margin-bottom: 10px;">Widely used to process 3D graphics in video games.</div> <div style="border: 1px solid black; padding: 5px; margin-bottom: 10px;">A microprocessor is used to control a washing machine.</div> <div style="border: 1px solid black; padding: 5px;">There are a number of processing units. Each processing unit executes the same instruction but on different data</div> </div> <div style="width: 45%;"> <p>Computer architecture</p> <div style="border: 1px solid black; padding: 5px; margin-bottom: 10px; text-align: center;">SIMD</div> <div style="border: 1px solid black; padding: 5px; margin-bottom: 10px; text-align: center;">MIMD</div> <div style="border: 1px solid black; padding: 5px; margin-bottom: 10px; text-align: center;">MISD</div> <div style="border: 1px solid black; padding: 5px; text-align: center;">SISD</div> </div> </div> <p style="text-align: right; margin-top: 10px;">1 mark for each correct line</p>	4
b)	<div style="display: flex; justify-content: space-between;"> <div style="width: 80%;"> <ul style="list-style-type: none"> <input type="checkbox"/> Only one (separate) processor / not many separate processors (is not massively parallel) <input type="checkbox"/> Quad core computer system // processing units share the same bus </div> <div style="width: 15%; text-align: right;"> <p>1 1 1 mark for each point, max 2</p> </div> </div>	2
c)	<ul style="list-style-type: none"> <input type="checkbox"/> Split into blocks of code <input type="checkbox"/> ... that can be processed simultaneously ... <input type="checkbox"/> ... instead of sequentially <input type="checkbox"/> Each block is processed by a different processor <input type="checkbox"/> which allows each of the many processors to simultaneously process the different blocks of code independently <input type="checkbox"/> Requires both parallelism and co-ordination <p style="text-align: right;">1 mark for each point, max 2</p>	2
d)	<p>1 mark for identification of hardware issue, for example:</p> <ul style="list-style-type: none"> <input type="checkbox"/> Communication between the different processors is the issue <p>1 mark for further explanation from:</p> <ul style="list-style-type: none"> <input type="checkbox"/> Each processor needs a link to every other processor <input type="checkbox"/> Many processors require many of these links <input type="checkbox"/> Challenging topology 	2

Question No. 4

a)	<table><thead><tr><th>Description</th><th>Type of processor</th></tr></thead><tbody><tr><td>It has a simplified set of instructions.</td><td rowspan="2">CISC</td></tr><tr><td>Emphasis is on the hardware rather than the software.</td></tr><tr><td>It makes extensive use of general purpose registers.</td><td rowspan="2">RISC</td></tr><tr><td>Many instruction formats are available.</td></tr></tbody></table> <p>1 mark for each correct line</p>	Description	Type of processor	It has a simplified set of instructions.	CISC	Emphasis is on the hardware rather than the software.	It makes extensive use of general purpose registers.	RISC	Many instruction formats are available.	3																																																							
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b) i)	<p>One mark per point – max 2</p> <ul style="list-style-type: none">• Pipelining is instruction level parallelism• Execution (A: processing) of an instruction is split into a number of stages• When first stage for an instruction is completed the first stage of the next instruction can start executing• Another instruction can start executing before the previous one is finished• Processing of a number of instructions can be concurrent / simultaneous	3																																																															
b) ii)	<table><thead><tr><th></th><th colspan="8">Time Interval</th></tr><tr><th>Stage</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th></tr></thead><tbody><tr><td>Fetch instruction</td><td>D</td><td>E</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>Read registers and decode instruction</td><td></td><td>D</td><td>E</td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>Execute instruction</td><td></td><td></td><td>D</td><td>E</td><td></td><td></td><td></td><td></td></tr><tr><td>Access operand in memory</td><td></td><td></td><td></td><td>D</td><td>E</td><td></td><td></td><td></td></tr><tr><td>Write result to register</td><td></td><td></td><td></td><td></td><td>D</td><td>E</td><td></td><td></td></tr></tbody></table> <p>D at time interval 1 (1) D and E in second row (in that order) (1) Remainder completed correctly (1)</p>		Time Interval								Stage	1	2	3	4	5	6	7	8	Fetch instruction	D	E							Read registers and decode instruction		D	E						Execute instruction			D	E					Access operand in memory				D	E				Write result to register					D	E			3
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c) i)	Two from: <ul style="list-style-type: none">• The result of the first addition is not stored in (register) r3 (1)• Before the next instruction needs to load value from r3 (1)• There is a data dependency issue (1)• r3 is being fetched and stored on the same clock pulse (1)	3
c) ii)	The third instruction is not dependent on the first two, therefore, instruction 2 and 3 need to be swapped	3

Question No. 5

a)	<p>1 mark per bullet point to max 4:</p> <ul style="list-style-type: none">• RISC has fewer instructions // CISC has more instructions• RISC has many registers // CISC has few registers• RISCs instructions are simpler // CISC's instructions are more complex• RISC has a few instruction formats // CISC has many instruction formats• RISC usually uses single-cycle instructions // CISC uses multi-cycle instructions• RISC uses fixed-length instructions // CISC uses variable-length instructions• RISC has better pipelineability // CISC has poorer pipelineability• RISC requires less complex circuits // CISC requires more complex circuits• RISC has fewer addressing modes // CISC has more addressing modes• RISC makes more use of RAM // CISC makes more use of cache/less use of RAM• RISC has a hard-wired control unit // CISC has a programmable control unit• RISC only uses load and store instructions to address memory // CISC has many types of instructions to address memory	4																																																																					
b) i)	<p>1 mark per bullet point:</p> <ul style="list-style-type: none">• Completing the As correctly• B in column 2, row 1 no other Bs in row 1• Remainder correctly completed <table><tr><th rowspan="2">Stage</th><th colspan="9">Time interval</th></tr><tr><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th></tr><tr><td>Fetch instruction</td><td>A</td><td>B</td><td>C</td><td>D</td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>Decode instruction</td><td></td><td>A</td><td>B</td><td>C</td><td>D</td><td></td><td></td><td></td><td></td></tr><tr><td>Execute instruction</td><td></td><td></td><td>A</td><td>B</td><td>C</td><td>D</td><td></td><td></td><td></td></tr><tr><td>Access operand in memory</td><td></td><td></td><td></td><td>A</td><td>B</td><td>C</td><td>D</td><td></td><td></td></tr><tr><td>Write result to register</td><td></td><td></td><td></td><td></td><td>A</td><td>B</td><td>C</td><td>D</td><td></td></tr></table>	Stage	Time interval									1	2	3	4	5	6	7	8	9	Fetch instruction	A	B	C	D						Decode instruction		A	B	C	D					Execute instruction			A	B	C	D				Access operand in memory				A	B	C	D			Write result to register					A	B	C	D		3
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b) ii)	<p>1 mark per bullet point:</p> <ul style="list-style-type: none">• Correct number of cycles for pipelining 8• Correct number of cycles without pipelining $4 \times 5 = 20$• No of cycles saved $20 - 8 = 12$	3																																																																					
c)	<p>1 mark for each row</p> <table><tr><th rowspan="2">Statement</th><th colspan="3">Architecture</th></tr><tr><th>SIMD</th><th>MIMD</th><th>SISD</th></tr><tr><td>Each processor executes a different instruction</td><td></td><td>✓</td><td></td></tr><tr><td>There is only one processor</td><td></td><td></td><td>✓</td></tr><tr><td>Each processor executes the same instruction input using data available in the dedicated memory</td><td>✓</td><td></td><td></td></tr><tr><td>Each processor typically has its own partition within a shared memory</td><td></td><td>✓</td><td></td></tr></table>	Statement	Architecture			SIMD	MIMD	SISD	Each processor executes a different instruction		✓		There is only one processor			✓	Each processor executes the same instruction input using data available in the dedicated memory	✓			Each processor typically has its own partition within a shared memory		✓		4																																														
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Question No. 6

a)	1 mark for 2/3 rows correct 2 marks for 4/5 rows correct 3 marks for 6 correct rows	<table><tr><th>Statement</th><th>RISC</th><th>CISC</th></tr><tr><td>Larger instruction set</td><td></td><td>✓</td></tr><tr><td>Variable length instructions</td><td></td><td>✓</td></tr><tr><td>Smaller number of instruction formats</td><td>✓</td><td></td></tr><tr><td>Pipelining is easier</td><td>✓</td><td></td></tr><tr><td>Microprogrammed control unit</td><td></td><td>✓</td></tr><tr><td>Multi-cycle instructions</td><td></td><td>✓</td></tr></table>	Statement	RISC	CISC	Larger instruction set		✓	Variable length instructions		✓	Smaller number of instruction formats	✓		Pipelining is easier	✓		Microprogrammed control unit		✓	Multi-cycle instructions		✓	3
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b) i)	1 mark per bullet point <input type="checkbox"/> SISD // Single instruction single data <input type="checkbox"/> SIMD // Single instruction multiple data <input type="checkbox"/> MISD // Multiple instruction single data <input type="checkbox"/> MIMD // Multiple instruction multiple data		4																					
b) ii)	1 mark per bullet point (max 3) <input type="checkbox"/> Large number of processors <input type="checkbox"/> ... working collaboratively on the same program <input type="checkbox"/> ... working together simultaneously on the same program <input type="checkbox"/> ... communicating via a messaging interface		3																					

Question No. 7

a)	1 mark for each correct term		4
	Description	Term	
	<ul style="list-style-type: none">There are several processors.Each processor executes different sets of instructions on one set of data at the same time.	MISD	
	<ul style="list-style-type: none">The processor has several ALUs.Each ALU executes the same set of instructions on different sets of data at the same time.	SIMD	
	<ul style="list-style-type: none">There is only one processor.The processor executes one set of instructions on one set of data.	SISD	
b)	1 mark per bullet point to max 3		3
	<ul style="list-style-type: none">A large number of processorsCollaborative processing // coordinated simultaneous processingNetwork infrastructureCommunicate using a message interface / by sending messages		

Question No. 8

-	<ul style="list-style-type: none">• RISC / reduced instruction set computer• CISC / complex instruction set computer• Pipelining	3
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Question No. 9

a)	Max three , one mark for role, one mark for expansion OS1, OS2 and OS3 are guest operating systems ... secondary to the one installed on the hardware OS4 is the host operating system ... interacts directly with the machine hardware MyApp needs to run on all three guest operating systems with identical results	3
b)	Any three from Create/delete/manage virtual machine Translate instructions used by guest operating system to that required by host operating system Hardware emulation Protecting each virtual machine ... so instances of MyApp can be tested together	3
c)	One mark for benefit and one mark for relevant explanation One mark for drawback one mark for relevant explanation For example: Benefit: multiple operating systems can exist simultaneously ... allowing for testing using the same hardware only one set of hardware required ... reduces cost of producing the app // no need to set up more than one computer Drawback: execution of extra code ... so performance is degraded // more time taken to execute the app // cannot make judgements about response time etc	4

Question No. 10

-	Software / a program Physical / different Guest Host	4
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Question No. 11

a) i)	Examples: Create / delete virtual machine Existing hardware made available to guest OS // hardware emulation Ensures each virtual machine is protected from actions of another virtual machine	2
a) ii)	Guest operating system: An operating system running in a virtual machine // Controls virtual hardware // OS is being emulated Host operating system: The operating system that is actually controlling the physical hardware // the operating system for the physical machine// the OS running the VM software Guest OS is running under the Host OS software	2
b) i)	Examples: Trial/use alternative replacement operating system(s) ... Test to identify possible problems Much easier to create VM with a new OS than create new computer system Trial/use alternative replacement web server software ... Test to identify possible problems Easier to try alternative new software <u>and</u> new OS combinations To provide some additional service(s) Trial/test its use - description e.g. a print server General description point – to provide a safe environment during testing (which does not disrupt the web server service)	4
b) ii)	Examples: Using virtual machine means execution of extra code // emulation of some hardware ... Non-VM installation may not perform in the same way Execution speed slower than non-VM system Problems in judging actual response times at time of maximum traffic needs fastest possible speed Particular hardware may be difficult to emulate	2

Question No. 12

a) i)	A: Guest (operating system) (1) B: Host (operating system) (1)	2
a) ii)	One mark for each valid point, max 3 <ul style="list-style-type: none">• Guest OS (A) handles request as if it were running on its own physical machine // guest OS (A) is not aware it is running on a virtual platform• Guest OS (A) handles the request as usual• I/O requests are translated by the virtual machine software• Into instructions executed by host OS (B)• Host OS (B) retrieves the data from the file• Host OS (B) passes the data to the virtual machine software• The virtual machine software passes the data to the guest OS (A)• Guest OS passes the data to the application	3
b) i)	One mark from: <ul style="list-style-type: none">• Because software can be tried on different OS using same hardware• Because no need to purchase / request all sorts of different hardware• Easier to recover if software causes system crash• VM provides protection to other software / host OS from malfunctioning software	1
b) ii)	Max 2 marks per limitation, max 2 limitations – max 4 marks Virtual machine may not be able to emulate some hardware ... So that hardware cannot be tested using a virtual machine ... By relevant example, e.g. developing hardware drivers Using virtual machine means execution of extra code // processing time increased ... so cannot accurately test speed of real performance A virtual machine might not be as efficient ... By relevant example, e.g. might not be able to access sufficient memory	4

Question No. 13

	<p>One mark for each benefit to max 2 from</p> <ul style="list-style-type: none">• Because software can be tried on different OS (using same hardware)• Because no need to purchase / request all sorts of different hardware• Easier to recover if software causes system crash• VM provides protection to other software / host OS from malfunctioning software <p>One mark for each limitation to max 2 from</p> <ul style="list-style-type: none">• Virtual machines may not be able to emulate some hardware• Virtual machines cannot directly access some hardware• Using virtual machine means execution of extra code // processing time increased• A virtual machine might not be as efficient // performance degrades• Use of a virtual machine increases the maintenance overheads	4
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