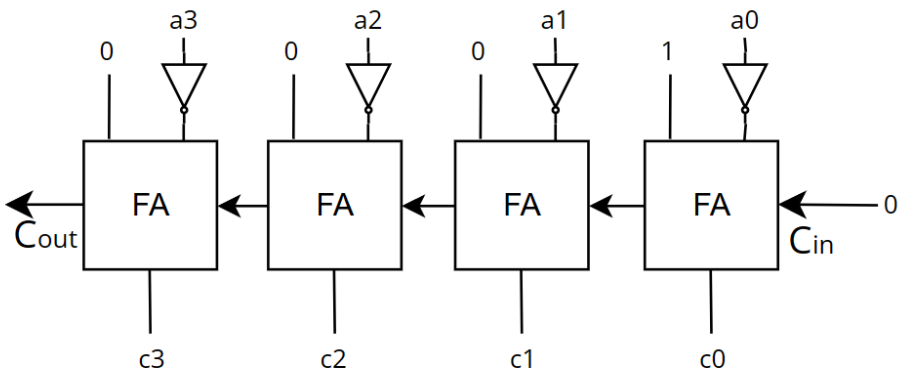
Problem Set – 2

CS 230, Spring 2023

Questions

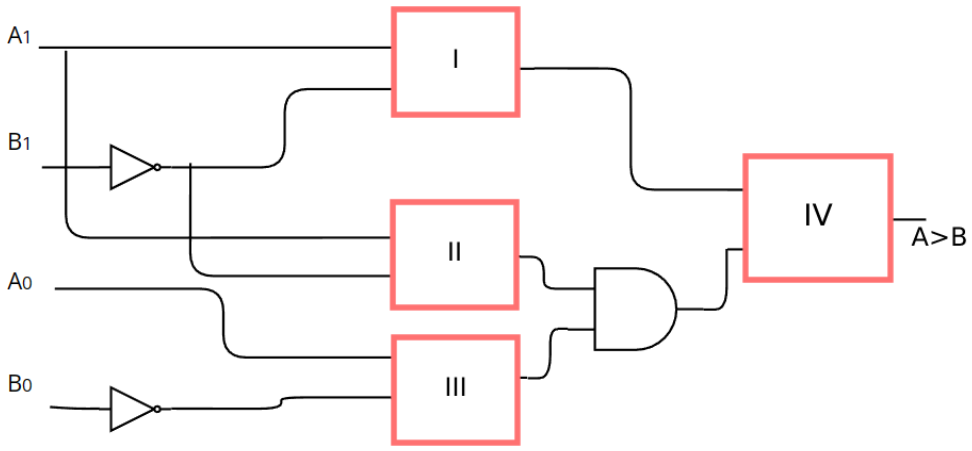
1. Consider a full-binary subtractor that accepts three input bits *a*, *b*, and B_{in}, and outputs *c* and B_{out}. *a* and *b* are the operands for the subtraction operation and B_{in} is the borrow taken by the previous digit. *c* is the resulting bit for the operation *(a - b)* and B_{out} is the borrow taken from the next digit for the subtraction. Then the boolean expression for *c* and B_{out} is:
   a. $c = \bar{a} \oplus b \oplus B_{in}\ ;\ B_{out} = \bar{a}B_{in} + a\bar{b} + bB_{in}$
   b. $c = a \oplus \bar{b} \oplus B_{in}\ ;\ B_{out} = \bar{a}B_{in} + \bar{a}b + bB_{in}$
   c. $c = a \oplus b \oplus B_{in}\ ;\ B_{out} = \bar{a}B_{in} + \bar{a}b + bB_{in}$
   d. $c = a \oplus b \oplus B_{in}\ ;\ B_{out} = \bar{a}B_{in} + \bar{a}b + b\overline{B_{in}}$

2. Consider the following logic circuit. Suppose binary numbers are represented in 2's complement form.



   a. What is the output $C = c_3c_2c_1c_0$ for input $A = 0101$?
   b. What does the above circuit do?
      i. Outputs $A + 1$
      ii. Outputs $\bar{A}$
      iii. Outputs $-A$
      iv. Outputs $-A + 1$

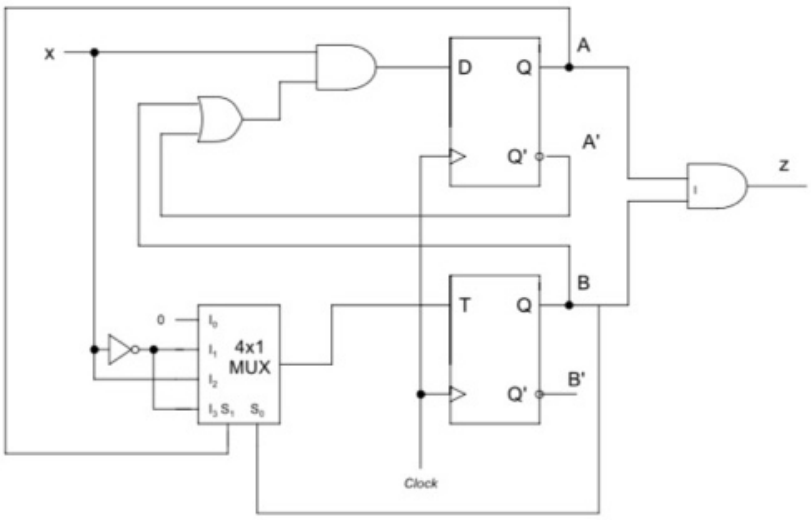
3. You have to design a two bit greater than comparator logic circuit ($A > B$). Following incomplete circuit is provided to you. Name appropriate logic gate for each red box to complete the circuit.



4. A toggle flip-flop (T flip-flop) toggles its output when the input T = 1 during clock signal transition. For input T = 0, the output remains same. The state table of T flip-flop is as follows:

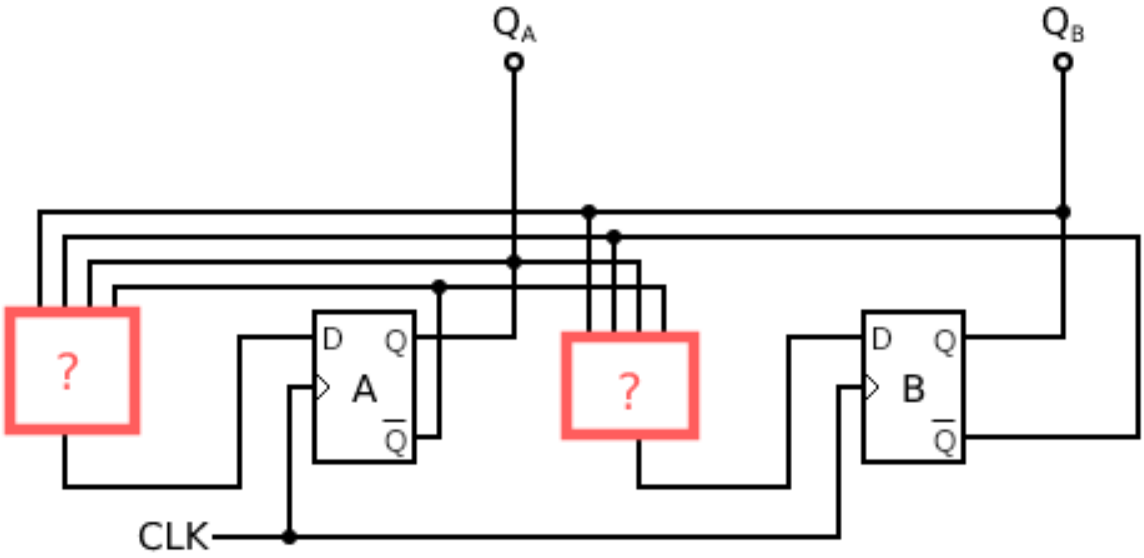
T	**Q_n**	**Q_{n+1}**	
0	0	0	Unchanged/hold
0	1	1	Unchanged/hold
1	0	1	Toggle
1	1	0	Toggle

Complete the state table of the following circuit.



Current State		Input	Next State		Output
A	B	x	A	B	z
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

5. You have to design a 2 bit mod 3 binary counter using D flip-flops. The counter should follow the following sequence:
   0, 1, 2, 0, 1, 2, 0……
   You are given the following circuit.



   Write the Boolean expression for D_A *and* D_B in terms of $Q_A, \overline{Q_A}, Q_B$ *and* $\overline{Q_B}$ to complete the circuit.

6. What is the minimum number of D flip-flops to design a counter for the sequence 0, 0, 1, 1, 2, 2, 3, 3, 4, 4, 5, 5, 6, 6, 7, 7, 0, 0, 1, 1…?