# Problem Set - 4
CS 230, Spring 2023

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1. Let $T_1$ and $T_2$ denote the execution time for pipeline and non pipelined mode respectively.
   Which of the following is true for a single instruction execution?

   (a) $T_1 > T_2$

   (b) $T_1 \geq T_2$

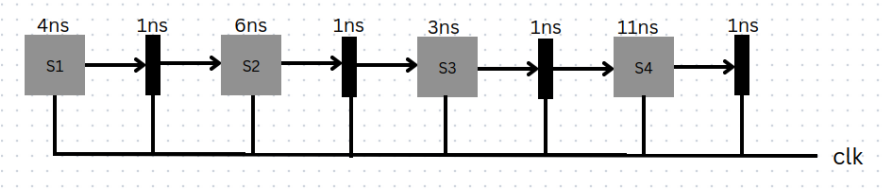
   (c) $T_1 < T_2$

   (d) $T_1 \leq T_2$

2. Consider two pipelines A and B where pipeline A is having 8 stages of uniform delay of 2ns and pipeline B is having 5 stages with respective delays of 2ns, 4ns, 6ns, 3ns and 2ns. How much time is saved using pipeline A instead of B when 100 instructions are executed?

3. Consider a 4 stage pipeline with respective delays of 20ns, 40ns, 30ns and 50ns. Interface registers are used between the stages and have a delay of 2ns. What is the speedup and efficiency of pipeline?
   Efficiency of a pipeline is the ratio of speedup to the ideal speedup of pipeline.

4. Consider the following pipeline

   What is the performance gain of the pipeline when very large number of instructions are pipelined?

5. Consider a 4 stage (IF,ID,EX,WB) pipeline used to execute the following code. In the pipeline, operand forwarding technique is used as an optimization to handle data hazards. All the instructions are spending 1 cycle on all the stages but MUL instruction takes 3 cycles and DIV instruction takes 5 cycles on EX stage.

$$I_0 : DIV \;\; r_0, r_1, r_2$$

$$I_1 : MUL\ r_3, r_2, r_4$$

$$I_2 : ADD\ r_4, r_3, r_2$$

$$I_3 : SUB\ r_5, r_4, r_2$$

(a) How many cycles are needed to complete the code with optimization?

(b) How many cycles are saved to run the code with optimization over without optimization?

6. Consider a 5 stage pipeline with 2ns clock that supports Branch instructions. Processor stops fetching the following instructions after branch instruction is executed. Target address is available in the pipeline when branch instruction execution is completed. Program contains 30% branch instructions. Among them 40% are conditional in which 60% of instructions don't satisfy the condition. When the condition is false, the following instructions are overlapped.

   (a) What is the average instruction execution time?

   (b) What is the speedup?