Problem Set 4 Solutions

CS 230, Spring 2023

1. B) $T_1 \geq T_2$

In pipelined CPU, there will be buffer delay and stage delay. So for 1 instruction nonpipelined CPU takes less time compared to pipelined CPU.

2. Pipeline A (Uniform Delay)

$$K = 8, t_p = 2ns, n=100$$

$$ET_A = (k+n-1)t_p$$

$$= (8+100-1)2$$

= 214 ns

Pipeline B (Non-uniform Delay)

$$k = 5$$
, $t_p = max(2, 4, 6, 3, 2) = 6ns$, $n=100$

$$ET_B = (k+n-1)t_p$$

$$= (5+100-1)6$$

$$= 624 ns$$

Time saved = 624-214 = 410ns

3. k = 4

 $t_p = \max(\text{stage delay} + \text{buffer delay})$

 $= \max(22,42,32,50)$ [Last stage does not have a buffer]

$$= 50 ns$$

$$t_n = 20 + 40 + 30 + 50 = 140 \text{ns}$$

Speedup (S) =
$$\frac{t_n}{4} = \frac{140}{50} = 2.8$$

Speedup (S) =
$$\frac{t_n}{t_p} = \frac{140}{50} = 2.8$$

Efficiency $(\eta) = \frac{S}{k} = \frac{2.8}{4} = 70\%$

4. k = 4

 $t_p = max(stagedelay + bufferdelay)$

 $= \max(5,7,4,12)$ [Here buffer is given at last stage explicitly]

$$= 12ns$$

$$t_n = 4+6+3+11 = 24$$
ns

Speedup =
$$\frac{t_n}{t_p} = \frac{24}{12} = 2$$

5. We have the following data dependencies:

$$I3 \rightarrow I2$$

With Operand Forwarding

	CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8	CC9	CC10	CC11	CC12	CC13
11	IF	ID	EX	EX	EX	EX	EX	WB					
12		IF	ID	ID	ID	ID	ID	EX	EX	EX	WB		
13			IF	IF	IF	IF	IF	ID	ID	ID	EX	WB	
14								IF	IF	IF	ID	EX	WB

= 13 cycles

Without Operand Forwarding

	CC1	CC2	ССЗ	CC4	CC5	CC6	сс7	CC8	СС9	CC10	CC11	CC12	CC13	CC14	CC15	CC16	CC17
11	IF	ID	EX	EX	EX	EX	EX	WB									
12		IF	ID	ID	ID	ID	ID	EX	EX	EX	WB						
13			IF	IF	IF	IF	IF	ID	ID	ID	ID	ID	EX	WB			
14								IF	IF	IF	IF	IF	ID	ID	ID	EX	WB

= 17 cycles

Thus, 4 cycles are saved

6. #stalls/Instruction =
$$0.3*0.6*4 + 0.3*0.4*0.4*4$$

= 0.192

Avg Instruction
$$ET_pipeline = (1 + \#stalls/instruction)t_p = (1+0.912)2ns$$

$$= 3.82 ns$$

Speedup =
$$\frac{k}{1 + \#stalls/instruction} = \frac{5}{1.912} = 2.61$$