# Python-based Verification of Asynchronous FIFO in Vyoma's Up Tick Pro Platform

Karthik Banakar
RTL Design, Modernize Chip Solutions Pvt Ltd
Hyderabad, India
karthikmb8@gmail.com

***Abstract*—Abstract—Most RTL designs are verified with Verilog, SystemVerilog, or UVM. Python programming because of its robustness shall be used in this paper to verify the Asynchronous FIFO's functionality and detect potential defects. The Vyoma Up Tick Pro platform, which provides the predefined python libraries needed for verification, is used to accomplish this project.***

***Keywords*—verification, python, asynchronousfifo, verilog, Vyoma UPTickPro, cdc**

## I. Description

Every digital circuit contains flip-flops, and the majority of SoCs concentrate on circuits with a single clock domain. Multiple data signals operating in different clock domains are being used by modern SoCs. When a signal is transferred from one clock domain to another clock domain, a clock crossing occurs. The data is asynchronous to the new clock domain and may not be sampled effectively in the destination domain, leading to metastability. Some sort of synchronization is necessary for these signals to be effectively acknowledged. Asynchronous FIFOs are thus used to synchronize the transition from the source clock domain to the destination clock domain.

## II. Verification

The design under test (DUT) comprises a FIFO memory and two distinct clock domains, each with its own reset. A write pointer is used to write the data into FIFO memory whereas a read pointer is used to read the data from it. Only when the ready and valid signals are high, the transaction will take place. Thus, input data is sent through this asynchronous FIFO, which operates in the ffi_clk domain, before being synchronized to the ffo_clk domain at the destination port. Moreover, the input parameters VALID, READY, and RESET will be varied, and the output coverage will be analyzed.

## III. Diagrams

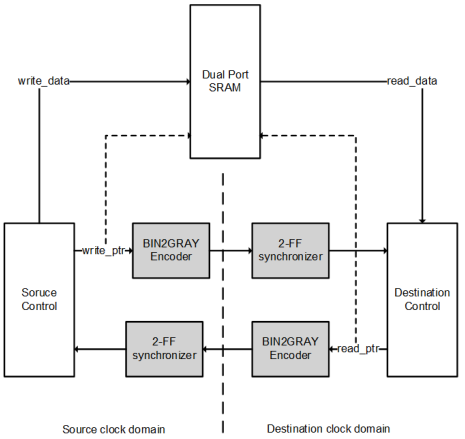


Fig. 1. Block diagram of Asynchronous FIFO

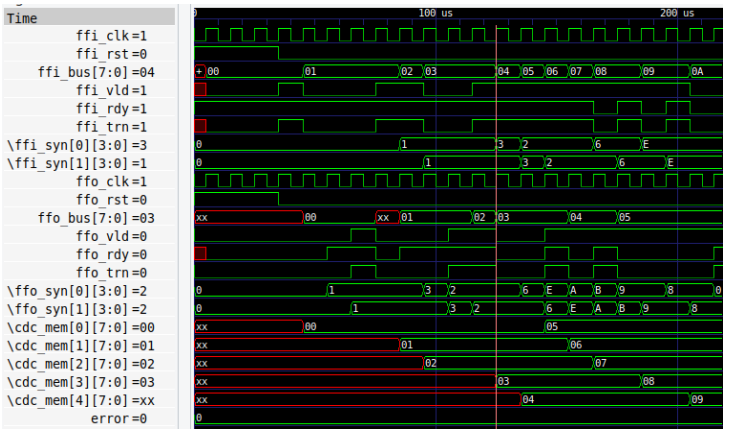


Fig. 2. Example of data transaction from ffi_clk domain to ffo_clk domain

## References

[1] https://anysilicon.com/clock-domain-crossing-cdc/
[2] Clifford E. Cummings, "Clock Domain Crossing (CDC) Design & Verification Techniques Using SystemVerilog", Sunburst Design, Inc.
[3] https://github.com/jeras/sockit_cdc
[4] https://vyomasystems.com