A BiCMOS Dynamic Multiplier Using Wallace Tree Reduction Architecture and 1.5-V Full-Swing BiCMOS Dynamic Logic Circuit

J. B. Kuo, K. W. Su, and J. H. Lou

***Abstract*—This brief presents a BiCMOS dynamic multiplier, which is free from race- and charge-sharing problems, using Wallace tree reduction architecture and 1.5-V full-swing BiCMOS dynamic logic circuit. Based on a 1-μm BiCMOS technology, a 1.5-V 8 $\times$ 8 multiplier designed, shows a 2.3$\times$ improvement in speed as compared to the CMOS static one.**

I. Introduction

HIGH-SPEED multipliers are usually realized by parallel architectures [1], where Wallace reduction structure [1], [2] and carry look-ahead circuit have been used to enhance the speed performance. In a high-speed parallel multiplier using Wallace tree reduction structure, the most important building cells are the full adder circuit and the carry look-ahead circuit. Although CMOS dynamic technique [2], [3] can provide a speed advantage over the static one for implementing serial adders, it is not suitable for realizing the full adder circuit for parallel multipliers using Wallace tree reduction structure due to race problems [3]. Currently, BiCMOS static logic circuits have been proved to be helpful for realizing high-speed VLSI systems [4]. In fact, BiCMOS dynamic logic circuits can also be very helpful for implementing high-speed digital systems. Recently, a BiCMOS dynamic carry look-ahead circuit, which is built by cascading BiCMOS dynamic logic gates without race problems, has been reported [5]–[8]. However, it is for 5-V operation. For advanced BiCMOS technologies, scaling power supplies are unavoidable [9], [10]. For a deep sub-half-micron BiCMOS technology, a 1.5-V supply is necessary. Recently, a 1.5-V BiCMOS static logic circuit [11] has been reported. In this brief, a 1.5-V BiCMOS dynamic multiplier using Wallace tree reduction techniques and 1.5-V full-swing BiCMOS dynamic logic circuit without race- and charge-sharing problems is described. In the following sections, the BiCMOS dynamic full adder circuit and carry look-ahead circuit based on the 1.5-V full-swing BiCMOS dynamic logic circuit techniques is described first, followed by the 8 $\times$ 8 multiplier circuit and discussion.

II. The 1.5-V BiCMOS Dynamic Full-Adder and CLA Circuit

Fig. 1(a) and (b) shows the 1.5-V BiCMOS dynamic full adder and CLA circuit. As shown in Fig. 1(a), the BiCMOS dynamic full adder circuit is composed of cascading two noninverting BiCMOS dynamic logic cells [12]–[14] for 1.5-V operation. The first BiCMOS dynamic logic cell is used to implement the $\overline{carry}$ signal (carry $= AB + BC + AC$), and the second cell is used to realize the sum signal (sum $= \overline{carry}(A+B+C)+ABC$). As in a dynamic BiCMOS digital circuit [12]–[14], during the precharge period, the clock signal (CK) is low, and the outputs of two cells are charged to high, and the bipolar devices are turned off by MN1 and MN2, which are controlled by CMOS NAND1 and NAND2. The function of the NAND's gate as shown in Fig. 1(a) and (b) is discharging the base of the BJT and disconnecting the p-logic-tree from the power supply after the output is pulled down.

In addition, MP1 and MP2 are off at this time. During the logic evaluation period, the CK is high. During the initial period of the logic evaluation period, MP1 and MP12 are on, and MN1 and MN2 are off. If at least any two of the three $(\overline{A_i}, \overline{B_i}, \overline{C_i})$ inputs are low, the $\overline{carry}$ signal is pulled low by the pull-down bipolar transistor. Then, the sum signal will be pulled down only when all of the three signals A_i, B_i, C_i are low or when the $\overline{carry}$ signal is low and at least one of the three signals A_i, B_i, C_i is low. Using the noninverting BiCMOS logic circuits, the full adder can be used in the high-speed parallel multiplier with Wallace reduction structure without race problems. Furthermore, in order to avoid charge-sharing problems [15], MP7, MP14, and MP19 have been used.

In a dynamic logic circuit, charge sharing [15] can be a serious problem. Consider the first logic circuit $(\overline{C_i})$ in the following situation: In a period, $\overline{A_i}$ and $\overline{B_i}$ are low, and $\overline{C_{i-1}}$ is high. During the precharge period, the voltage at node $X1$ is pulled high to 1.5 V, and the bipolar device is off since the base is pulled down to ground. In the logic evaluation period, $\overline{A_i}$ and $\overline{B_i}$ switch from low to high, and $\overline{C_{i-1}}$ turns low. During this period, the bipolar device is supposed to maintain the off condition. However, due to the parasitic capacitance at node $X1$, the base voltage may not be 0 V any more. This is called charge sharing, which is often a problem when the cascoding input path is long. Here, using MP7 to set the voltage at $X1$ to 0.7 V during each period, charge sharing has been avoided. In the full adder circuit, only the nodes with a large parasitic capacitance are equipped with the "charge-sharing prevention" transistors—MP7, MP14, and MP19. In nodes with a small parasitic capacitance, for example at node $X2$, it is not necessary.

Fig. 1(b) shows the BiCMOS dynamic carry look-ahead circuit. The function of the carry look-ahead circuit is

$$C_i = G_i + C_{i-1} \cdot P_i, \quad \text{for } i = 1 \sim n$$

where n is the bit number. G_i and P_i are the generate and propagate signals $(G_i = X_i \cdot Y_i, P_i = X_i \oplus Y_i)$ produced from two inputs (X_i, Y_i) to the half adder. In the carry look-ahead

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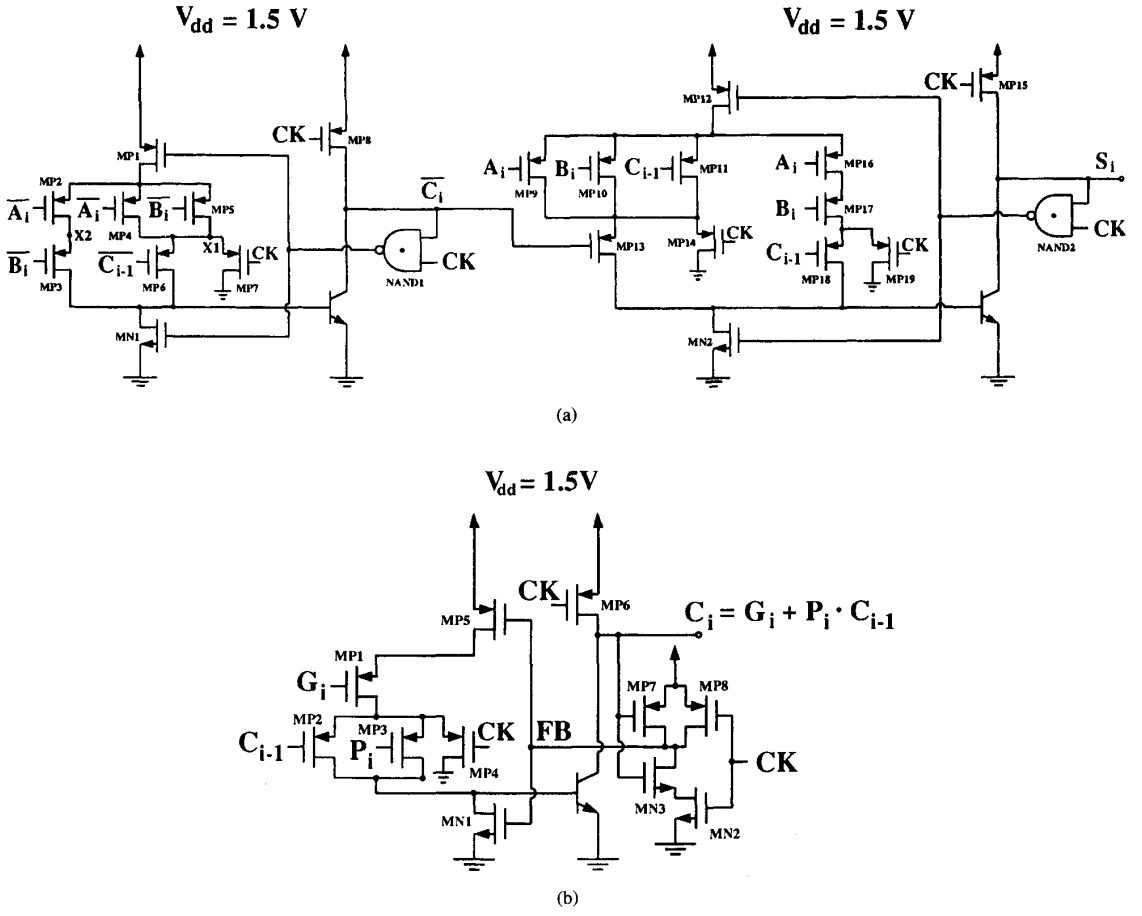

Fig. 1. (a) The 1.5-V full-swing BiCMOS dynamic full adder circuit. (b) The 1.5-V full-swing BiCMOS dynamic carry look-ahead circuit.

circuit, each bit *carry* signal (C_i) is high if the generate signal (G_i) is high or if the propagate signal (P_i) is high and the *carry* signal of the previous bit (C_{i-1}) is high.

Fig. 2(a) shows the propagation delay versus the power supply voltage of the full adder circuit and the carry look-ahead circuit using the BiCMOS dynamic and CMOS static techniques. The design is based on a 1 μm-BiCMOS technology, where it has a gate oxide thickness of 180 Å, a threshold voltage of ± 0.7 V, and a bipolar device with a unity gain frequency of 8 GHz. The aspect ratios of all NMOS and PMOS devices used are 36 μm/1 μm and 64 μm/1 μm, respectively. (Note that the aspect ratio of CMOS devices is not a dominant factor in determining the switching speed of the BiCMOS circuit. The most important factor in determining the speed performance of the BiCMOS circuit is the bipolar device.) In the study, an output load of 0.2 pf has been assumed. For a power supply voltage of 5 V, the speed advantage of the CLA and the full-adder using BiCMOS dynamic circuit is 5.3× and 2.8×, respectively. For a power supply voltage of 1.5 V, the speed advantage of the CLA and the full-adder using BiCMOS is 3.5× and 1.7×, respectively. Fig. 2(b) shows the propagation delay versus the load of the full adder circuit and the carry look-ahead circuit using the BiCMOS dynamic and CMOS static techniques. As shown in Fig. 1(b), the propagation delay of the BiCMOS dynamic circuits is less sensitive to the load due to the driving power of the BJT. Compared to the CMOS logic circuit, the BiCMOS dynamic logic circuit only has a slightly higher ac power dissipation. The consistent higher speed advantage of the BiCMOS dynamic full adder is very important for realizing parallel multipliers using Wallace tree reduction architecture.

As in a pipelined system, cascading dynamic logic gates may have serious race problems [8]. In the BiCMOS dynamic logic gate circuit with the BiPMOS pull-down structure, no race problems exist since the BiPMOS pull-down structure functions as a noninverting buffer.

III. The BiCMOS Dynamic Multiplier

High-speed parallel multipliers with Wallace tree reduction structure have been realized by CMOS static circuits [2], but they suffer from the speed penalty as a result of complex routing, long wiring, and irregular layout of the architecture [2]. Due to race problems, CMOS dynamic circuits are not suitable for building high-speed parallel multipliers with Wallace tree reduction structure. In fact, the BiCMOS

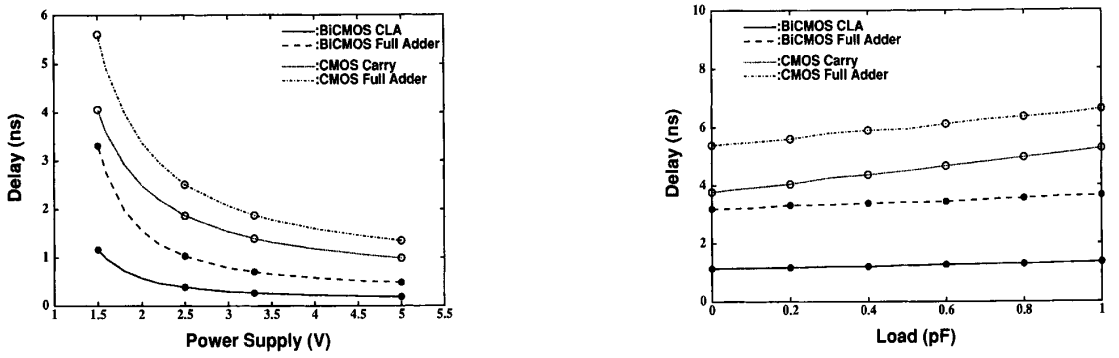

Fig. 2. Propagation delay of the full adder and the carry look-ahead using the 1.5-V full-swing BiCMOS dynamic logic circuit technique versus (a) the supply voltage. (b) load.

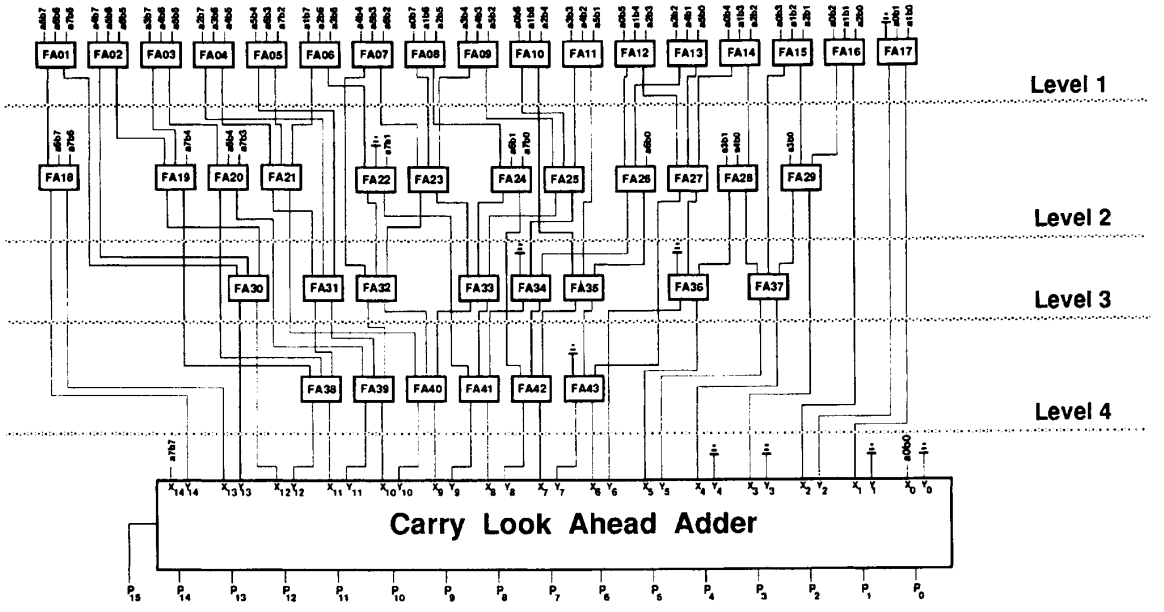

Fig. 3. Block diagram of the 8 × 8 parallel multiplier using Wallace tree reduction architecture with 1.5-V BiCMOS dynamic full adders and carry look-ahead circuit.

dynamic circuits are appropriate for implementing Wallace tree reduction architecture with complicated wiring. In order to show the versatilities of the BiCMOS dynamic full adder circuit for constructing parallel multipliers with Wallace tree reduction structure, an 8 × 8 parallel multipliers as shown in Fig. 3 has been designed.

Fig. 4 shows the transient waveforms at P_{15} and X_6 of the critical path via FA12, FA26, FA35, FA43, and the CLA as shown in Fig. 3. As shown in Fig. 4, a full swing of 1.5 V has been obtained. Note that as the CK signal turns high, the node voltage exceeds 1.5 V, which is due to the clock feedthrough over the C_{gd} of the precharge PMOS devices. In addition, the node voltage may go below 0 V, which is the result of the effect of the C_{bc} of the bipolar device. Fig. 5 shows the propagation delay of the critical path versus the supply voltage in the 8 × 8 parallel multiplier using Wallace tree reduction architecture, and the 1.5-V full-swing BiCMOS dynamic logic circuit. As shown in this figure, at a power supply voltage of 5 V, the speed advantage of the BiCMOS dynamic multiplier is 3.67×. At a supply of 1.5 V, the speed advantage is 2.26×.

IV. Discussion

The performance of the BiCMOS dynamic logic gate described above has also been compared to a CMOS dynamic logic gate [16], [17] as shown in Fig. 6. Fig. 7 shows the switching time versus the output load of the 1.5-V CMOS dynamic logic circuit and the 1.5-V BiCMOS dynamic logic circuit. For the CMOS circuit, the switching time is proportional to the load capacitance. On the other hand, the switching time of the BiCMOS circuit is relatively independent of its

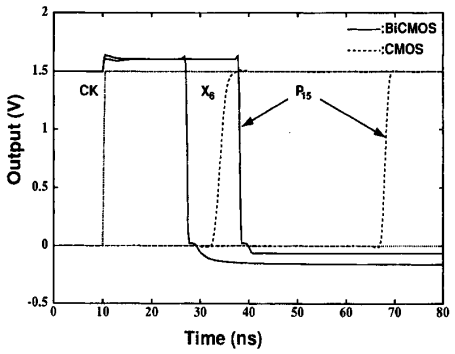

Fig. 4. Transient waveform at P_{15} and X_6 of the critical path via FA12, FA26, FA35, FA43, and the CLA.

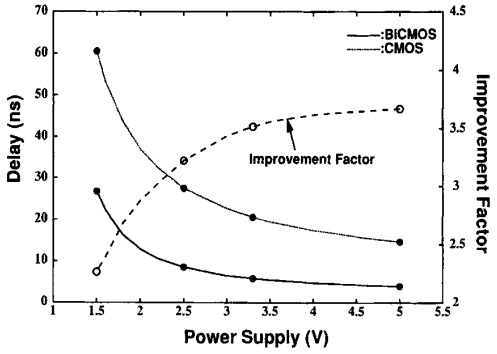

Fig. 5. Propagation delay of the critical path versus the supply voltage in the 8 × 8 parallel multiplier using Wallace tree reduction architecture and the 1.5-V full-swing BiCMOS dynamic logic circuit.

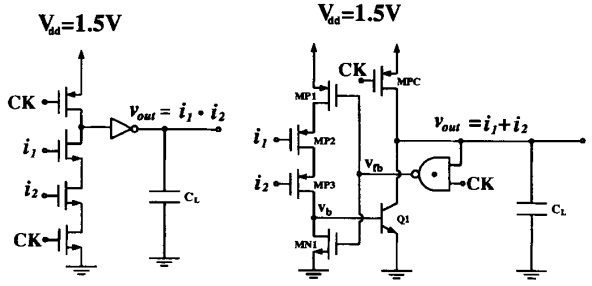

Fig. 6. (a) The 1.5-V CMOS dynamic logic circuit. (b) The 1.5-V BiCMOS dynamic logic circuit.

load. With an output load of 0.2 pf, the improvement is 3 ×. For a load of 1 pf, the improvement is around 4×. The improvement in the switching speed of the BiCMOS dynamic circuit over the CMOS circuit is attributed to the enhanced pull-down capability from the bipolar device.

For deep submicron CMOS technology using 1.5-V supply voltage, threshold voltages are difficult to design. Using the 1.5-V BiCMOS dynamic logic circuit, the problems associated with the threshold voltage can be reduced owing to the bipolar device. Fig. 8 shows the switching time versus the absolute

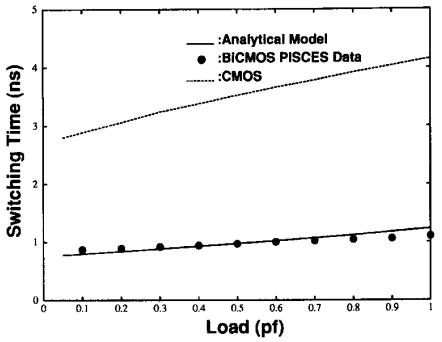

Fig. 7. Switching time of the 1.5-V CMOS dynamic logic circuit and 1.5-V BiCMOS dynamic logic circuit versus the load capacitance.

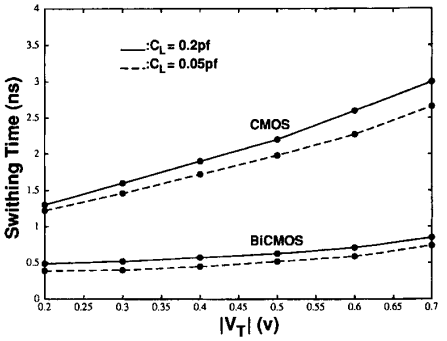

Fig. 8. The switching time versus the absolute value of the threshold voltage of the CMOS device of the 1.5-V dynamic logic circuit using CMOS and BiCMOS with an output load of 0.2 pf and 0.05 pf.

value of the threshold voltage of the CMOS device of the 1.5-V dynamic logic circuit using CMOS and BiCMOS with an output load of 0.2 and 0.05 pf. As shown in Fig. 8, the switching time of the CMOS circuit is proportional to the magnitude of its threshold voltage. A large magnitude in the threshold voltage leads to a long switching time as a result of the reduced current drive. On the other hand, the BiCMOS circuit is relatively insensitive to the magnitude of the threshold voltage regardless of the load capacitance.

V. Conclusion

This brief presents a BiCMOS dynamic multiplier, which is free from race- and charge-sharing problems, using Wallace tree reduction architecture and 1.5-V full-swing BiCMOS dynamic logic circuit. A 1.5-V 8 × 8 multiplier, which is designed based on a 1 μm BiCMOS technology, shows a 2.3× improvement in speed as compared to the CMOS static one.

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