Implementation of a 8-bit CMOS Wallace Tree Multiplier

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Abstract

A Wallace tree is a variant of long multiplication, a method used for the multiplication of two numbers. There are various similar CMOS multiplier architectures, such as a carry-save multiplier, array multiplier, Dadda multiplier, Wallace multiplier. Wallace tree has been widely used and is the most preferred algorithm for multiplication because of its fast speed and ease of fabrication[1].

In this paper, a 3-bit multiplier is implemented with the Wallace reduction method using esim software(open-source tool for circuit design, analysis and PCB design) and CMOS technology from the sky130 PDK process node.

1 Circuit Details

In CMOS technology both NMOS and PMOS transistors are used to realize the logic which is an advantage of CMOS over NMOS and bipolar technology, also has lesser power dissipation[1]. This helps in reducing the area covered by the circuit and allowing to occupy more gates per square area.

The structure is implemented using half adders, full adders, XOR and AND gates. In Wallace tree reduction, every bit is multiplied with every bit of the other number, then these partial products which have weight equal to the product of its factors are further reduced to obtain the respective weights by using half adders or full adders based on the size. The final result is calculated by the weighted sum of all these partial products.

Through esim software, schematic was designed and netlist of the schematic was exported to perform simulation using ngspice. During simulation, I have passed four patterns to both the inputs "a" and "b" each 3 bits wide, which results in a 6-bit value. The first pattern inputs are a2a1a0 = 101, b2b1b0 = 010 so the output here is z5z4z3z2z1z0 = 001010, the second pattern inputs are a2a1a0 = 000, b2b1b0 = 011 and output z5z4z3z2z1z0 = 000000, the third pattern inputs are a2a1a0 = 111, b2b1b0 = 110, output z5z4z3z2z1z0 = 101010, the fourth pattern inputs are a2a1a0 = 100, b2b1b0 = 001 so the output here is z5z4z3z2z1z0 = 00100

A 3 x 3 multiplier designed using CMOS technology based on sky130 design elements shows a significant improvement in performance.

2 Implemented Circuit

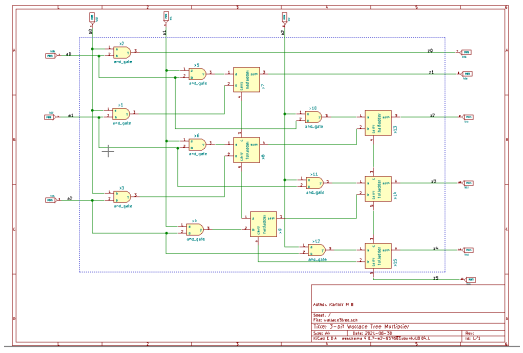

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

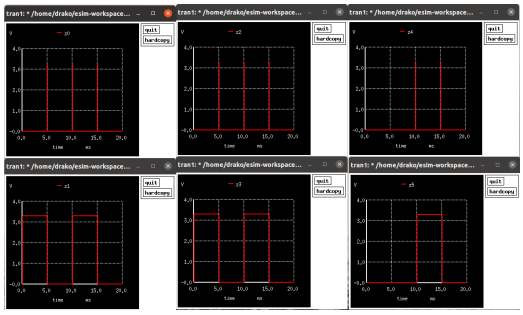

Figure 2: Implemented waveform.

References

[1] K. W. S. J. B. Kuo and J. H. Lou. A bicmos dynamic multiplier using wallace tree reduction architecture and 1.5-v full-swing bicmos dynamic logic circuit. https://ieeexplore.ieee.org/document/400440.

[2] H. B. Xiaoping Li, Xingguo Xiong and P. Patra. Implementation of a 8-bit cmos wallace-tree multiplier. https://core.ac.uk/display/52956427?utm_source=pdf&utm_medium=decoration-v1.