Specification Sheet for 8-bit Modified Wallace-Tree Multiplier

[dvsd_wt3206m]

An Application for a Wallace Tree Multiplier(dvsd_wt3206m)
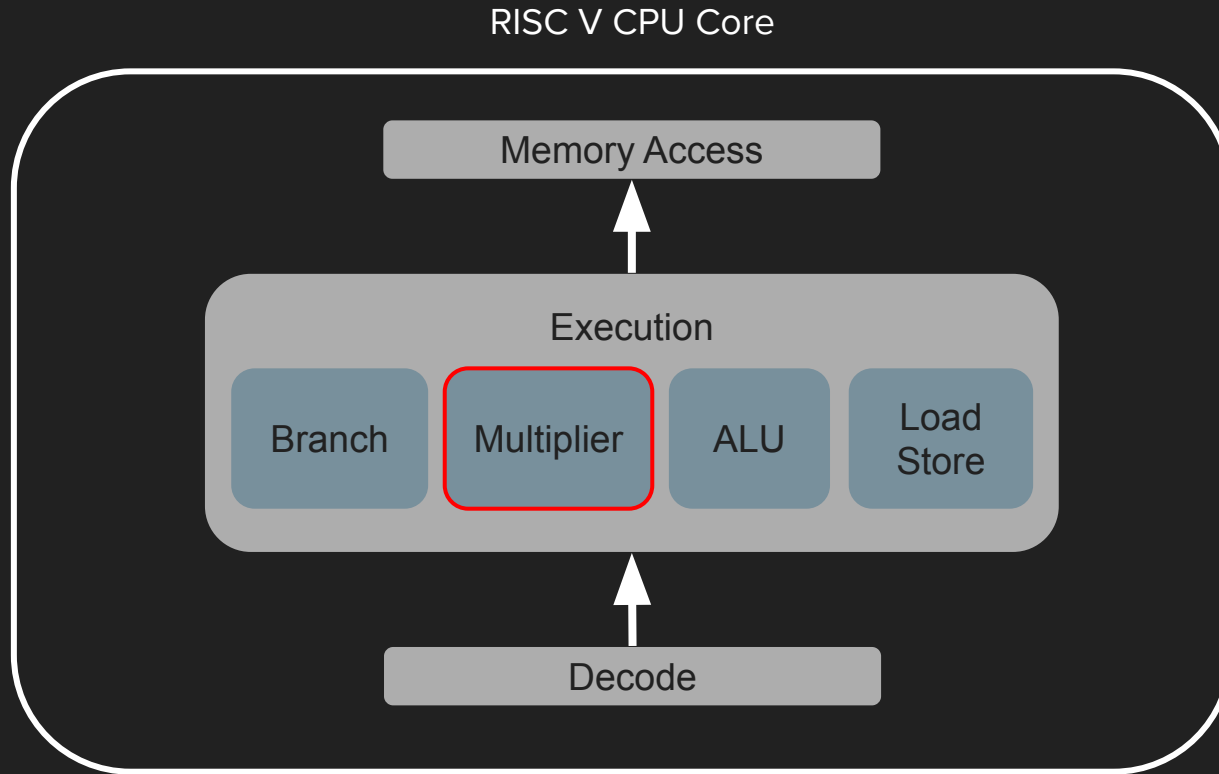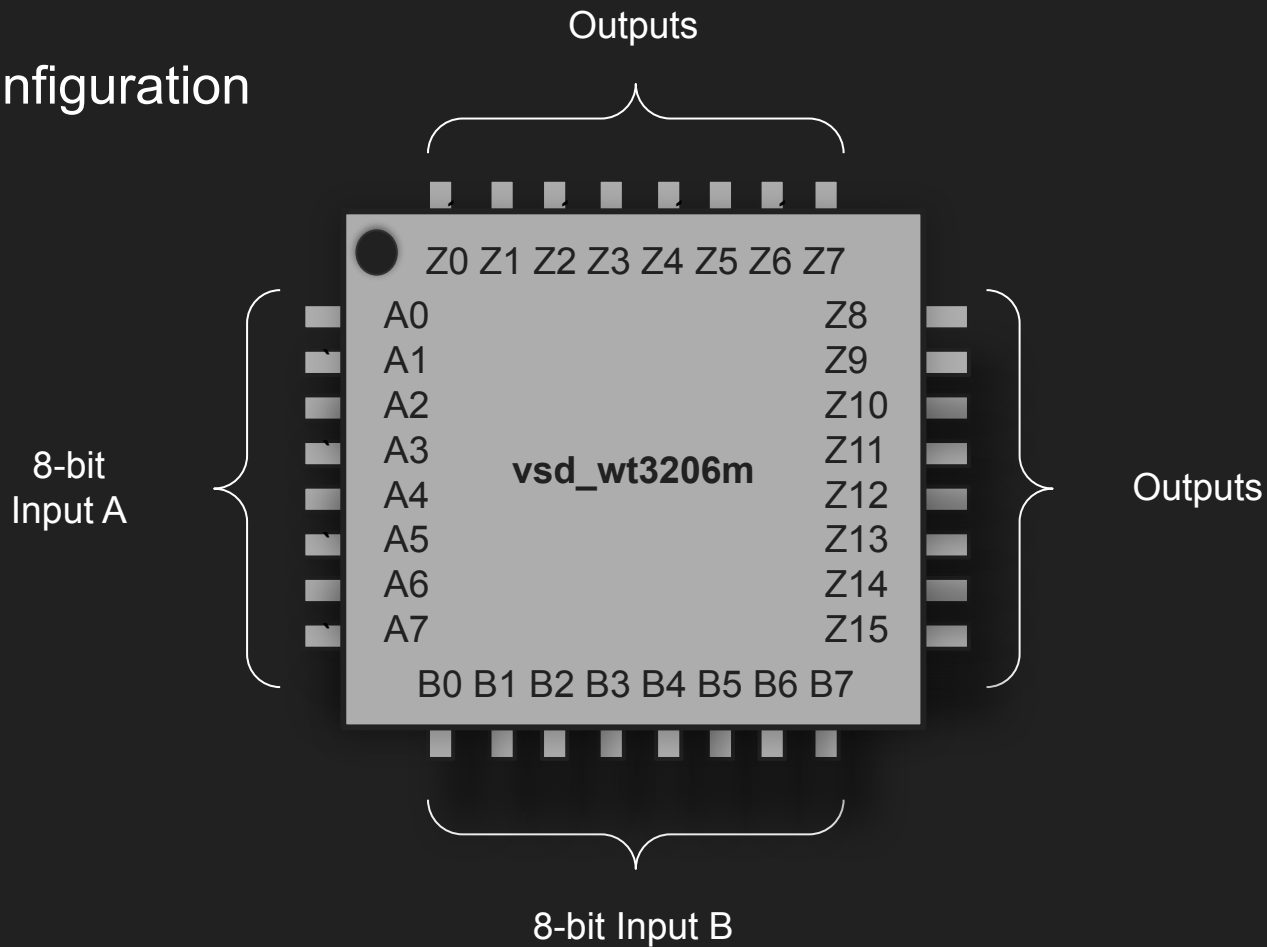

fig. Execution pipeline for RISC V12

Pin Configuration

Outputs

Z0 Z1 Z2 Z3 Z4 Z5 Z6 Z7

A0
A1
A2
A3
A4
A5
A6
A7

vsd_wt3206m

Z8
Z9
Z10
Z11
Z12
Z13
Z14
Z15

B0 B1 B2 B3 B4 B5 B6 B7

8-bit
Input A

Outputs

8-bit Input B

Components:

- CMOS AND Gate
- CMOS XOR-XNOR Gate
- CMOS 2-input Multiplexer
- Half Adder
- Full Adder
- 3:2 Compressor
- 4:2 Compressor
- 5:2 Compressor
- 16-bit adder(Kogge Stone adder)
- 8-bit Modified Wallace Tree Multiplier

SPECIFICATIONS

At Ta = +25C and VDD = 3VDC

Parameter	min	typ	max	units
Input				
a[7:0]	0	1.8	VDD	mV
b[7:0]	0	1.8	VDD	mV
Output				
z[15:0]	0	1.8	VDD	mV
vref	1.8		VDD	mV
gnd		0		mV
delay		7.168(expected)		ns
error		0.1		mV

Complexity(Normal Wallace Tree)

Full Adders   : 38
Half Adders   : 15
Total Gates   : 402