Performance Analysis of Wallace Tree Multiplier with Kogge Stone Adder using 15-4 Compressor

A.Sundhar, S.Deva tharshini, G.Priyanka, S.Ragul and C.Saranya

***Abstract*—The major role of electronics device is to provide low power dissipation and compact area with high speed performance. Among the major modules in digital building blocks system, multiplier is the most complex one and main source of power dissipation. Approximate Computing to multiplier design plays major role in electronic applications, like multimedia by providing fastest result even though it possesses low reliability. In this paper, a design approach of 16bit Wallace Tree approximate multiplier with 15-4 compressor is considered to provide more reliability. The 16×16 Wallace tree multiplier is synthesized and simulated using Xilinx ISE 14.5 software. The multiplier occupies about 15% of total coverage area. The dissipated power and delay of the multiplier are 0.042µw, 3.125ns respectively.**

***Index Terms*—Kogge stone adder, 15-4 compressor, Wallace tree multiplier, area, power delay and Xilinx ISE 14.5.**

I. Introduction

MULTIPLIERS are the essential part of the digital system like Arithmetic and Logic Units, Digital Signal Processors, etc. Usually, they prompt the performance like power, delay and area utilization of the system. Hence there is an increasing demand for the improvement of performance of the multiplier[1-4]. The multiplier consists of 3 stages - partial products generation, partial products reduction and addition at the last stage. The second stage (partial product) in multiplier utilize more time and power. Various techniques were suggested to diminish multipliers critical stages. The most popular technique is using the compressor in the reduction stage of partial product. The compressor is simply an adder circuit. It takes a number of equally-weighted bits, adds them, and produces some sum signals. Compressors are commonly used with the aim of reducing and accumulating a large number of inputs to a smaller number in a parallel manner. Their main application is within a multiplier, where partial products have to be summed up in a large amount concurrently. The inner structure of compressors avoids carry propagation. Either there are not any carry signals or they do arrive at the same time of the internal values[5-7].

For the purpose of reducing the delay in the second stage, several compressors are needed. Small sizes of compressors are useful for designing the small size multiplier. In multiplier design, the different sizes of compressors are required depending upon the bit size. In this paper, a scheme for delay reduction in 16bit Wallace tree multiplier with 15:4 compressor is considered. To build 15:4 compressor, a 5:3 compressor is considered as a basic module. AND gate is used for the generation of partial products. For 'N' bit multiplier 'N2' AND gates are needed. In the partial product reduction phase, there are three major components namely half adder, full adder and 5-3 compressor[8-11]. The final stage of addition is done by using Kogge-Stone adder. Fig. 1 shows the structure of 16X16 multiplier. Simulation results show that the approximate multiplier with compressor using Kogge stone adder achieves high performance while comparing to the multipliers with compressor using other adder like parallel adder. This paper is elaborated in following sections. Designs of approximate 16×16 Wallace tree multiplier are detailed in section II. Brief notes and design of 15-4 compressor, 5-3 compressor and Kogge stone adder is described in section III. The section IV depicts the Result analysis. Section V concluded the overall paper.

II. Wallace Tree Multiplier

Multiplier is the substantive part of the electronic device and decides the overall performance of the system [1]. When designing a multiplier, huge amount of power and delay are generated. To minimize these disadvantages, adders and compressor are used. Hence reducing delay in multiplier has been a main aim to enhance the performance of the digital systems like DSP processors [8]. Hence many attempts are done on multipliers to make it faster. It is an effective hardware realization of digital system that is nothing but a Wallace tree which multiplies two numbers and minimizes the number of partial products [4]. In vector processors, several multiplications are performed to obtain data or loop level parallelism. High processing speed and low power consumption are the major advantages of this multiplier [2].

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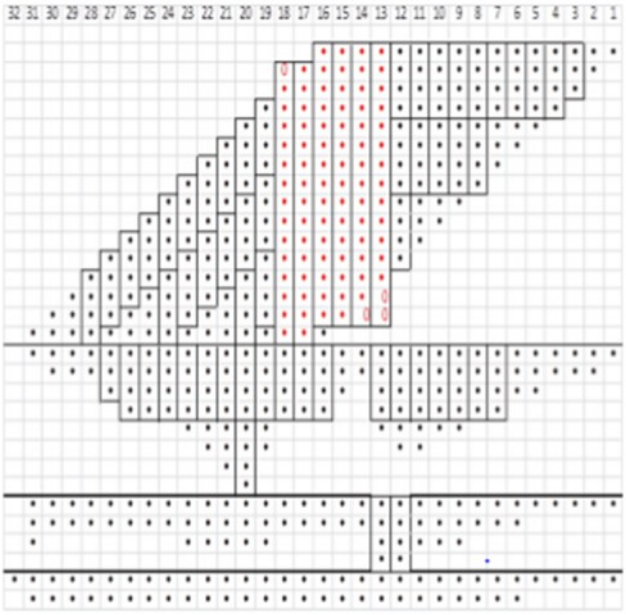

Fig. 1. Structure of 16×16 Multiplier using 15-4 compressor

The three stages of Wallace tree multiplier are mentioned below:

1) Partial products generation
2) Partial products reduction
3) Addition at the final stage

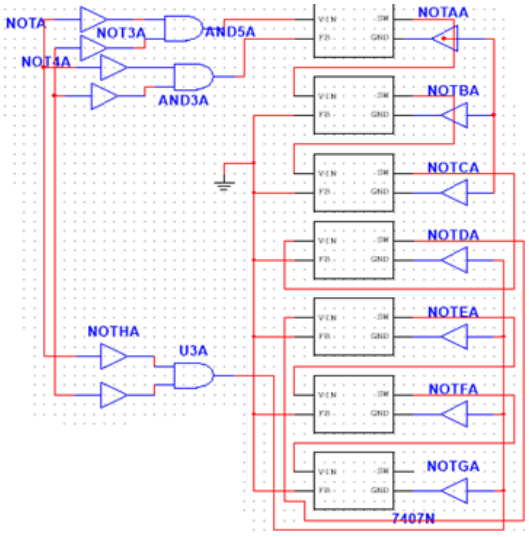

Fig. 2. Schematic View of 16×16 Bit Wallace Tree Multiplier

Fig. 1 and Fig. 2 describes the structure and schematic view of 16bit multiplier using with the help of 15-4 compressor. Here in this design each dot denotes partial product. From 13th column onwards, 15-4 compressors are used in this multiplier architecture. Column number 13 consist of 13 partial products, in order to get 15 partial products 2 zeros are added. Similarly, in 14th column, one zero is added. Approximate compressors are used in 13th, 14th and15th column of multipliers. The partial product reduction phase consists of half adder, full adder and 5:3 compressors. When the numbers of bits in the column are 2 and 3 half adders and full adders are used in each column. In case of a single bit, it is moved further to the subsequent level of that particular column without any need for further processing. Until only two rows will remain, this reduction process is repeated. Finally, summation of the last two rows is achieved using 4-bit Kogge-Stone adder.

III. 15-4 COMPRESSOR

A compressor is simply an adder circuit. It takes a number of equally-weighted bits, adds them, and produces some sum signals. Compressors are commonly used with the aim of reducing and accumulating a large number of inputs to a smaller number in a parallel manner. They are the important parts of the multiplier design as they highly influence the speed of the multiplier. Their main application is within a multiplier, where a huge number of partial products have to be summed up concurrently. For high speed applications like DSP, image processing needs several compressors to perform arithmetic operation. A compressor adder provides reduced delay over conventional adders using both half adders and full adders. Here the representation as 'N-r', in which 'N' denotes as the number of bits and 'r' denotes as the total number of 1's present in 'N' inputs. The compressor reduces the number of gates and the delay with reference to other adder circuits. The inner structure of compressors avoids carry propagation. Either there are not any carry signals or they do arrive at the same time of the internal values. Compressors are widely used in the reduction stage of a multiplier to accumulate partial products in a concurrent manner. In this part it is considered the design of 15-4 compressor by using with approximate 5-3 compressors [5]. This compressor compresses 15 inputs (C0-C14) into 4 outputs (B0-B3). The 15-4 compressor consists of three phases. The first phase has five full adders, the second phase uses two 5-3 compressors and finally the 4-bit kogge stone adder. In this compressor design, approximate 5-3 compressor are preferred over accurate 5-3 compressors as shown in the Fig. 3

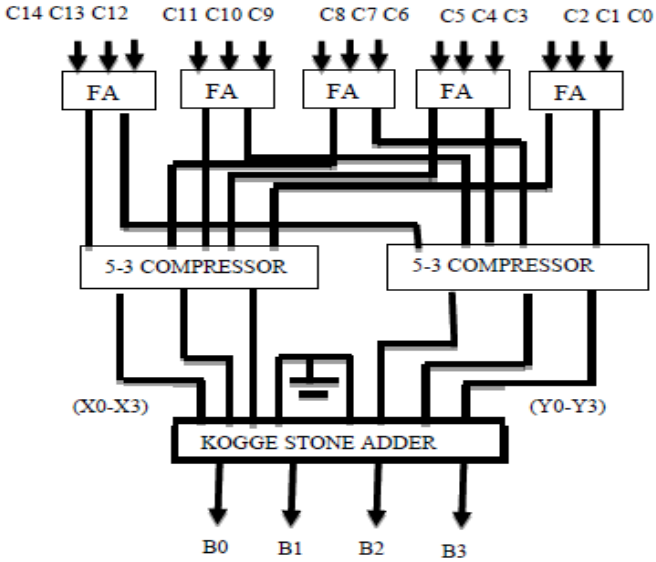

Fig. 3. Logic Diagram of Approximate 15-4 Compressor [6]

A. 5-3 Compressor

The 15-4 compressor consists of 5-3 compressor as a basic design. The 5-3 compressor utilizes five primary inputs namely A0, A1, A2, A3, A4 and produces three outputs namely B0, B1, B2. In this compressor, the presence of number of 1's at the input decides the output of compressor and also uses counter property.

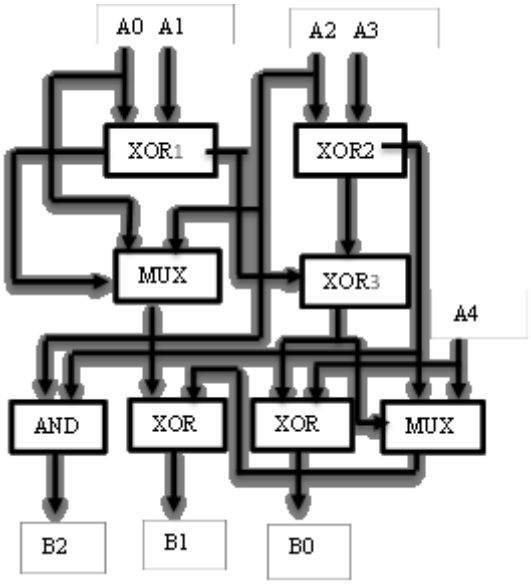

Fig. 4. Logic diagram of 5-3 compressor

$$B_2' = [A_3.A_2] \quad (1)$$

$$B_2=A_0.[\sim(A_0 \oplus A_1)]+A_2.(A_0 \oplus A_1)[A_3. (\sim(A_0 \oplus A_1 \oplus A_2 \oplus A_3))] + A_4.[A_0 \oplus A_1 \oplus A_2 \oplus A_3] \quad (2)$$

$$B_1=A_0.[\sim(A_0 \oplus A_1)]+A_2.(A_0 \oplus A_1) \oplus [A_3. (\sim(A_0 \oplus A_1 \oplus A_2 \oplus A_3))] + A_4.[A_0 \oplus A_1 \oplus A_2 \oplus A_3] \quad (3)$$

$$B_0=[A_0 \oplus A_1 \oplus A_2 \oplus A_3 \oplus A_4] \quad (4)$$

The design of compression of given 5 inputs into 3 output is called the design of 5-3 compressor. Error rate of 5-3 compressor is considered. The design equations of 5-3 approximate compressor are shown in following equations respectively. The logic diagram of approximate 5-3 compressor is as shown in Fig. 4.

B. Kogge Stone Adder

In 1973, Peter M. Kogge and Harold S. Stone introduced the concept of efficient and high-performance adder called kogge-stone adder. It is basically a parallel prefix adder. This type of adder has the specialty of fastest addition based on design time. It is known for its special and fastest addition based on design time [9], [10]. In Fig. 5 and Fig. 6, the functional block diagram and RTL view of a 4-bit Kogge-Stone Adder is shown. By using the ith bit of given input, the propagate signals 'Pi' and generate signals 'Gi' are calculated. Similarly, these generated signals produce output carry signals. Therefore by minimizing the computation delay, Prefix Adders are mainly classified into 3 categories.

A. Pre- processing

B. Generation of Carry

C. Final processing.

A. Pre-Processing

In this stage, the generate and propagate signals are given by the equations 5&6.

$$P_i=A_i \oplus B_i \quad (5)$$

$$G_i=A_i \,.\, B_i \quad (6)$$

B. Generation of carry

In this stage, carries are calculated with their corresponding bits and this operation is executed in parallel manner. Carry propagation and generation are used as intermediate signals. The logic equations for carry propagate and generate are shown below.

$$G_i= (P_i \,.\, G_{iprev}) +G_i \quad (7)$$

$$P_i= (P_i \,.\, P_{iprev}) \quad (8)$$

C. Final Processing

In final processing, the sum and carry outputs bits are computed for the given input bits and the logic equation for the final processing stage is given by

$$C_i=G_i \quad (9)$$

$$S_i=Pi \oplus C_{i-1} \quad (10)$$

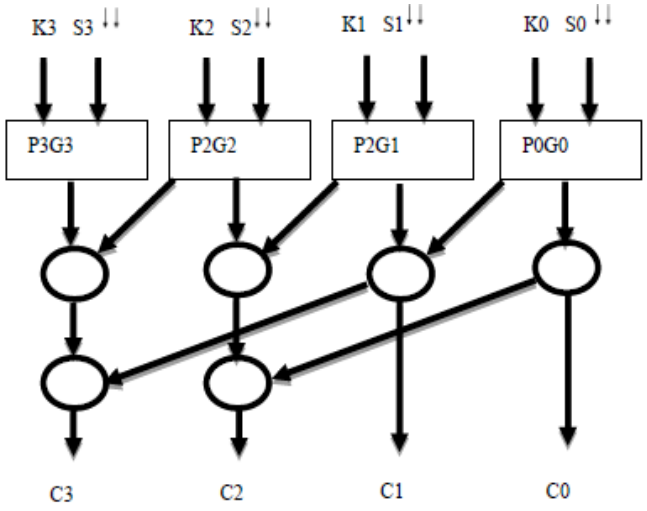

Fig. 5. Block diagram of kogge stone adder

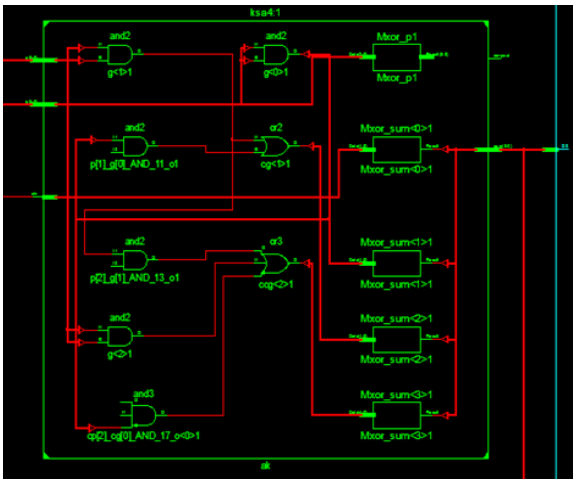

Fig. 6. RTL view of kogge-stone adder

IV. Simulation Result

The design of approximate16 bit Wallace multiplier using 15-4 compressor has been done in HDL, using Xilinx ISE 14.5. Simulation results show the design of overall architecture of Wallace tree multiplier as shown in Fig. 7. The parameters of area are utilized by the multiplier design and power consumption are obtained through simulation and tabulated in Table I and Table II. The snapshot of delay obtained through simulation is shown in Fig. 8. The processing delay at the end of addition level can be reduced by using kogge stone adder.

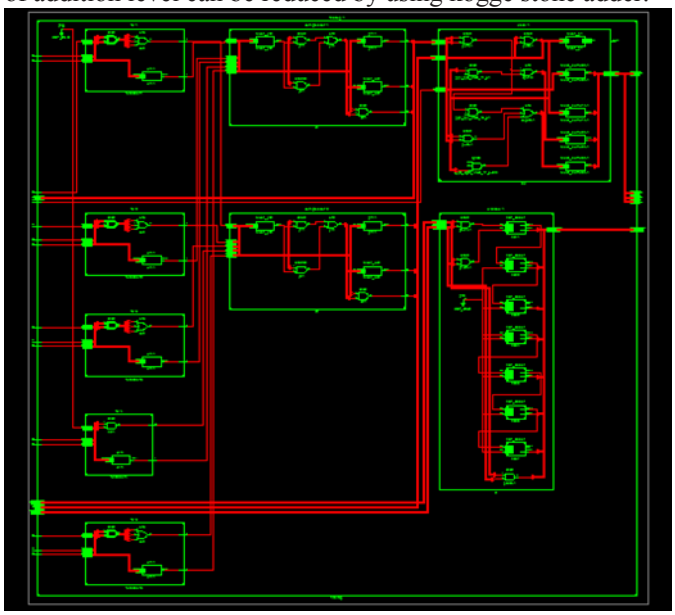

Fig. 7. Overall Architecture Of 16×16 Bit Wallace Tree Multiplier

Table I and II describes the area utilization and power parameters of a 16-bit Wallace multiplier. It shows better result than other adder apart from that it gives less area and low propagation delay.

TABLE I
DEVICE UTILIZATION OF 16×16 WALLACE TREE MULTIPLIER

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	20	63400	0%
Number of fully used LUT-FF pairs	0	20	0%
Number of bonded IOBs	33	210	15%

TABLE II
POWER ANALYSIS OF 16×16 WALLACE TREE MULTIPLIER

On-Chip	Power (W)
Logic	0.000
Signals	0.000
IOs	0.000
Leakage	0.042
Total	0.042

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Timing Summary:
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Speed Grade: -2

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 3.125ns
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Fig. 8. Delay analysis of 16×16bit Wallace tree multiplier

TABLE III
DESIGN ANALYSIS OF MULTIPLIER

SI.NO	Types of Multiplier	Area (μm^2)	Power (µw)	Delay (ns)
1	**16×16bit multiplier using Accurate 15-4 compressor**	5066.2	563.20	4.24
2	**16×16bit multiplier using 15-4 compressor with 4-bit parallel adder**	5159.3	557.2	4.24
3	**16×16bit multiplier using 15-4 compressor with kogge stone adder**	1570	420	3.125

The performance of 15-4 compressor based approximate 16×16 multiplier is also compared with various adders at the final stage instead of Kogge stone adder. The comparative results in terms of reduced delay, area and power dissipation are tabulated in Table III.

V. Conclusion

The approximate 16×16bit Wallace tree multiplier using 15-4 compressor architecture has been designed and synthesized using on Spartan 3 XC3S100E board and simulated in Xilinx ISE 14.5. The performance of proposed Multiplier with kogge stone adder is compared with the same architecture of multiplier using parallel adder. It can be inferred that 16×16 multiplier architecture using 15-4 compressor with kogge stone adder is faster compared to multiplier with parallel adder. In future the performance of the proposed multiplier can be improved and applied in applications like video and image processing.

References

[1] C. S. Wallace, A Suggestion for a Fast Multiplier, IEEE Transactions on Computers, 13, 1964,14-17.

[2] K. Bhardwaj, P. S. Mane, and J. Henkel, ‘‘Power-and area-efficient approximate Wallace tree multiplier for error-resilient systems,’’in Proc.15thInt. Symp. Quality Electron. Design (ISQED), Mar. 2014, pp. 263–269.

[3] C.-H. Lin and I.-C. Lin, ‘‘High accuracy approximate multiplier with error correction,’’ in Proc. IEEE 31st Int. Conf. Comput. Design (ICCD), Oct. 2013, pp. 33–38

[4] D. R. Gandhi, and N. N. Shah, Comparative Analysis for Hardware Circuit Architecture of Wallace Tree Multiplier, IEEE International Conference on Intelligent Systems and Signal Processing, Gujarat, 2013, 1-6.

[5] R. Menon and D. Radhakrishnan, ‘‘High performance 5:2 compressor architectures,’’ Proc. IEE-Circuits, Devices Syst., vol. 153, no. 5, pp. 447–452, Oct. 2006

[6] R. Marimuthu, M. Pradeepkumar, D. Bansal, S. Balamurugan, and P. S. Mallick, ‘‘Design of high speed and low power 15-4 compressor,’’ in Proc. Int. Conf. Commun. Signal Process. (ICCSP), Apr. 2013, pp. 533–536.

[7] Momeni, J. Han, P. Montuschi, and F. Lombardi, “Design and analysis of approximate compressors for multiplication,” IEEE Trans. Comput., vol. 64, no. 4, pp. 984–994, Apr. 2015.

[8] Teffi Francis, Tera Joseph and Jobin K Antony., “Modified MAC Unit for low power high speed DSP application using multiplier with bypassing technique and optimized adders”, IEEE-31661, 4th ICCCNT, 2013.

[9] Yezerla, Sudheer Kumar, and B. Rajendra Naik. "Design and Estimation of delay, power and area for Parallel prefix adders." In Engineering and Computational Sciences (RAECS), 2014 Recent Advances in, pp. 1-6. IEEE, 2014.

[10] Y. Choi, “Parallel Prefix Adder Design” Proc. 17th IEEE Symposium on Computer Arithmetic, pp 90-98, 27th June 2005.

[11] Belle W. Y. Wei and Clark D. Thompson, “Area-Time Optimal Adder Design”, IEEE transactions on Computers, vol.39, pp. 666-675, May1990.