Circuit Design and Simulation Marathon using eSim

Certificate of Completion

672db

This is to certify that

Mr./Ms. Karthik M B

from ***Maven Silicon VLSI Training Center***

has submitted the circuit:

Implementation of a 8-bit CMOS Wallace Tree Multiplier

in the Circuit Design and Simulation Marathon using eSim.

He/ She has performed an ***Outstanding****/~~Excellent/Very Good/Good~~ work.*

The Marathon was conducted in the month of June 2021
for a duration of 2 weeks. This was an initiative of the FOSSEE
(Free/Libre and Open Source Software in Education) Project, IIT Bombay
in association with VLSI System Design Corp.Pvt.Ltd.

Prof. Kannan Moudgalya
Principal Investigator - FOSSEE
IIT Bombay

Kunal P Ghosh
Co-Founder, VLSI System Design
Corp. Pvt. Ltd

Indian Institute of Technology Bombay

eSim
An open source EDA tool

fossee better education

VLSI System Design

NMEICT
National Mission on Education Through ICT

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