Group # 38

Intesarul Khan # 260579991

Tamim Sujat # 260551583

ECSE 323: Lab Report 3: Group 38 VGA

Circuit name: VGA

Input: Clock (1 bit), rst (1bit)

Output: Blanking (1 bit), HSYNC (1 bit), VSYNC (1 bit), ROW (10 bits), COLUMN (10 bits)

Description:

The final purpose of the VGA circuit is to enable an Altera DE1 board have a 12bit VGA video output that can be used to drive the monitor. Initially the circuit was used to generate the HSYNC, VSYNC and BLANKING signals alongside ROW and COLUMN counters to indicate a pixel location in a scan. (Refer to figure 1.1)

The vertical and horizontal counters are implemented in the VGA circuit using the LPM counter module from the Alter lpm library. We assigned the lpm_width at 11bit for horizontal and 10 bits for vertical and assigned the binary values of 1039 and 665 respectively inside the counters. The horizontal counter is clocked at the rising edge at 50 MHz & the vertical counter is enabled when the horizontal counter reaches maximum value.

Using the values obtained from the vertical counter the ROW value is calculated. ROW count is vertical minus 43 when the value is within the range of the visible area. Otherwise, the ROW value is set at 599 (for vertical counts higher than 642 or lower than 43).

Using the values obtained from the horizontal counter the COLUMN value is calculated. COLUMN count is horizontal minus 176 when the value is within the range of the visible area. Otherwise, the COLUMN value is set at 799 (for horizontal counts higher than 975 or lower than 176).

Finally, a horizontal sync occurs when the horizontal count value exceeds 120 and a vertical sync occurs when the vertical count value exceeds 6. Blanking occurs whenever the values of horizontal or vertical are set to 799 and 599 respectively (i.e. out of range for the monitor).

Pinout Diagram:

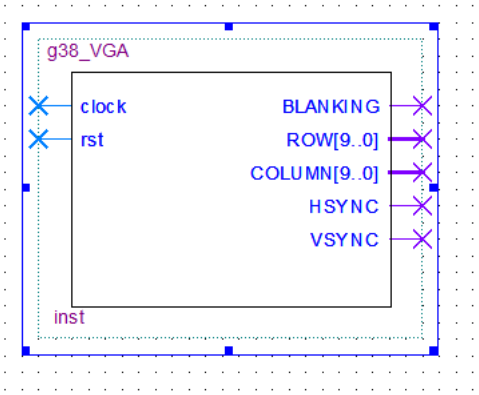


Figure 1.1: Pinout diagram for VGA circuit

Group # 38

Intesarul Khan # 260579991

Tamim Sujat # 260551583

Testing:

Initially, the circuit was checked using the RTL viewer to ensure the logic is correct (Figure 1.2). The circuit was then tested using a functional simulation using the Altera Model Sim software. The circuit performed as desired and as we can see from figure 1.3 that the ROW and COLUMN were calculated according to the range described before. The HSYNC and VSYNC performed according as well. The clock was run at 50 MHz. The simulation was run for 12 ms to provide enough data for a conclusive output.

To find out whether the circuit performs accordingly in real hardware a Signal Tap II testing was performed. Using an edge triggered Vertical Sync and a 2K sample depth for the clock the circuit provided the output as desired. The results are portrayed in figure 1.4.

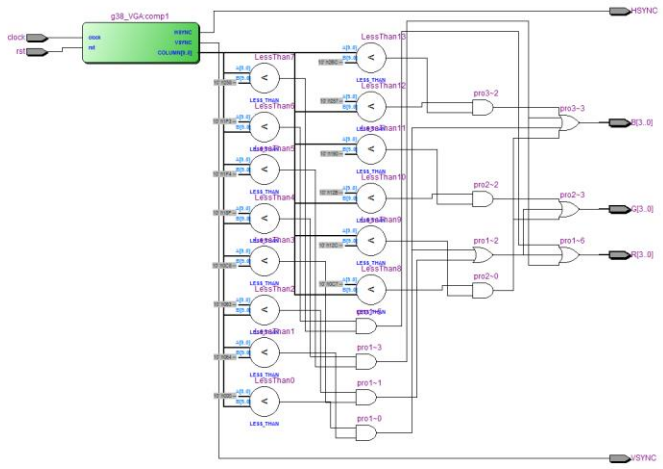


Figure 1.2: RTL view of entire process for VGA Signal Generator

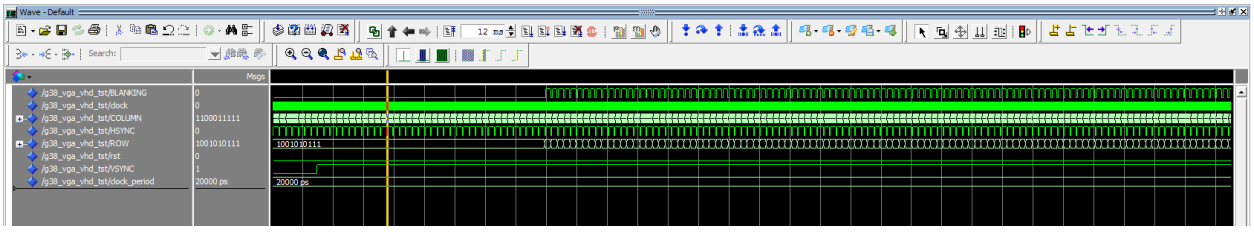


Figure 1.3: Functional simulation of VGA Signal Generator

Group # 38

Intesarul Khan # 260579991

Tamim Sujat # 260551583

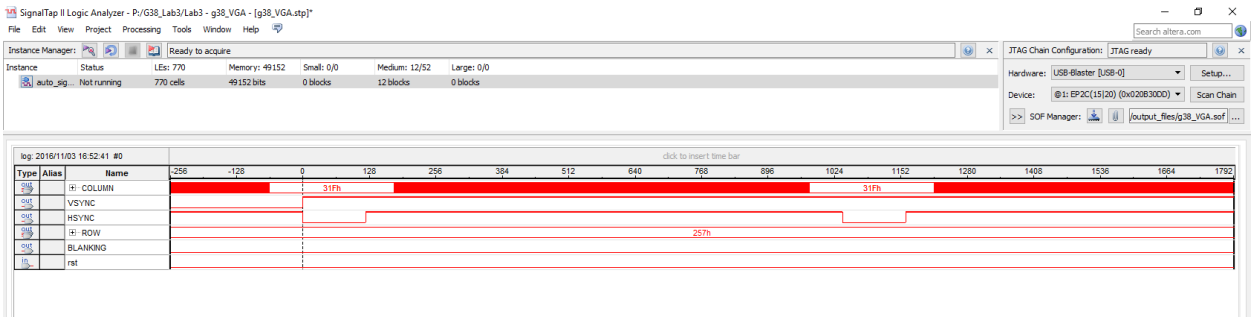


Figure 1.4: On-Chip Signal Tap II logic analysis of VGA Signal Generator

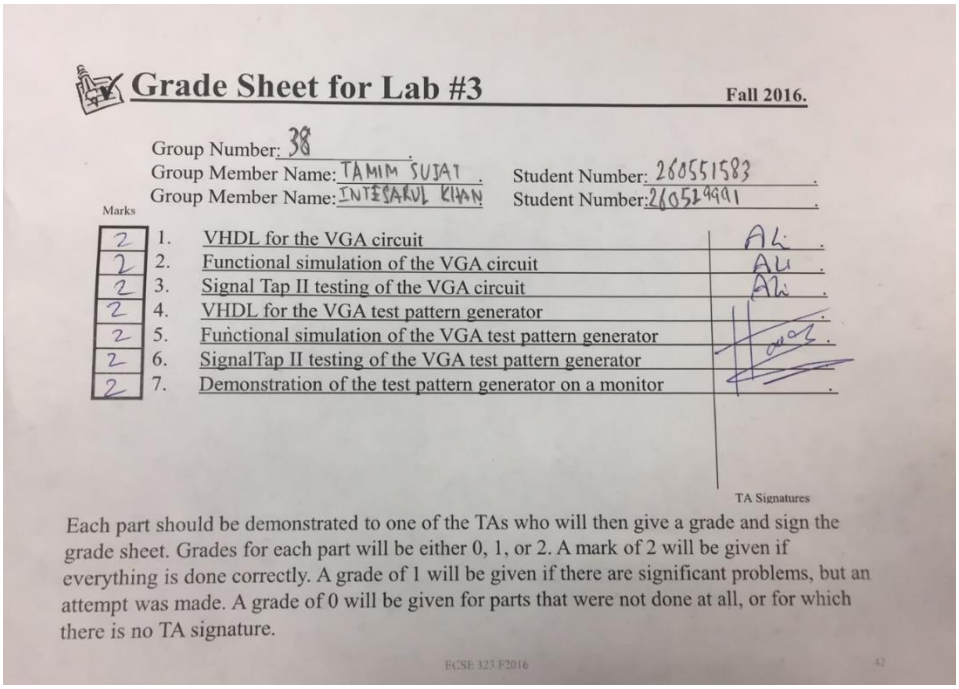
Summary of FPGA resource utilization

Flow Summary	
Flow Status	Successful - Fri Nov 04 11:03:44 2016
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Full Version
Revision Name	g38_VGA
Top-level Entity Name	g38_VGA_Test_Pattern
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Total logic elements	770 / 18,752 (4 %)
Total combinational functions	507 / 18,752 (3 %)
Dedicated logic registers	562 / 18,752 (3 %)
Total registers	562
Total pins	16 / 315 (5 %)
Total virtual pins	0
Total memory bits	28,672 / 239,616 (12 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Group # 38

Intesarul Khan # 260579991

Tamim Sujat # 260551583



Grade Sheet for Lab #3

Fall 2016.

Group Number: 38

Group Member Name: TAMIM SUJAT Student Number: 260551583

Group Member Name: INTESARUL KHAN Student Number: 260579991

Marks			TA Signatures
2	1.	VHDL for the VGA circuit	AK
2	2.	Functional simulation of the VGA circuit	AK
2	3.	Signal Tap II testing of the VGA circuit	AK
2	4.	VHDL for the VGA test pattern generator	
2	5.	Functional simulation of the VGA test pattern generator	
2	6.	SignalTap II testing of the VGA test pattern generator	
2	7.	Demonstration of the test pattern generator on a monitor	

Each part should be demonstrated to one of the TAs who will then give a grade and sign the grade sheet. Grades for each part will be either 0, 1, or 2. A mark of 2 will be given if everything is done correctly. A grade of 1 will be given if there are significant problems, but an attempt was made. A grade of 0 will be given for parts that were not done at all, or for which there is no TA signature.

ECSE 323 F2016 42