Group # 38

Intesarul Khan # 260579991

Tamim Sujat # 260551583

ECSE 323: Lab Report 2 – Keyboard Encoder

Circuit name: Keyboard Encoder

Input: Keys (64 bits)

Output: ASCII code (7 bits)

Description:
The purpose of this circuit is to take a 64-bit input signal and generate a 7-bit ASCII code output signal. This is implemented in VHDL using a conditional assignment statement using the 64-6-bit encoder as a component. Since the output generated by the 64-6 encoder is 6 bit, in order to convert it into a 7-bit output, the MSB {M1(5) from our VHDL code} is checked. When M1(5) = '1', the value of output ASCII CODE is represented by the function "10" and M1(4 downto 0). Similarly, when M1(5) = '0', the value of output ASCII CODE is represented by the function "01" and M1(4 downto 0). In the ASCII table the index along the top row is the 3 MSB of the codes while the index along the left column is the 4 LSB of the code. We are assuming in this question that our 64 keys on our keyboard include the symbol represented by the 2,3,4 and 5 columns of the ASCII table. Hence the input values from 2^0 to 2^63 results in the output of the ASCII Table from position, 20 to 5F, where 2 & 5 represents the column and 0 & F represents the rows of the table (See Fig 1.1).

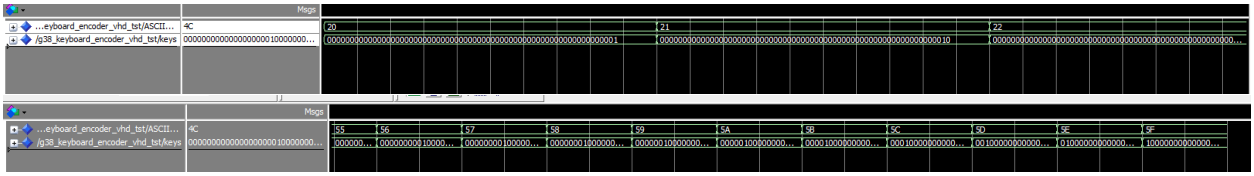


Figure 1.1: Simulation plot for keyboard encoder circuit

Pinout Diagram:

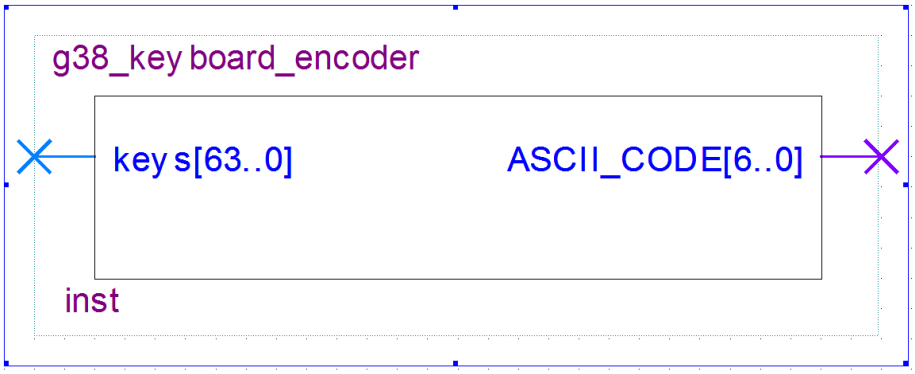


Figure 1.2: Pinout diagram for keyboard encoder circuit

Group # 38

Intesarul Khan # 260579991

Tamim Sujat # 260551583

Testing:

Initially the keyboard encoder circuit was tested using a functional simulation. Using a loop statement all the 64 input values were incremented thus allowing all the outputs of the ACSII table to be represented (see 'description section above & figure 1.1). Each iteration was compared to the expected result and yielded successful values.

To test the circuit on the DE1 board we designed a '7-segment decoder' circuit. Alongside we designed another circuit called 'ALTERA_segment_decoder' which combined the output from the keyboard encoder with the 7 segment decoder to yield the results on the Altera board. The RTL diagram below (figure 1.3) portrays the total process in a simplistic manner.

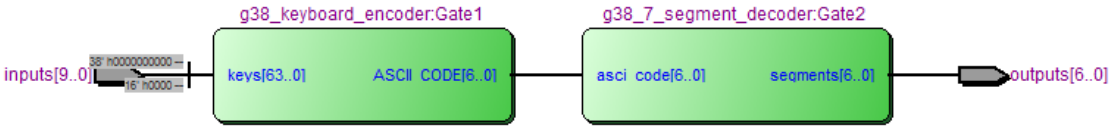


Figure 1.3: RTL view of entire process('ALTERA_segment_decoder') *for Altera testing*

The '7-segment decoder' functions by converting the 7-bit ACSII output from the keyboard encoder into a 7-bit format that is represented by the Altera LED as specified on the assignment description. All the values from 0-9 and A-Z were covered by the '7-segment decoder' we designed. Using functional simulations this was verified (See figure 1.4 below).

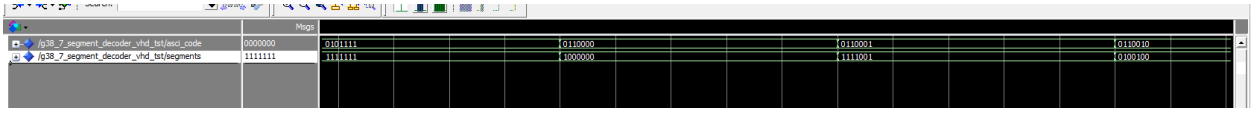


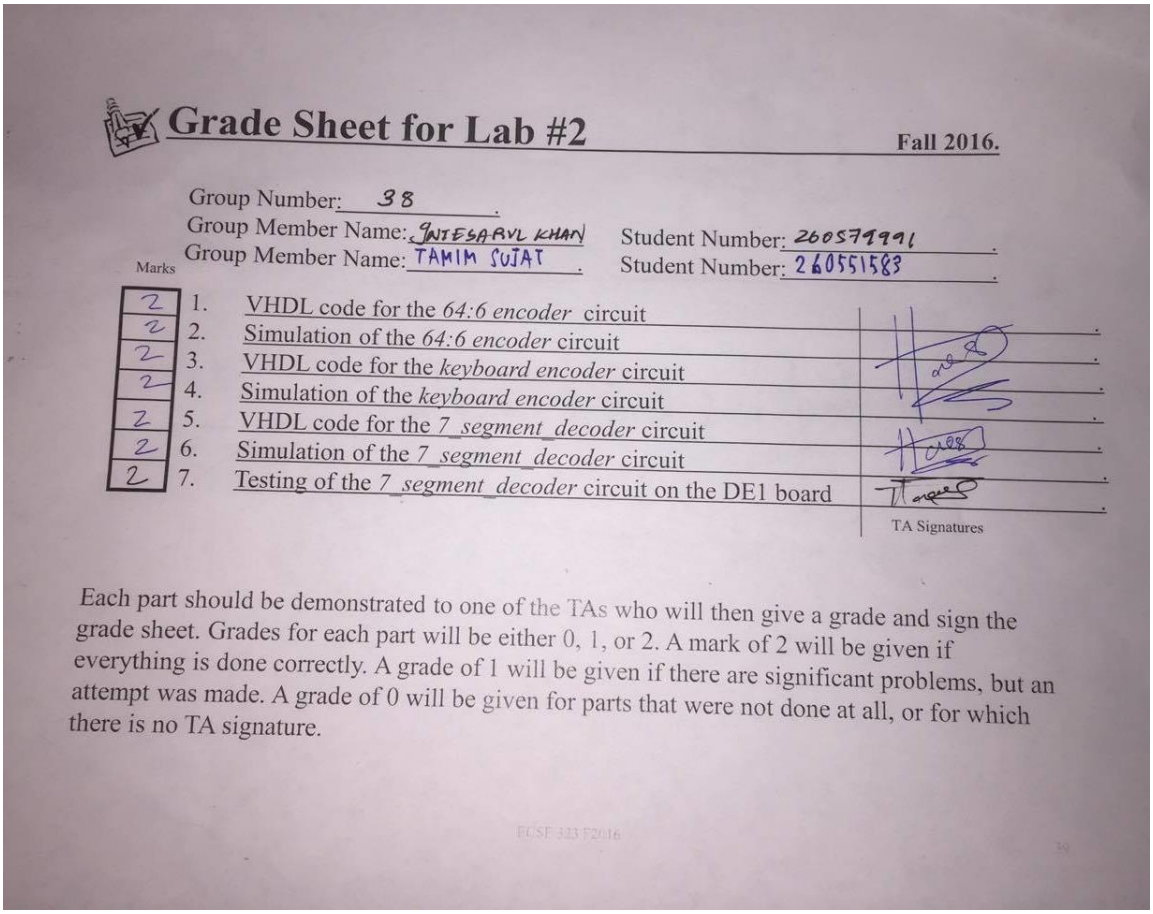
Figure 1.4: Functional simulation of '7-segment decoder'

The 'ALTERA_segment_decoder' uses the '7-segment decoder' and 'keyboard encoder' as components and combines with 54 extra zeros as input values to yield a satisfactory result on the LED. We have as well tested the condition in which if more than one key was pressed, the output was the smallest index as expected. For example, if both '9' and '3' switches on the Altera were turned on, the LED displayed the corresponding output for '3'.

Group # 38

Intesarul Khan # 260579991

Tamim Sujat # 260551583



Grade Sheet for Lab #2

Fall 2016.

Group Number: 38

Group Member Name: INTESARUL KHAN Student Number: 260579991

Group Member Name: TAMIM SUJAT Student Number: 260551583

Marks			TA Signatures
2	1.	VHDL code for the *64:6 encoder* circuit	
2	2.	Simulation of the *64:6 encoder* circuit	
2	3.	VHDL code for the *keyboard encoder* circuit	
2	4.	Simulation of the *keyboard encoder* circuit	
2	5.	VHDL code for the *7_segment_decoder* circuit	
2	6.	Simulation of the *7_segment_decoder* circuit	
2	7.	Testing of the *7_segment_decoder* circuit on the DE1 board	

Each part should be demonstrated to one of the TAs who will then give a grade and sign the grade sheet. Grades for each part will be either 0, 1, or 2. A mark of 2 will be given if everything is done correctly. A grade of 1 will be given if there are significant problems, but an attempt was made. A grade of 0 will be given for parts that were not done at all, or for which there is no TA signature.

ECSE 323 F2016