Group # 38

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ECSE 323: Lab Report 4

Group 38 VGA Test Pattern

Circuit name: VGA Test Pattern

Input: clock1(1 bit), rst1(1 bit), level_T(3bits), life_T (3 bits)

Output: R (4 bits), G (4 bits), B (4 bits), HSYNC1(1 bit), VSYNC1 (1 bit)

Description:
The purpose of the VGA test pattern circuit is used to display only a single line of text on the VGA monitor (Score, Level and Life). To do so we implemented the following design:

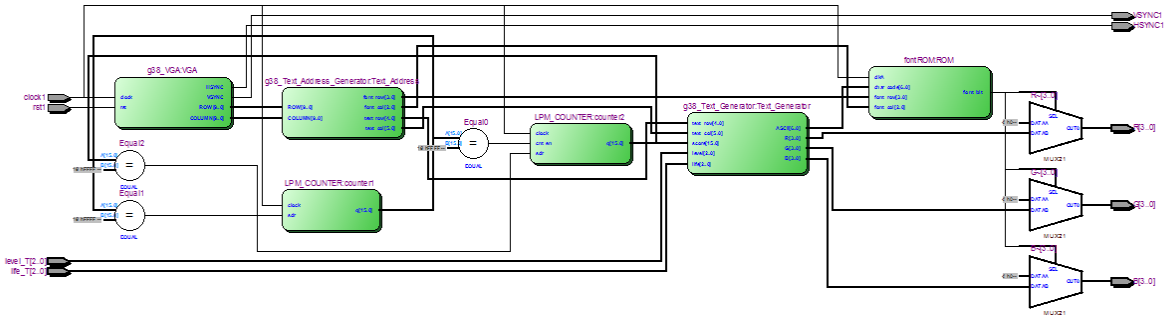

Figure 1.1: RTL view of the entire VGA Test Pattern circuit

The VGA circuit (designed in lab #3) generates the row and column coordinates of the pixel currently being drawn on the monitor screen.

The Text_Address_Generator circuit determines the location (text_row, text_col) of the character that is currently being drawn on the monitor screen. This treats character locations as being on 18 row by 50 column grid with horizontal spacing of 16 pixels and a vertical spacing of 32 pixels. It also generates the current pixel location within the character (font_row, font_col).

The Text_Generator determines the particular type of character that is currently being displayed (i.e. its ASCII code), based on the current character location (text_row, text_col), and various input parameters (score, level, life).

The fontROM circuit was premade and provided to us. This outputs a one bit signal, font_bit, which corresponds to the pixel value (on/off) at row font_row and column font_col in the character with 7-bit ASCII code char_code.

Finally, for the **VGA test pattern** (See figure 1.2 for pinout) all of the above components were connected together. Additionally, two counters are implemented using the LPM counter module to increment the score value. The first counter was used to increment the second counter when a high value of 2^16 was reached. This enabled us to slow down the counting rate of the score value to a readable speed on the VGA monitor. The Video Overlay from the lab description was created inside the VGA test pattern circuit. This was done by implementing 3 MUX(multiplexers) in the last phase of the VGA test pattern to output the R, G, B colors obtained from the VGA Test Generator onto the VGA monitor when the output value of 'font_row' is '1' from the fontROM circuit. If the value of fontROM is not '1', then all the values of R, G, B are set to "0000" and no output is shown on the monitor.

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Pinout Diagram:

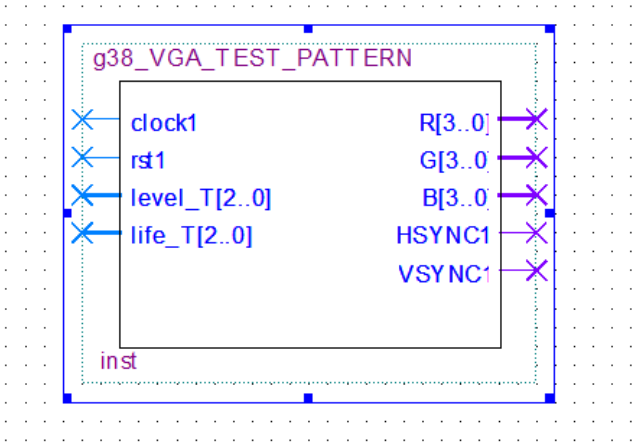

Figure 1.2: Pinout diagram for VGA Test Pattern circuit

Testing:

The completed VGA Test Pattern was programmed onto the Altera DE1 board and tested on a monitor via VGA. The inputs of level and life were controlled using the toggle switches on the board and tested for all the different values. A separate toggle switch was used for the reset function. The score counter increments were at a suitable rate since we implemented two counters to steady down the rate of change. Overall, the circuits performance was as desired and can be portrayed in the figures below:

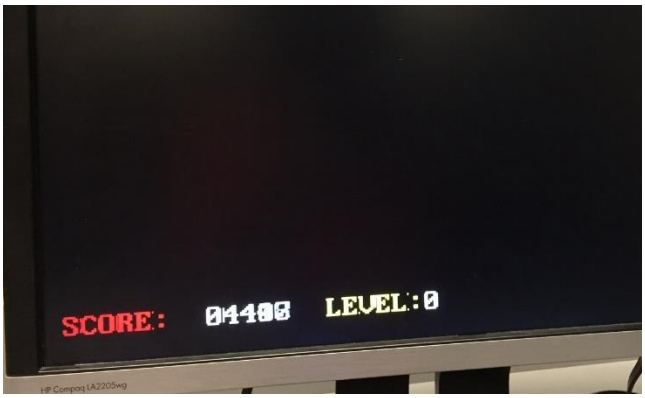

Figure 1.3a: Testing at level:0 & life:0

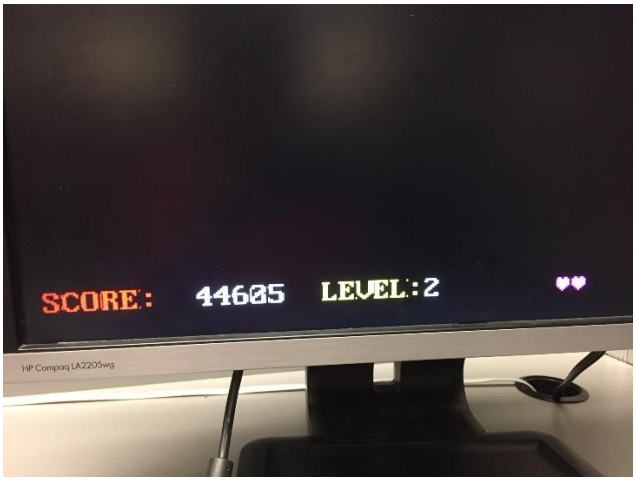

Figure 1.3b: Testing at level:2 & life:2

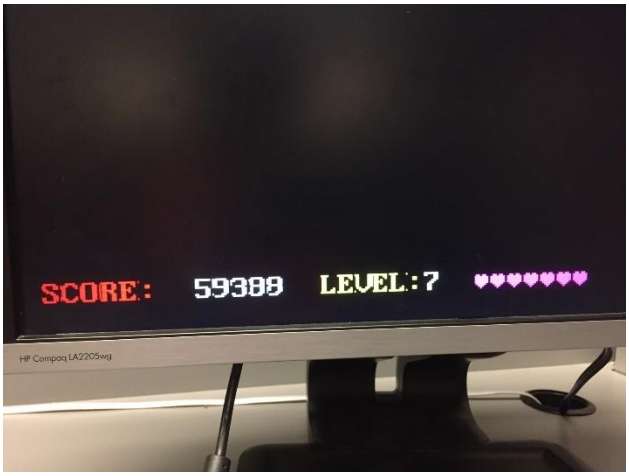

Figure 1.3c: Testing at level:7 & life:7

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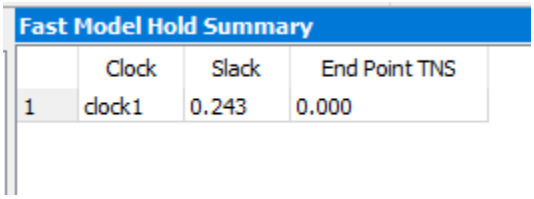
Summary of Time Quest timing analysis

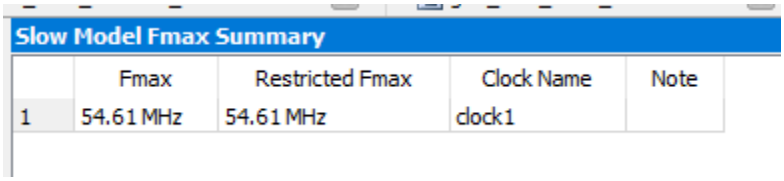
The time quest timing analysis was carried out by creating a sdc file with the instructions for the lab 4 slides. Upon execution we got positive values fast model hold slack and slow model setup slack. The slow model Fmax was also greater than 50 Mhz. All these combined has concluded that the timing requirements of the circuit was met. The results are shown below:



Fast Model Hold Summary

	Clock	Slack	End Point TNS
1	clock1	0.243	0.000

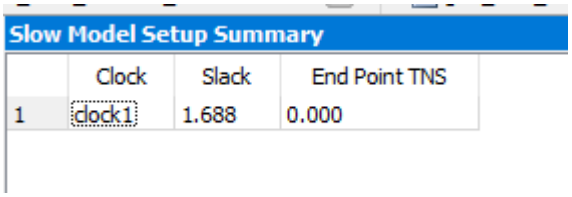
Figure 1.4a: Fast model hold slack value



Slow Model Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	54.61 MHz	54.61 MHz	clock1	

Figure 1.4b: Slow model Fmax



Slow Model Setup Summary

	Clock	Slack	End Point TNS
1	clock1	1.688	0.000

Figure 1.4c: Slow model setup slack value

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Summary of FPGA resource utilization

Flow Summary	
Flow Status	Successful - Thu Nov 24 17:17:00 2016
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Full Version
Revision Name	g38_VGA
Top-level Entity Name	g38_VGA_TEST_PATTERN
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Total logic elements	1,019 / 18,752 (5 %)
Total combinational functions	761 / 18,752 (4 %)
Dedicated logic registers	594 / 18,752 (3 %)
Total registers	594
Total pins	22 / 315 (7 %)
Total virtual pins	0
Total memory bits	45,056 / 239,616 (19 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)