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Title: G38 16 4 Encoder

Input: Block_col (16 bits)

Output: Code (4 bits), Error (1 bit)

Description: The purpose of this circuit is to take a 16-bit input which represents a number value of 0 to 2^16 and encode it to a 4-bit binary number indicating the index of the input bit that is high. The code is structured in a way of a priority encoder so that if one of the input bits are high it outputs the lowest index and in the case that none of the input are high an error output line is driven to a high value. For example: In the extra case of "0000" the error line is driven to a high. In other cases, the error line is at zero.

Pinout Diagram:

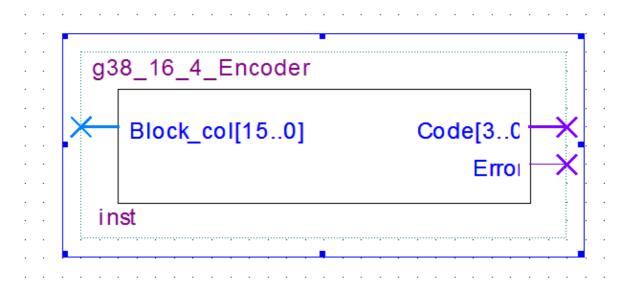


Figure 1: Pinout diagram for 16:4 Encoder Circuit

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Gate level diagram:

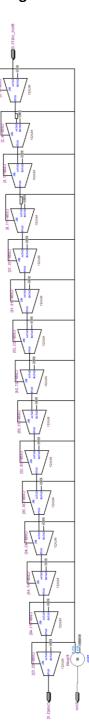


Figure 2: Gate level schematic of 16:4 Encoder Circuit

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Testing:

The circuit was tested using a functional simulation. Using a loop statement, the value of Block_col was incremented from 0 to 15 to verify the different scenarios. In the output waveform generated the value of each iteration was compared to the expected result. It can be concluded that the circuit works correctly since all the values of the output were in accordance to the values of the Block_col.

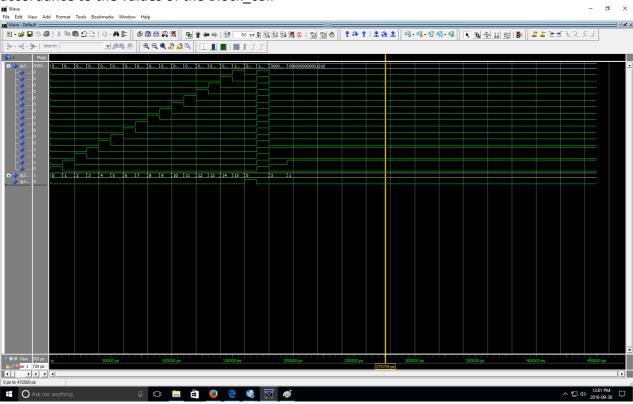


Figure 3: Simulation plot test for 16:4 Encoder Circuit

Simulation plot:

The stair like pattern of output from the index values of 0 to 15 is an easy way to understand that the circuit is behaving correctly. The error line stays at 0 for all values expect the special case when the input is "0000".

Group 38 – Lab 1 Report (ECSE 323)Tamim Sujat – 260551583

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國.	Grade Sheet for Lab #1	Fall 2016.
	Group Number: 38	
	Group Member Name: 9 WEWARULKHAN Student Number: 26 057-20	91 .
	Group Member Name: Tanin Sujat . Student Number: 26655158	<u>s</u>
Marks		0.1
-	Schematic diagram for the 6-bit comparator VHDL file for the 6-bit comparator	M.
2	VHDL file for the 6-bit comparator Initial partial simulation results for the 6-bit comparator	THE
5	Complete simulation results for the 6-bit comparator	Ala .
2	5. VHDL description for the 16:4 encoder circuit	Ali .
2	6. Simulation Testbench VHDL for the 16:4 encoder circuit	
2	7. Simulation results for the 16:4 encoder circuit	the same of the sa
		TA Signatures
Each pa	part should be demonstrated to one of the TAs who will then give a grade	and sign the
	sheet. Grades for each part will be either 0, 1, or 2. A mark of 2 will be g	
verythi	ning is done correctly. A grade of 1 will be given if there are significant	problems, but an
tempt	t was made. A grade of 0 will be given for parts that were not done at al	ll, or for which
	no TA signature.	