Beyond Moore's Law: VLSI Design in the Era of More-than-Moore

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***Abstract*—It may come as a shock to hear that the most famous law in the computer industry follows the trajectory of a saturation curve. The field of electronics and computing has long been driven by Moore's Law, which states that the number of transistors on an integrated circuit (IC) will double every two years. For a long period, this scaling remained the key engine of technological growth. However, contextually, we are reaching a saturation point. When transistors are scaled down to a smaller size than a certain threshold, quantum tunneling effects take place, leading to leakage current and untrustworthy cycling. The innovation in the semiconductor industry is no longer focused purely on reducing size; it is happening beyond the aspect of scaling through new architectures, materials, and integration techniques. This paper explores the "More-than-Moore" (MtM) paradigm, focusing on heterogeneous integration, 3D-ICs, and chiplet architectures as the sustainable path forward.**

***Index Terms*—Moore's Law, VLSI, More-than-Moore, 3D-IC, Chiplets, Heterogeneous Integration.**

I. Introduction

Moore's Law is widely considered the governing rule of the computer industry. It states that the number of transistors on an integrated circuit (IC) will double approximately every two years [1]. This scaling has been the primary engine of technological growth for decades.

However, we are reaching a physical saturation point. When transistors are scaled down beyond a specific threshold, quantum tunneling effects occur. This allows electrons to "tunnel" through barriers where they should be blocked, resulting in leakage current, untrustworthy on/off cycling, and increased static power consumption. Consequently, innovation in the semiconductor industry is no longer focused solely on scaling. It is occurring beyond the aspect of scaling through newly developed architectures, materials, and integration techniques.

II. Background: The End of Moore's Law

Gordon Moore, co-founder of Fairchild Semiconductor and Intel, forecasted in 1965 that transistor doubling would continue for ten years; surprisingly, it has remained relevant to this day. However, in the contemporary world, IC technology stretches the limits of physics. The distance between the gates of transistors is now so small that charge-carrying electrons are able to pass through unintended channels [1].

A. Dennard Scaling And Breakdown

Robert Dennard's invention of the 4-bit microprocessor in 1974 brought a theory of transistor scaling rules known as Dennard Scaling. He ventured that if the device size could be scaled down by a factor of $1/k$, and the concentration of dopants raised by k, the voltage would be decreased by $1/k$. Therefore, the delay would decrease by $1/k$, and power dissipation would be reduced by $1/k^2$. This allowed transistors to operate at higher speeds using less power with constant power density [2].

As long as these conditions were met, the industry received performance enhancements "for free." But this scaling has broken down due to leakage currents and heating effects. The power density is no longer a constant value, leading to the so-called "power wall."

B. Economic Factors

There is also an economic slowdown in process node advancement; the cost per transistor can no longer fall at historical rates. This has resulted in the rise of alternative value metrics, including energy efficiency and performance-per-watt, rather than raw transistor count.

III. The "More-Than-Moore" Paradigm

The "More-than-Moore" (MtM) paradigm exemplifies a new approach to semiconductor innovation. It attempts to achieve higher performance via a different path than conventional scaling. While "More Moore" is concerned with scaling down transistors and putting increasingly more of them on a single chip, MtM focuses on parallel functional diversification, heterogeneous integration, and system-level innovation [3].

The aim is to integrate both digital and non-digital functionalities (RF, power sensors, actuators, and mixed-signal components) into compact designs, specifically targeting the interface of the digital and analog domains [4].

A. Key Directions in MtM

1) Heterogeneous Integration: This entails combining different technologies to create a highly diverse system. It includes integrating sensors, analog/mixed-signal components, and passive elements in the same package as CMOS blocks [4]. Direct wafer bonding facilitates this by bonding together different substrate materials, making the integration of compound semiconductors with silicon devices possible.

2) Advanced Devices: New devices designed with MtM concepts may provide reasonable performance for lower supply voltages and are studied for use in applications demanding higher frequency switching. Reconfigurable Field Effect Transistors (RFETs), which can switch between n-channel and p-channel behavior, are also being developed for MtM applications.

B. Materials

Carbon-containing materials such as nanotubes and graphene are being explored for applications aside from scaling. Atomic layer deposition techniques are being researched to extend Moore's Law, especially for 3D complex structures.

IV. 3D-ICs and TSVs in More than Moore

3D Integrated Circuits (3D-ICs) and Through-Silicon Vias (TSVs) are integral to MtM functionality because they enable large increases in density, performance, and functionality without purely depending on scaling down transistors.

A. Greater Density and Functionality

3D-ICs achieve integration by providing greater functionality within smaller packaging. This enables the vertical stack bonding of diverse dies including logic, memory, analog, RF, and MEMS, which can be produced at different process nodes. This provides a solution to System-on-Chip (SoC) integration delays caused by expensive transitions to new process nodes.

B. Performance and Bandwidth

TSVs facilitate high performance by significantly reducing the lengths of interconnects, leading to improved electrical performance. The growing communication density in 3D-ICs leads to faster data transfer speeds and reduced latencies [6].

C. Reduction of Power

Interconnects in 3D-ICs are shorter, which reduces signal degradation and energy loss, leading to reduced power consumption compared to traditional 2D counterparts.

D. Thermal Management

The three-dimensional stacking of layers in 3D-ICs enables good dissipation of heat, thereby resolving thermal difficulties associated with densely packed electronics.

V. System-on-Chip (SoC) and System-in-Package (SiP)

Both SoC and SiP are essential for the MtM concept, representing different strategies of combining functionalities.

A. System-on-Chip (SoC)

Traditionally, SoC aims to integrate all functions onto a single chip. While this conforms to Moore's Law by pushing miniaturization, it encounters growing complexity and cost challenges at advanced nodes.

B. System-in-Package (SiP)

SiP is considered a key solution to "Moore Stress." It refers to the packaging of two or more dies, often stacked on an interconnection substrate within a single package. It allows for heterogeneous integration of logic, memory, RF, MEMS, and optical components which do not necessarily scale together [8]. SiP offers smaller size, lower cost, and faster time-to-market by leveraging commercial off-the-shelf components.

VI. Chiplet-Based Architectures

Chiplet-based architectures represent a paradigm shift in semiconductor design, using a modular approach compatible with the MtM era.

A. Overcoming Limitations

Chiplets are an attractive alternative to monolithic designs. Complex systems are subdivided into specialized functional blocks produced separately and packed using advanced processes [9]. A universal "socket" standard (similar to UCIe) allows designers to purchase a CPU chiplet from one vendor and an AI accelerator from another, gluing them together in one package.

B. Heterogeneous Integration and Efficiency

Chiplets allow different functional blocks to be optimized on different process nodes. This enables designers to develop highly customized systems. Furthermore, chiplet architectures can boast higher performance while reducing power consumption due to tighter integration of compute and memory units.

C. Adaptability to AI Era

Chiplet architectures are especially well-suited for the demands of Generative AI workloads, which require huge parallel processing and high-bandwidth memory that single-chip designs cannot economically deliver.

VII. Integration of Photonics, Bioelectronics, and Quantum Components

A. Photonics Integration

Silicon photonics extends scaling beyond electrical interconnects by integrating optical waveguides, modulators, and detectors on standard silicon wafers. This addresses the limitations of copper-based interconnects (high insertion loss, crosstalk) by enabling low-latency, energy-efficient optical communication.

B. Bioelectronics and Quantum

Bioelectronics falls under the MtM umbrella, dealing with the integration of biological systems with electronic components. Similarly, quantum computing is adopting modular architectures and chiplet-like designs to meet performance targets, requiring the embedding of components that move beyond classical electronic processing.

VIII. Modern VLSI Design Challenges

The VLSI design environment is facing a transition from Moore's Law to the MtM era.

A. Complexity and EDA

Electronic Design Automation (EDA) is an enabler for VLSI design as chip complexity exceeds human capability. Modern chips with billions of transistors require advanced algorithms for physical design and precise SPICE models.

B. Thermal Management and STCO

As VLSI designs transition to 3D stacked architectures, the trade-off between power delivery and heat removal becomes critical. System Technology Co-Optimization (STCO) is a framework incorporating both system cues and technology-level optimization, potentially yielding up to 61% power saving at iso-delay.

IX. Simulation Methodology and Analysis

To assess the effect of the MtM approach, particularly 3D integration on wirelength and signal delay, we utilized a Monte Carlo simulation framework. The simulation reflects the transition from a standard 2D planar architecture to a 2-tier 3D IC.

A. Scope and Parameters

The research concerns Block Level Floorplanning rather than Gate Level placement. The geometric constraints simulate a mid-range SoC (common in smartphones):

- **Die Area:** 100 mm^2 (Base 2D size of 10 mm $\times$ 10 mm).
- **Node Number:** $N = 2000$ distinct functional blocks (macros).
- **Tier Height:** 50μm, assuming standard wafer thinning.

B. Electrical Interconnect Model

We used the Elmore Delay model to compute signal propagation. Electrical parameters were obtained from ITRS projections (Table I).

TABLE I
Simulation Electrical Parameters

Parameter	Value	Justification
Wire Resistance (R)	0.08Ω/μm	Intermediate Cu layer
Wire Capacitance (C)	0.20 fF/μm	Fringing capacitance
TSV Resistance (R_{tsv})	0.05Ω	Cu TSV (5μm dia, 50μm)
TSV Capacitance (C_{tsv})	10.0 fF	TSV liner oxide parasitic

C. Area Overhead Modeling

A critical element is the TSV Area Penalty. The total silicon area in 3D is defined as:

$$A_{3D} = \frac{A_{2D}}{N_{tiers}} + (N_{TSV} \times A_{TSV}) \quad (1)$$

Where A_{TSV} is set to 25μm^2 (5μm $\times$ 5μm exclusion zone). This reflects the trade-off where 3D stacking shrinks chip size but vertical connectivity introduces area bloat.

D. Simulation Results

The simulation of the transition from a standard 2D architecture to a 2-tier 3D IC yielded significant improvements in interconnect performance:

- **Wirelength Reduction (26.41%):** A considerable amount of reduction in the global wirelength was obtained by the 3D floorplanning. This is because the functional blocks are stacked up vertically. As a result, the "Manhattan distance" between the connected functional blocks gets reduced. It is clear that the 3D approach is useful in overcoming the bottleneck of global interconnects in the SoC.

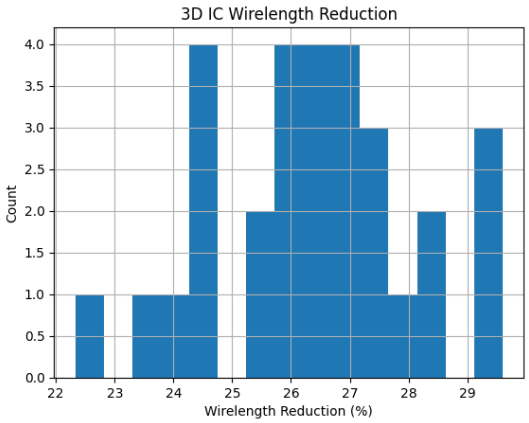

Fig. 1. Simulation of the reduction of wirelenght in a 3D IC

- **Delay Reduction (40.01%):** The metric for improved timing, which is 40.01 percent, showed a substantial acceleration compared to that of wirelength, which was 26.41 percent. This happens because, as a function of resistance and capacitance, delay, as calculated by Elmore Delay, is nonlinearly correlated to a decrease in wirelength. This also demonstrates that 3D ICs are superior to traditional plane semiconductors in terms of providing faster data transfer speed and performance.

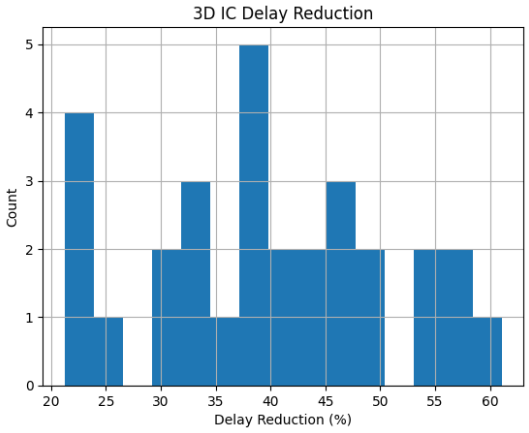

Fig. 2. Simulation of delay reduction in a 3D IC

- **TSV Efficiency (0.049 TSVs/Net):** TThis value is an indication of an optimal partitioning of the netlist achieved by the design. This design effectively packs highly connected functional modules into the same tier because it achieves a ratio of one TSV per 20 nets, thus the "TSV Area Penalty" is avoided because the performance benefit is not achieved at the expense of area overhead.

X. Case Studies

A. TSMC's CoWoS and InFO

TSMC has made significant strides with CoWoS (Chip-on-Wafer-on-Substrate). This technology enables integrating multiple dies into a single package, offering high bandwidth for HPC and AI applications. They also lead in silicon photonics, exploring co-design of Photonic Integrated Circuits (PICs) [10].

B. Intel's Foveros and EMIB

Intel utilizes Foveros 3D packaging and EMIB (Embedded Multi-die Interconnect Bridge). These innovations allow stacking and interconnecting different processors and memory into compact systems for AI workloads.

C. AMD's Chiplet Design

AMD successfully adopted a chiplet-based approach for Ryzen and EPYC processors. By integrating multiple smaller dies onto a single package, they achieve scalability and cost-efficiency previously unattainable with monolithic designs.

XI. Future Outlook

The Future of VLSI will include the simultaneous integration of Digital, Analog, and Non-Digital Systems. Photonics will become a key driver, leading to Electronic-Photonic Integrated Circuits. Standardization via UCIe will enable mixing chiplets from different vendors. Moreover, AI-powered EDA ("Circuit Foundation Models") will automate complex verification and layout synthesis.

XII. Conclusion

Moore's Law has started to slow, yet innovation remains. The "More-than-Moore" paradigm typifies a sustainable evolution path. The VLSI designer has become multi-disciplinary, spanning architecture, materials science, and packaging. As the simulation methodology shows, the transition to 3D architecture involves new challenges between area and performance that must be carefully managed.

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