
STM32
CubeMX

1. Description

1.1. Project

Project Name	uti1
Board Name	NUCLEO-H745ZI-Q
Generated with:	STM32CubeMX 6.8.1
Date	07/03/2023

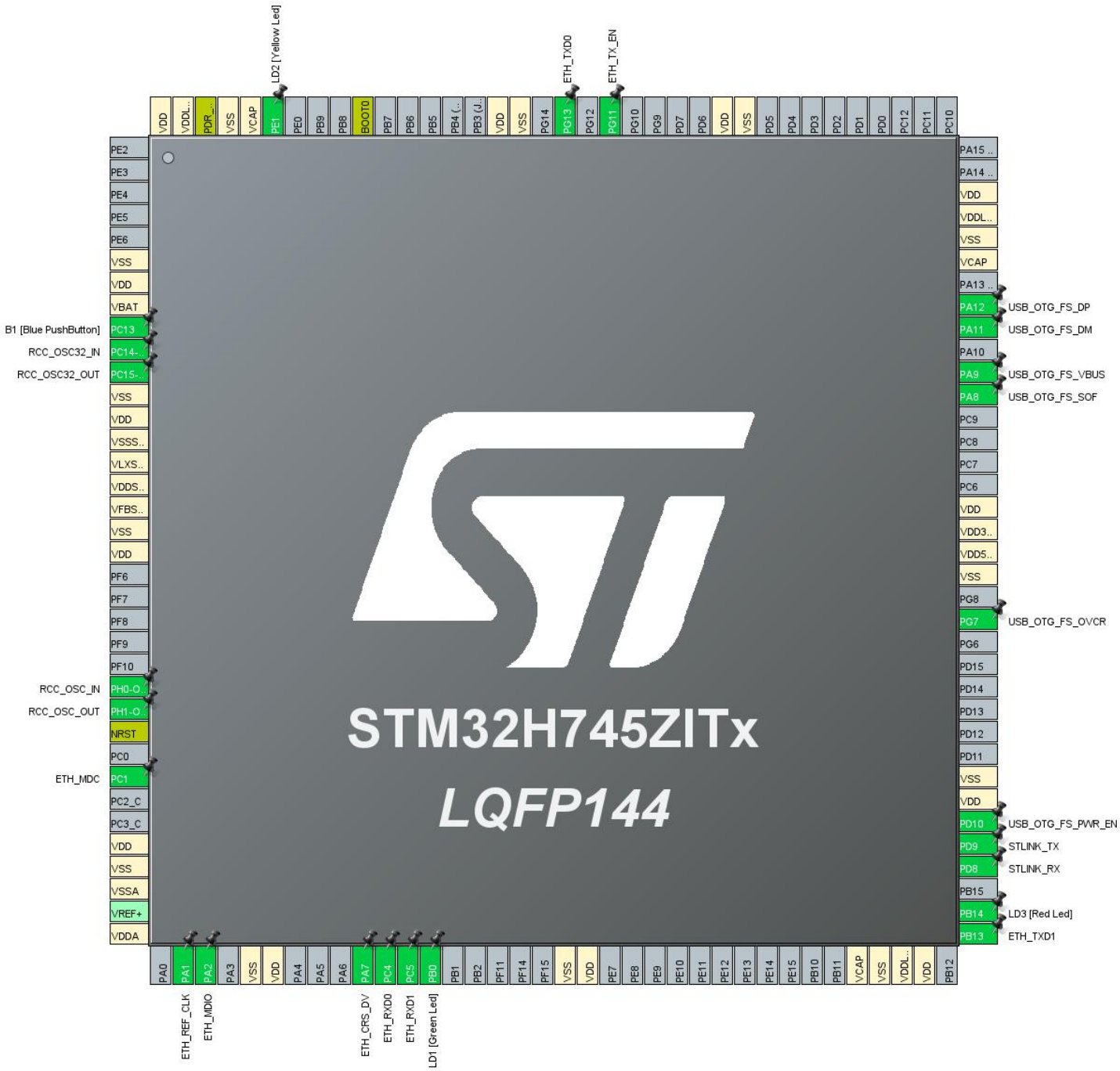
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H745/755
MCU name	STM32H745ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	ARM Cortex-M7 ARM Cortex-M4

2. Pinout Configuration



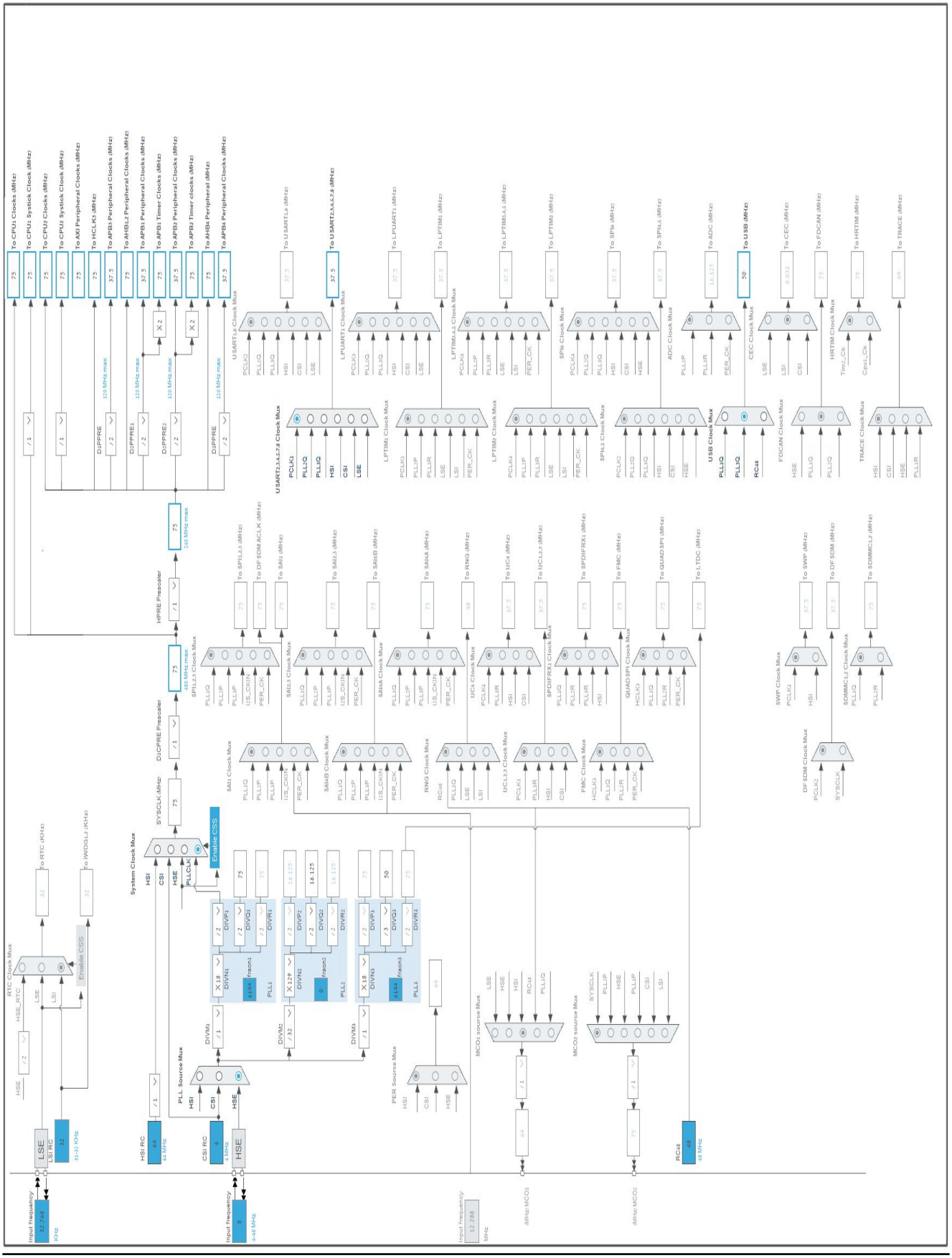
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VSS	Power		
7	VDD	Power		
8	VBAT	Power		
9	PC13 *	I/O	GPIO_Input	B1 [Blue PushButton]
10	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
11	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
12	VSS	Power		
13	VDD	Power		
14	VSSSMPS	Power		
15	VLXSMPS	Power		
16	VDDSMPS	Power		
17	VFBSMPS	Power		
18	VSS	Power		
19	VDD	Power		
25	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
26	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
27	NRST	Reset		
29	PC1	I/O	ETH_MDC	
32	VDD	Power		
33	VSS	Power		
34	VSSA	Power		
36	VDDA	Power		
38	PA1	I/O	ETH_REF_CLK	
39	PA2	I/O	ETH_MDIO	
41	VSS	Power		
42	VDD	Power		
46	PA7	I/O	ETH_CRS_DV	
47	PC4	I/O	ETH_RXD0	
48	PC5	I/O	ETH_RXD1	
49	PB0 *	I/O	GPIO_Output	LD1 [Green Led]
55	VSS	Power		
56	VDD	Power		
68	VCAP	Power		
69	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
70	VDDLDO	Power		
71	VDD	Power		
73	PB13	I/O	ETH_TXD1	
74	PB14 *	I/O	GPIO_Output	LD3 [Red Led]
76	PD8	I/O	USART3_TX	STLINK_RX
77	PD9	I/O	USART3_RX	STLINK_TX
78	PD10 *	I/O	GPIO_Output	USB_OTG_FS_PWR_EN
79	VDD	Power		
80	VSS	Power		
87	PG7	I/O	GPIO_EXTI7	USB_OTG_FS_OVCR
89	VSS	Power		
90	VDD50_USB	Power		
91	VDD33_USB	Power		
92	VDD	Power		
97	PA8	I/O	USB_OTG_FS_SOF	
98	PA9	I/O	USB_OTG_FS_VBUS	
100	PA11	I/O	USB_OTG_FS_DM	
101	PA12	I/O	USB_OTG_FS_DP	
103	VCAP	Power		
104	VSS	Power		
105	VDDLDO	Power		
106	VDD	Power		
118	VSS	Power		
119	VDD	Power		
124	PG11	I/O	ETH_TX_EN	
126	PG13	I/O	ETH_TXD0	
128	VSS	Power		
129	VDD	Power		
135	BOOT0	Boot		
139	PE1 *	I/O	GPIO_Output	LD2 [Yellow Led]
140	VCAP	Power		
141	VSS	Power		
142	PDR_ON	Reset		
143	VDDLDO	Power		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	uti1
Project Folder	C:\Users\ghkh1\STM32CubeIDE\workspace_2\uti1
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls ARM Cortex-M7

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ETH_Init	ETH
4	MX_USART3_UART_Init	USART3
5	MX_USB_OTG_FS_PCD_Init	USB_OTG_FS
6	MX_TIM16_Init	TIM16

5.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

Rank	Function Name	Peripheral Instance Name

Rank	Function Name	Peripheral Instance Name
1	MX_ETH_Init	ETH
2	MX_USART3_UART_Init	USART3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H745/755
MCU	STM32H745ZITx
Datasheet	DS12923_Rev1

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(DD36000)
Capacity	36000.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	450.0 mA
Max Pulse Current	1000.0 mA
Cells in series	1
Cells in parallel	1

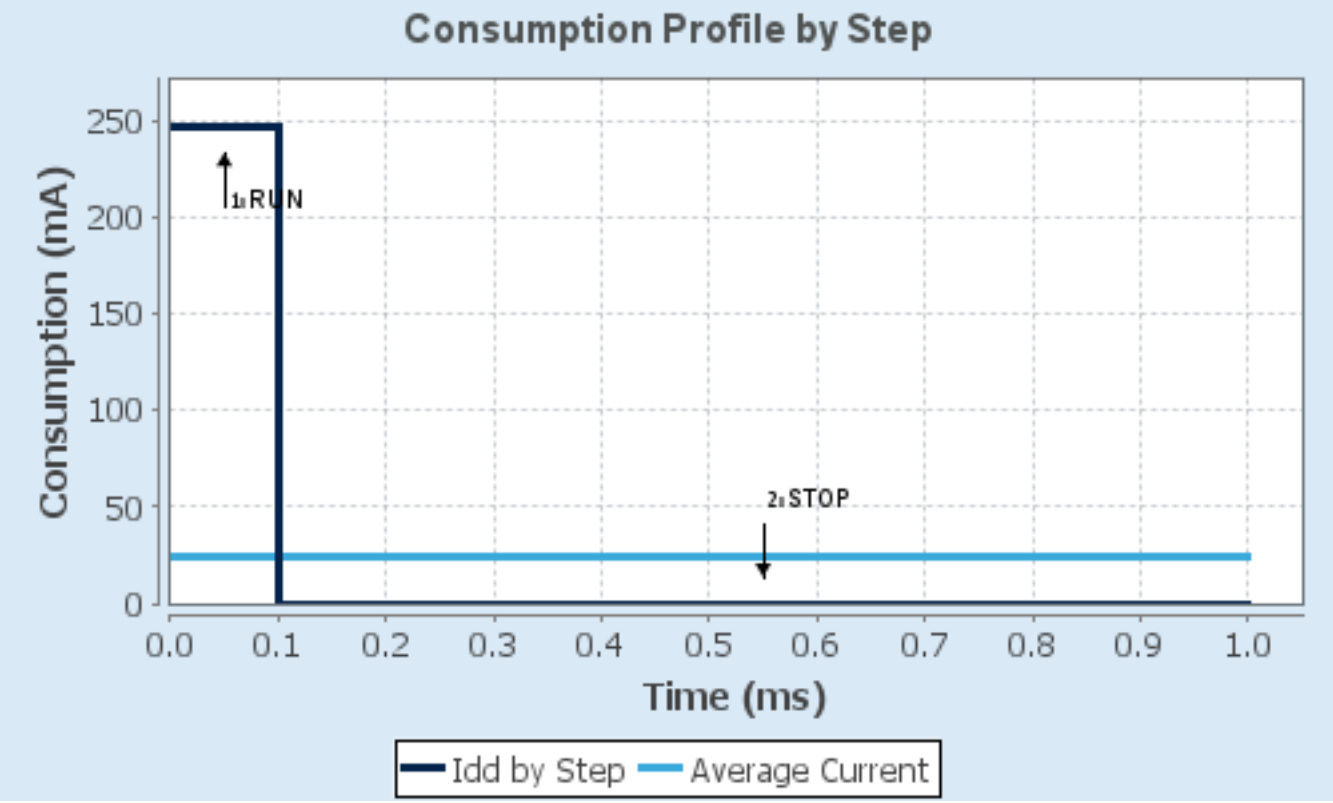
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN/CRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	CM7: ITCM/Cache / CM4: FLASH_B/ART	CM7: NA / CM4: NA
CM7 Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL ALL_IPs_ON	LSE Flash-ON
CM4 Frequency	240 MHz	0 Hz
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	247 mA	145 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	24.83 mA
Battery Life	1 month, 29 days, 21 hours	Average DMIPS	1027.2001 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
250
200
150
100
50
0
1: RUN
2: STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ETH

Mode: RMII

7.1.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	D2

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30000200 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30000000 ***
Rx Buffers Length	1524

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	D3

Power Parameters:

SupplySource	PWR_DIRECT_SMPS_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100

LSE Startup Timout Value (ms)	5000
CSI Calibration Value	32
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	1 WS (2 CPU cycle)
Product revision	rev.V

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL3 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	MEDIUM VCO range
PLL3 clock Output range	MEDIUM VCO range

7.3. SYS

Timebase Source: SysTick

7.3.1. Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	

7.4. SYS_M4

Timebase Source: SysTick

7.4.1. Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	

7.5. TIM16

mode: Activated

7.5.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**7500-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10000 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

7.6. USART3

Mode: Asynchronous

7.6.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	D2

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable

Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.7. USB_OTG_FS
Mode: Device_Only
Activate_VBUS: VBUS sensing
mode: Activate_SOF

7.7.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2
Speed	Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Low power	Disabled
Battery charging	Enabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Enabled
Signal start of frame	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7* Cortex-M4	D2
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7* Cortex-M4	D2
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7* Cortex-M4	D2
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7* Cortex-M4	D2
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7* Cortex-M4	D2
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7* Cortex-M4	D2
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7* Cortex-M4	D2
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7* Cortex-M4	D2
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7* Cortex-M4	D2
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_RX	Cortex-M7* Cortex-M4	D2
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_TX	Cortex-M7* Cortex-M4	D2
USB_OTG_FS	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	n/a		Cortex-M7	D2
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D2
	PA12	USB_OTG_F	Alternate Function	No pull-up and no pull-	Low		Cortex-M7	D2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
		S_DP	Push Pull	down				
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	B1 [Blue PushButton]	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Green Led]	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red Led]	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_OTG_FS_PWR_EN	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PG7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USB_OTG_FS_OVCR	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Yellow Led]	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4

* Initialized context

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC1

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM16 global interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line[9:5] interrupts	unused		
USART3 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 86	unused		
CM4 send event interrupt for CM7	unused		
FPU global interrupt	unused		
USB On The Go FS End Point 1 Out global interrupt	unused		
USB On The Go FS End Point 1 In global interrupt	unused		
USB On The Go FS global interrupt	unused		
HSEM1 global interrupt	unused		
RAM ECC diagnostic global interrupt	unused		
Hold core interrupt	unused		

8.5.2. NVIC1 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM16 global interrupt	false	true	true

8.5.3. NVIC2

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
EXTI line[9:5] interrupts	unused		
CM7 send event interrupt for CM4	unused		
FPU global interrupt	unused		
HSEM2 global interrupt	unused		
RAM ECC diagnostic global interrupt	unused		
Hold core interrupt	unused		

8.5.4. NVIC2 Code generation

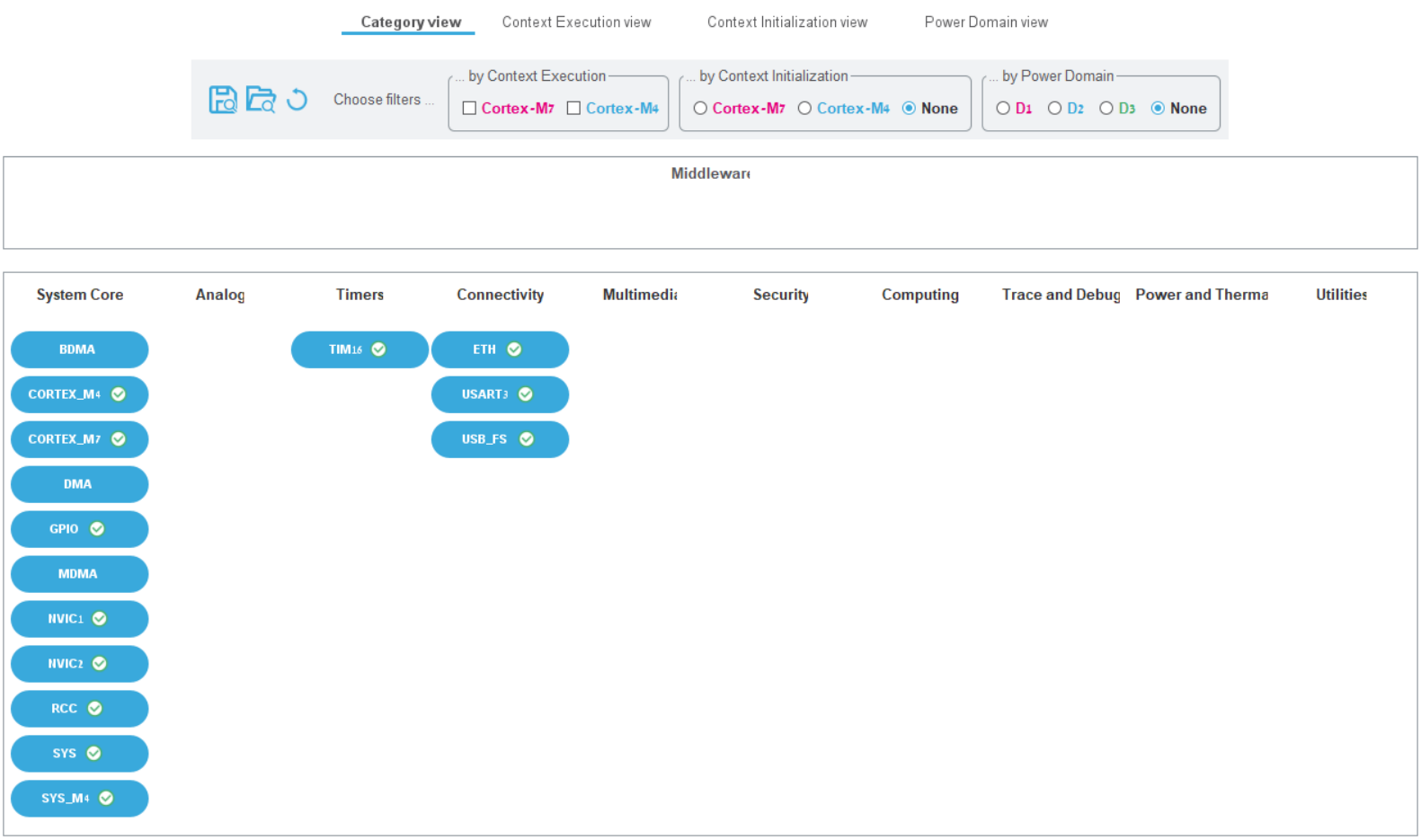
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

*** User modified value**

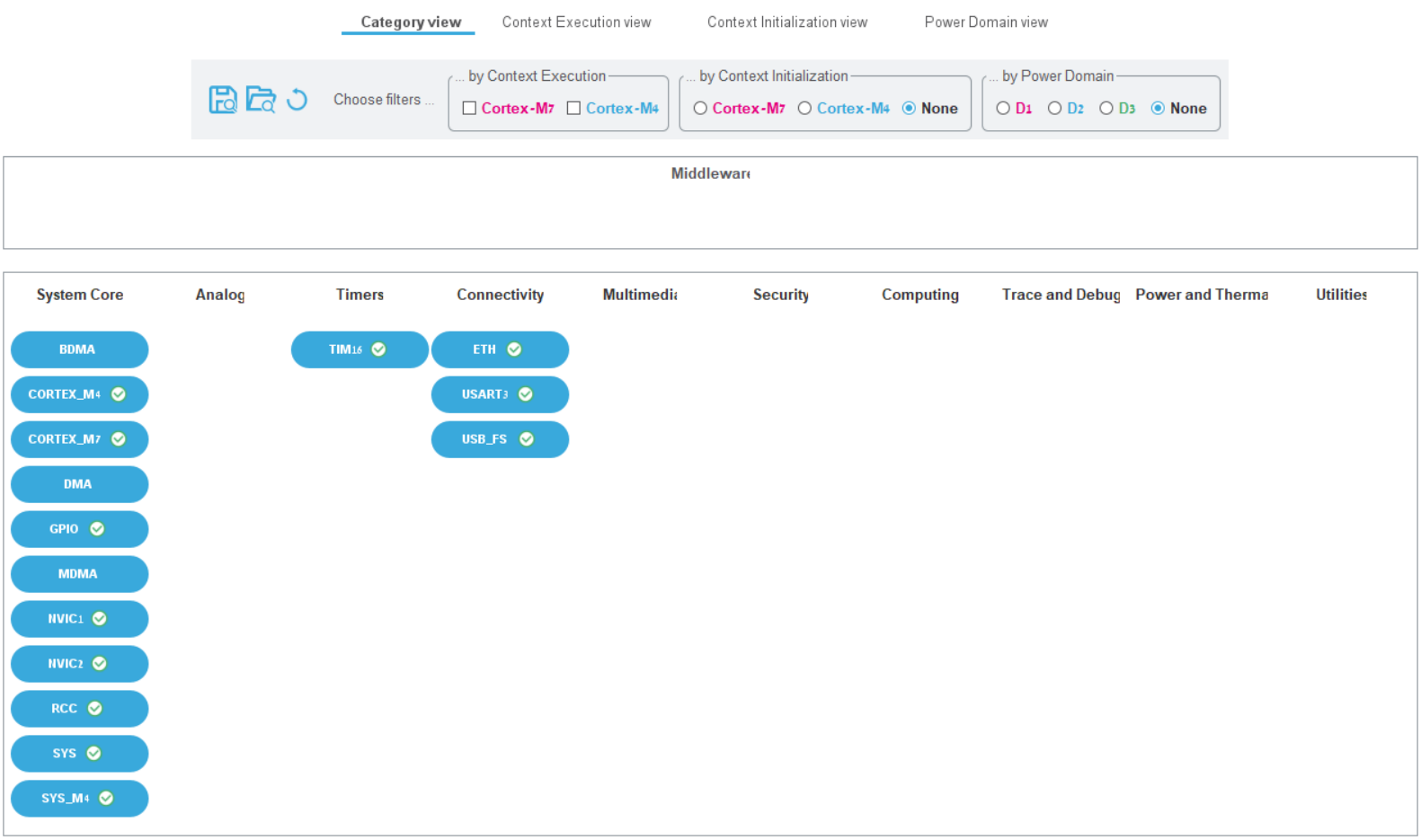
9. System Views

9.1. Category view

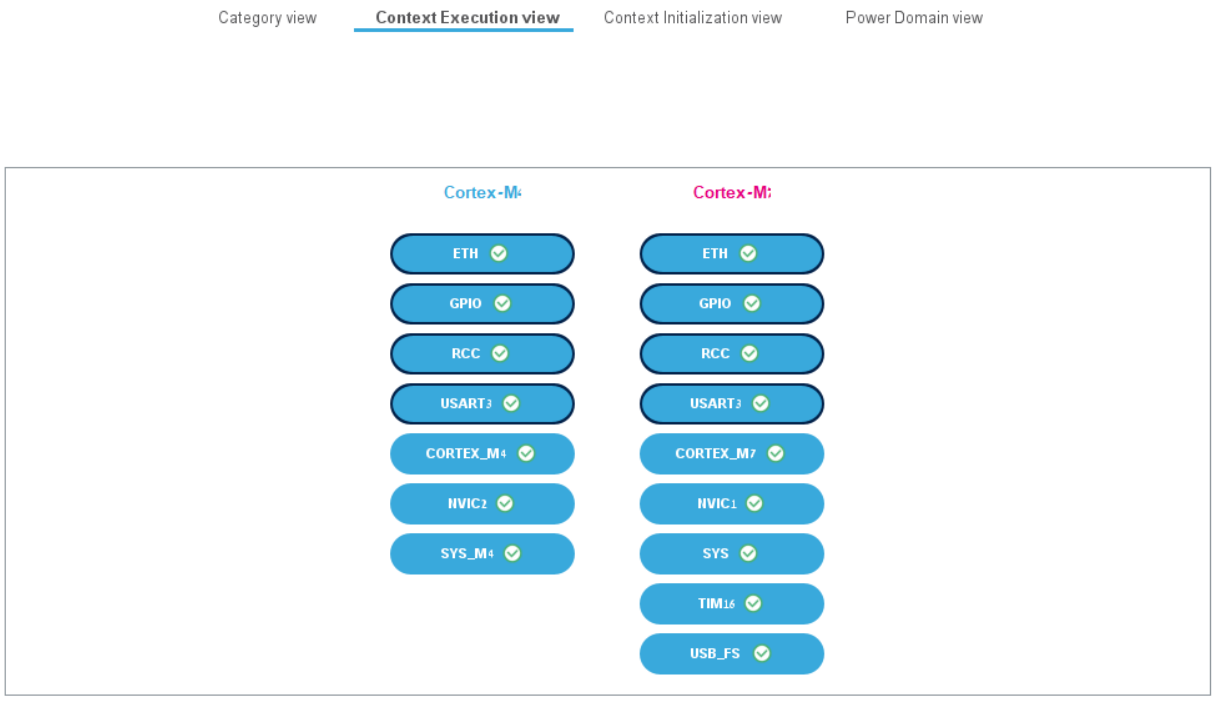
9.1.1. Current



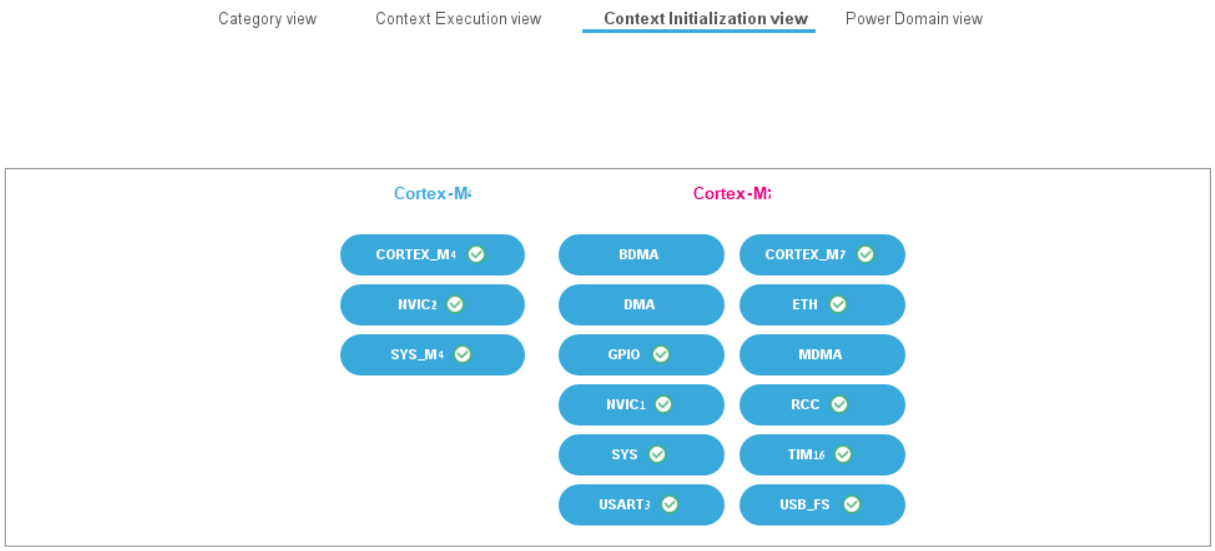
9.1.2. Without filters



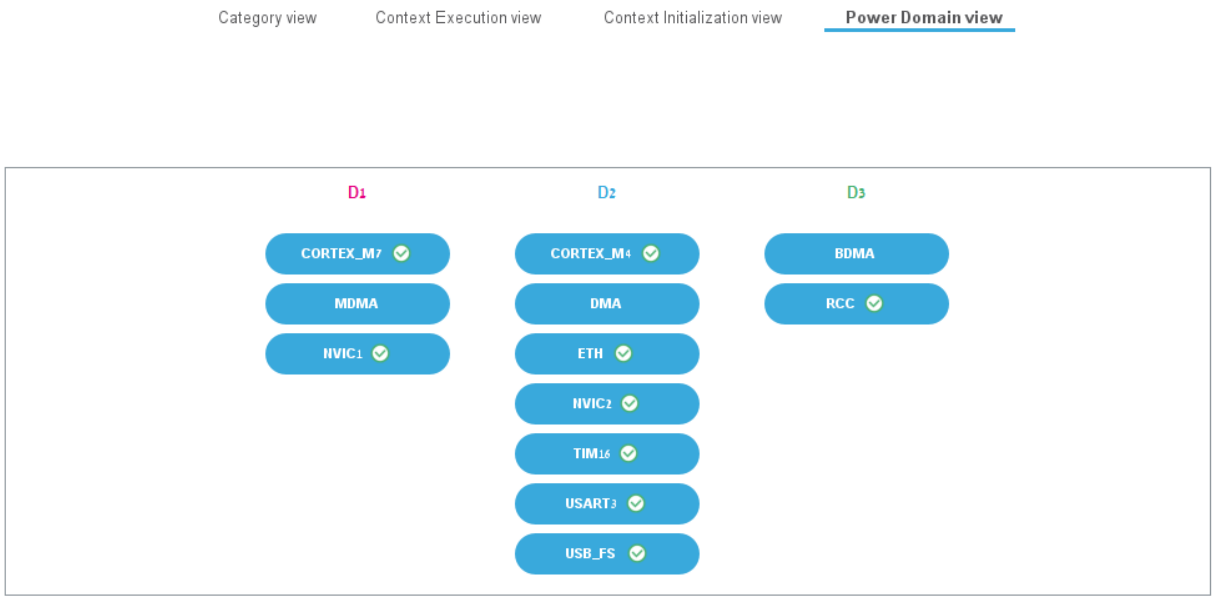
9.2. Context Execution view



9.3. Context Initialization view



9.4. Power Domain view



10. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32h7_svd.zip
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32h7_svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Training Material	https://www.st.com/resource/en/sales_guide/sg_sc2154.pdf
Training Material	https://www.st.com/resource/en/training_certification/faecp_stm32h7_dualcore_edr.pdf
Training Material	https://www.st.com/resource/en/training_certification/faecp_stm32h7_edr.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7vl.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1181-electrostatic-

	discharge-sensitivity-measurement-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2834-how-to-get-the-best-adc-accuracy-in-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2867-oscillator-design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4013-stm32-crossseries-timer-overview-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
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