Assign_4_Grp_27

**Assignment 4 (Verilog)
Group No 27
Question 1
Semester 5
Yash Sirvi (21CS10083)
Sanskar Mittal (21CS10057)

Arithmetic shift module

Input: Two 8 bit inputs `a` and `q`
Output: Two 8 bit outputs `a_out`, `q_out`
Behaviour:
It shifts q arithmetically towards the right by 1 bit.
Preserves the last bit of a and sets it as the msb of q
Arithmetic shifts a towards right by 1 bit

Adder module

Input: two 8 bit values n1 and n2
Output: 8 bit sum value
Behaviour:
Returns n1+n2

Subtractor module

Input: two 8 bit values n1 and n2
Output: 8 bit difference
Behaviour:
Returns n1-n2

Top Level module

Input:

- two 8 bit inputs `multiplicand` and `multiplier`
- one clock signal `clk`
  Output: 16 bit output `prod`
  Behaviour:
  Uses booths algorithm to calculate the product of multiplicand and mulitplier.
  We first initialise the values of our temporary registers.
  We then iterate 8 times on positive edge ofclock signal to perform the add or subtract operation of the booths algorithm

During the negative edge, we perform the shift operation of the booths algorithm. We also use a qbuff to store the value of `Q-1`.

Schematic