Assignment 6 Group 27

Assignment 4 (Verilog)
Group No 27
Question 1
Semester 5
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Q1

Top_Level module

Input:

- `clk` clock signal
- `reg_addr` address of register, 3 bits long
- `mem_addr` address of memory location, 4 bits long
- `data` Data to be written directly, 32 bits long
- `opcode` Code of the operation to be executed, 2 bits long

Output:

- `data_out` output register of 32 bit

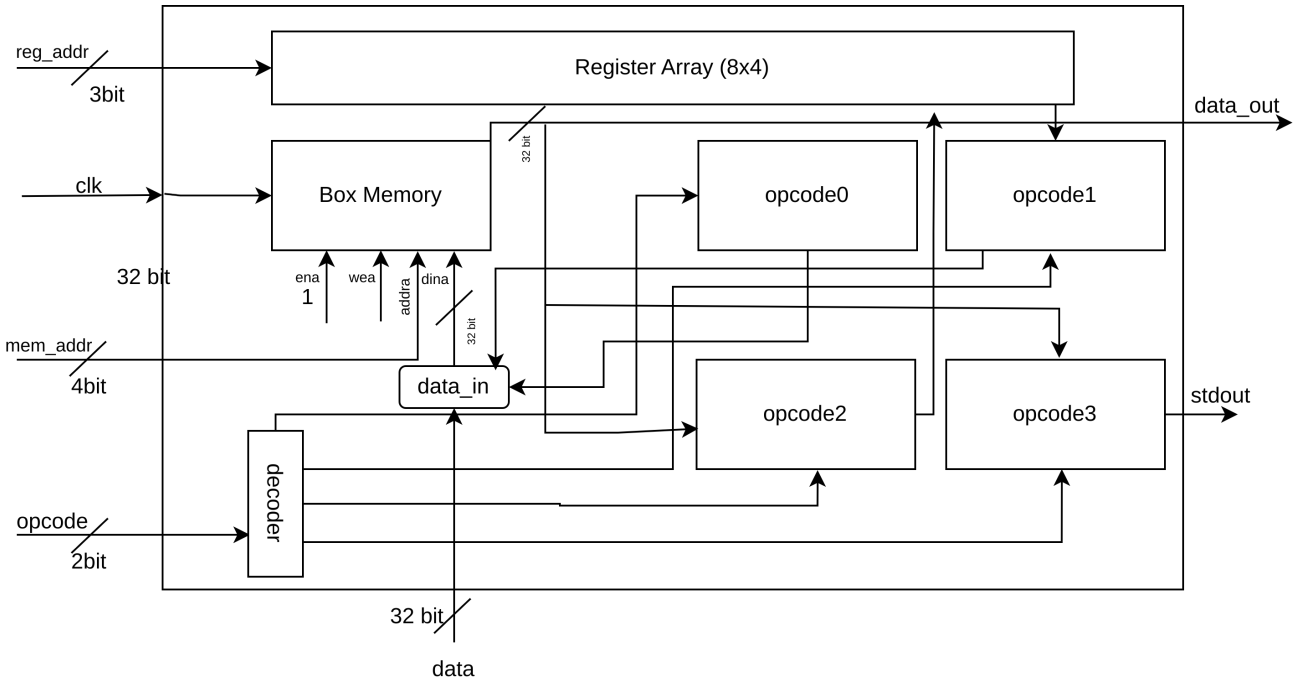
Opcode Definitions:

- `0` : Read a 4-bit data and store it into a specified memory location with 4-bit address
- `1` : Given a register number and a memory address, transfer data from register to memory
- `2` : Same as above, but transfer data from memory to register.
- `3` : Given a memory address, display the contents of the memory location

Testbench

- We first store the value `10` into memory location at address `4` using opcode `0`
- Then use the stored value of `4` th memory location into register `4` using opcode `2`
- And then write `4` th registers value into `12` th memory location using opcode `1`
- Finally we display the value of `12` th memory location using opcode `3`

Schematic


reg_addr
3bit
Register Array (8x4)
data_out
clk
Box Memory
32 bit
opcode0
opcode1
32 bit
ena
1
wea
addra
dina
32 bit
mem_addr
4bit
data_in
opcode2
opcode3
stdout
decoder
opcode
2bit
32 bit
data