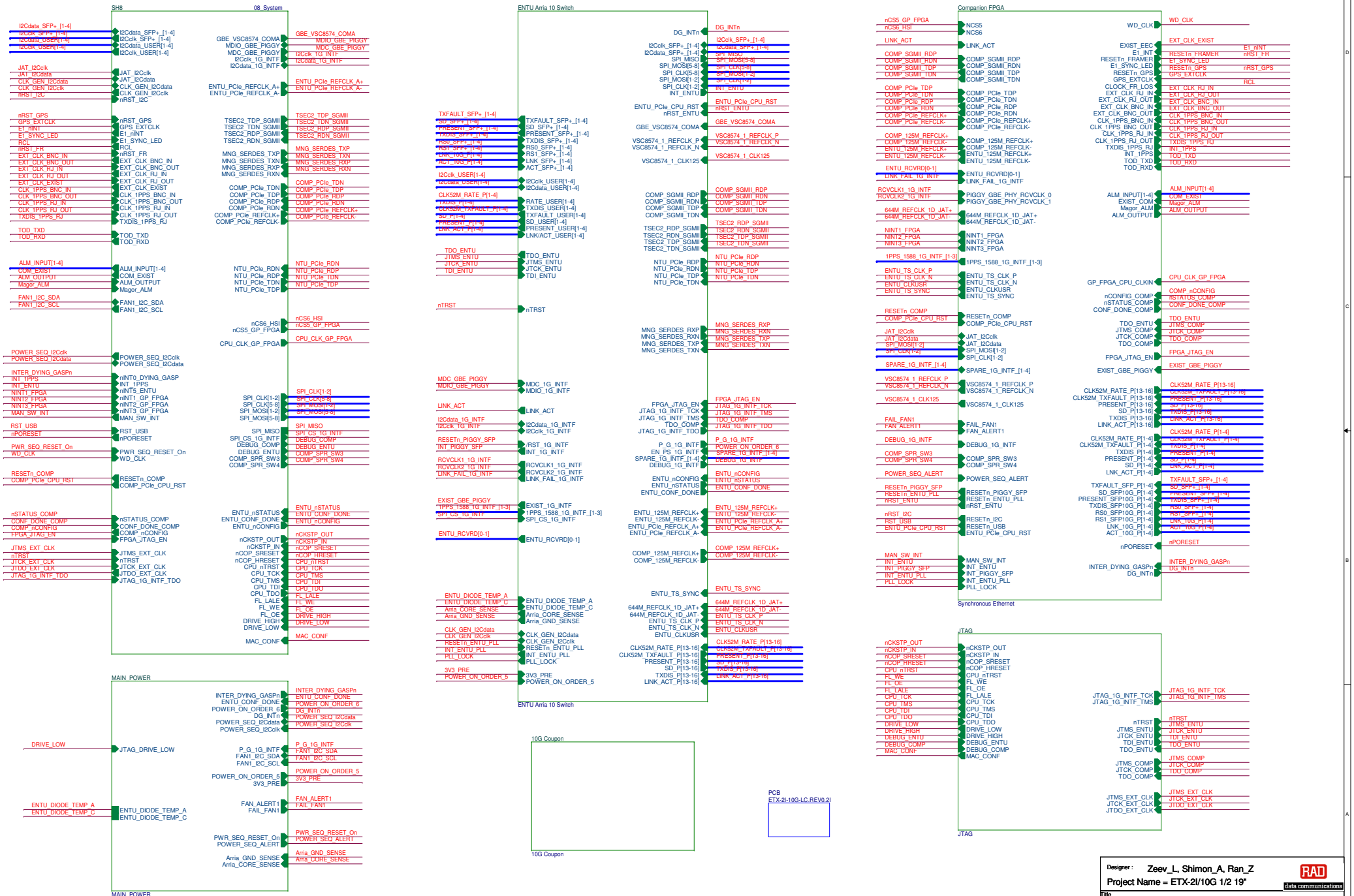
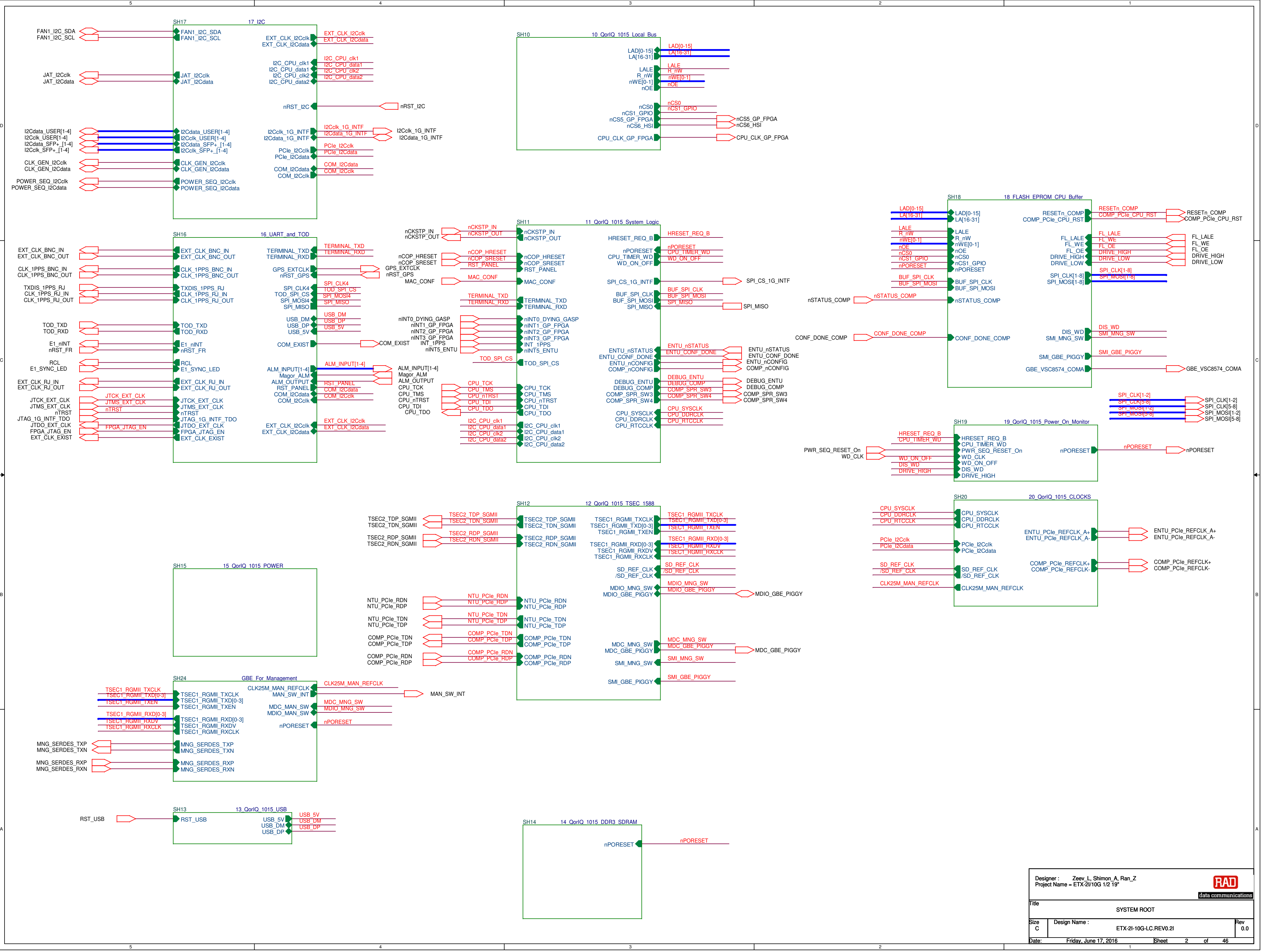
ETX-2i/10G 1/2 19" MAIN




SH17 17_I2C
FAN1_I2C_SDA
FAN1_I2C_SCL
JAT_I2Cclk
JAT_I2Cdata
I2Cdata_USER[1-4]
I2Cclk_USER[1-4]
I2Cdata_SFP+_[1-4]
I2Cclk_SFP+_[1-4]
CLK_GEN_I2Cclk
CLK_GEN_I2Cdata
POWER_SEQ_I2Cclk
POWER_SEQ_I2Cdata
EXT_CLK_I2Cclk
EXT_CLK_I2Cdata
I2C_CPU_clk1
I2C_CPU_data1
I2C_CPU_clk2
I2C_CPU_data2
nRST_I2C
I2Cclk_1G_INTF
I2Cdata_1G_INTF
PCIe_I2Cclk
PCIe_I2Cdata
COM_I2Cdata
COM_I2Cclk
SH10 10_QorIQ_1015_Local_Bus
LAD[0-15]
LA[16-31]
LALE
R_nW
nWE[0-1]
nOE
nCS0
nCS1_GPIO
nCS5_GP_FPGA
nCS6_HSI
CPU_CLK_GP_FPGA
SH18 18_FLASH_EPROM_CPU_Buffer
RESETn_COMP
COMP_PCIe_CPU_RST
nCS0
nCS1_GPIO
nPORESET
BUF_SPI_CLK
BUF_SPI_MOSI
FL_LALE
FL_WE
FL_OE
DRIVE_HIGH
DRIVE_LOW
SPI_CLK[1-8]
SPI_MOSI[1-8]
nSTATUS_COMP
CONF_DONE_COMP
DIS_WD
SMI_MNG_SW
SMI_GBE_PIGGY
GBE_VSC8574_COMA
SPI_CLK[1-2]
SPI_CLK[5-8]
SPI_MOSI[1-2]
SPI_MOSI[5-8]
SH16 16_UART_and_TOD
EXT_CLK_BNC_IN
EXT_CLK_BNC_OUT
CLK_1PPS_BNC_IN
CLK_1PPS_BNC_OUT
TXDIS_1PPS_RJ
CLK_1PPS_RJ_IN
CLK_1PPS_RJ_OUT
TOD_TXD
TOD_RXD
E1_nINT
nRST_FR
RCL
E1_SYNC_LED
EXT_CLK_RJ_IN
EXT_CLK_RJ_OUT
JTCK_EXT_CLK
JTMS_EXT_CLK
nTRST
JTAG_1G_INTF_TDO
JTDO_EXT_CLK
FPGA_JTAG_EN
EXT_CLK_EXIST
TERMINAL_TXD
TERMINAL_RXD
GPS_EXTCLK
nRST_GPS
SPI_CLK4
TOD_SPI_CS
SPI_MOSI4
SPI_MISO
USB_DM
USB_DP
USB_5V
COM_EXIST
ALM_INPUT[1-4]
Magor_ALM
ALM_OUTPUT
RST_PANEL
COM_I2Cdata
COM_I2Cclk
SH11 11_QorIQ_1015_System_Logic
nCKSTP_IN
nCKSTP_OUT
nCOP_HRESET
nCOP_SRESET
RST_PANEL
MAC_CONF
nINT0_DYING_GASP
nINT1_GP_FPGA
nINT2_GP_FPGA
nINT3_GP_FPGA
INT_1PPS
nINT5_ENTU
TOD_SPI_CS
CPU_TCK
CPU_TMS
CPU_nTRST
CPU_TDI
CPU_TDO
HRESET_REQ_B
nPORESET
CPU_TIMER_WD
WD_ON_OFF
SPI_CS_1G_INTF
BUF_SPI_CLK
BUF_SPI_MOSI
SPI_MISO
ENTU_nSTATUS
ENTU_CONF_DONE
ENTU_nCONFIG
COMP_nCONFIG
DEBUG_ENTU
DEBUG_COMP
COMP_SPR_SW3
COMP_SPR_SW4
CPU_SYSCLK
CPU_DDRCLK
CPU_RTCCLK
SH19 19_QorIQ_1015_Power_On_Monitor
HRESET_REQ_B
CPU_TIMER_WD
PWR_SEQ_RESET_On
WD_CLK
WD_ON_OFF
DIS_WD
DRIVE_HIGH
nPORESET
SH20 20_QorIQ_1015_CLOCKS
CPU_SYSCLK
CPU_DDRCLK
CPU_RTCCLK
PCIe_I2Cclk
PCIe_I2Cdata
SD_REF_CLK
/SD_REF_CLK
CLK25M_MAN_REFCLK
ENTU_PCIe_REFCLK_A+
ENTU_PCIe_REFCLK_A-
COMP_PCIe_REFCLK+
COMP_PCIe_REFCLK-
SH12 12_QorIQ_1015_TSEC_1588
TSEC2_TDP_SGMII
TSEC2_TDN_SGMII
TSEC2_RDP_SGMII
TSEC2_RDN_SGMII
NTU_PCIe_RDN
NTU_PCIe_RDP
NTU_PCIe_TDN
NTU_PCIe_TDP
COMP_PCIe_TDN
COMP_PCIe_TDP
COMP_PCIe_RDN
COMP_PCIe_RDP
TSEC1_RGMII_TXCLK
TSEC1_RGMII_TXD[0-3]
TSEC1_RGMII_TXEN
TSEC1_RGMII_RXD[0-3]
TSEC1_RGMII_RXDV
TSEC1_RGMII_RXCLK
SD_REF_CLK
/SD_REF_CLK
MDIO_MNG_SW
MDIO_GBE_PIGGY
MDC_MNG_SW
MDC_GBE_PIGGY
SMI_MNG_SW
SMI_GBE_PIGGY
SH15 15_QorIQ_1015_POWER
SH24 GBE_For_Management
TSEC1_RGMII_TXCLK
TSEC1_RGMII_TXD[0-3]
TSEC1_RGMII_TXEN
TSEC1_RGMII_RXD[0-3]
TSEC1_RGMII_RXDV
TSEC1_RGMII_RXCLK
MNG_SERDES_TXP
MNG_SERDES_TXN
MNG_SERDES_RXP
MNG_SERDES_RXN
CLK25M_MAN_REFCLK
MAN_SW_INT
MDC_MAN_SW
MDIO_MAN_SW
nPORESET
SH13 13_QorIQ_1015_USB
RST_USB
USB_5V
USB_DM
USB_DP
SH14 14_QorIQ_1015_DDR3_SDRAM
nPORESET
Designer : Zeev_L, Shimon_A, Ran_Z
Project Name = ETX-2I/10G 1/2 19"
RAD data communications
Title SYSTEM ROOT
Size C
Design Name : ETX-2I-10G-LC.REV0.2I
Rev 0.0
Date: Friday, June 17, 2016
Sheet 2 of 46

General-Purpose POR Configuration Register (GPPORCR)
Software can use this value to inform the operating system about initial system configuration. Typical interpretations include circuit board type, board ID number, or a list of available peripherals.

It has a weak internal pull-up

Default 0xFFFF

VDD_3.3V

R1066 4.7K N.C. LAD0
R1094 4.7K N.C. LAD1
R1095 4.7K N.C. LAD2
R1096 4.7K N.C. LAD3
R1097 4.7K N.C. LAD4
R1098 4.7K N.C. LAD5
R1134 4.7K N.C. LAD6
R1135 4.7K N.C. LAD7
R334 4.7K N.C.
R335 4.7K N.C.
R336 4.7K N.C.
R337 4.7K N.C.
R338 4.7K N.C.
R365 4.7K N.C.
R366 4.7K N.C.
R367 4.7K N.C.

operation for future to control functionality

VDD_3.3V

cfg_eng_use[0:2]

R305 4.7K N.C.
R304 4.7K N.C.
R303 4.7K N.C.
R310 4.7K
R309 4.7K
R308 4.7K
LA20
LA21
LA22

The value of LA28, during reset is used to set the System Speed settings.

It has a weak internal pull-up

Default "1"

VDD_3.3V

LA28 cfg_sys_speed

R349 4.7K N.C.

LA28 cfg_sys_speed	Meaning
1	SYSCLK frequency is at or above 66 MHz.

The value of LA23, during reset is used to set the Platform Speed settings.

It has a weak internal pull-up

Default "1"

CCB clock platform 266.664Mhz

VDD_3.3V

LA23 cfg_plat_speed

R302 4.7K N.C.
R307 4.7K

LA23 cfg_plat_speed	Meaning
0	Platform clock frequency is above 267 MHz and below 300 MHz.
1	Platform clock frequency is at or above 300 MHz.

It has a weak internal pull-up

Default "11"

VDD_3.3V VDD_3.3V

LGPL3 cfg_boot_seq0
LGPL5 cfg_boot_seq1

R406 4.7K N.C.
R353 4.7K N.C.

The value of , LGPL3 and LGPL5 during Power on reset sets the Boot Sequencer Configuration.

LGPL3 cfg_boot_seq[0]	LGPL5 cfg_boot_seq[1]	Meaning
1	1	Boot sequencer is disabled. No I2C ROM is accessed (default)

It has a weak internal pull-up

Default "111"

VDD_3.3V VDD_3.3V VDD_3.3V

LWE1_B cfg_host_agt0
LA18 cfg_host_agt1
LA19 cfg_host_agt2

R405 4.7K N.C.
R330 4.7K N.C.
R329 4.7K N.C.

The value of LWE1, LA18 and LA19 during Power on reset sets the Host/Agent Configuration for PCI Express/serial RapidIO.

LWE1 cfg_host_agt[0]	LA18 cfg_host_agt[1]	LA19 cfg_host_agt[2]	Meaning
1	1	1	Device acts as the host processor/root complex for all PCI Express interfaces (default).

The value of LA24, during reset is used to set the Core 0 Speed settings.

It has a weak internal pull-up

Default "1"

core speed 533.328M

VDD_3.3V

LA24 cfg_core0_speed

R301 4.7K N.C.
R306 4.7K N.C.

LA24 cfg_core0_speed	Meaning
0	Core 0 clock frequency is less than 450 MHz.
1	Core 0 clock frequency is greater than or equal to 450 MHz

Default "11"

VDD_3.3V

LA27 cfg_cpu0_boot
LA16 cfg_cpu1_boot

R1142 4.7K
R331 4.7K

The value of , LA27 and LA16 during Power on reset sets the CPU Boot Configuration.

LA27 cfg_cpu0_boot	LA16 cfg_cpu1_boot	Meaning
1	0	e500 core 0 is allowed to boot without waiting for configuration by an external master, while e500 core 1 is prevented from booting until configured by an external master or the other core

The value of LA25, during reset is used to set the Core 1 Speed settings.

It has a weak internal pull-up

Default "1"

VDD_3.3V

LA25 cfg_core1_speed

R279 4.7K N.C.
R280 4.7K N.C.

LA25 cfg_core1_speed	Meaning
0	Core 1 clock frequency is less than 450 MHz.
1	Core 1 clock frequency is greater than or equal to 450 MHz

The value of LA26 during reset is used to set the DDR Controller Speed settings.

It has a weak internal pull-up

Default "1"

666.66 MHz

VDD_3.3V

LA26 cfg_ddr_speed

R1144 4.7K N.C.
R1143 4.7K N.C.

LA26 cfg_ddr_speed	Meaning
1	DDR controller clock frequency is greater than or equal to 450 MHz.

The value of LWE0, UART_SOUT1 and READY_P1 are latch during Power on reset and sets the e500 core1 : CCBCLK Ratio.

No Default

VDD_3.3V

/LWE0 cfg_core1_pll0

R363 4.7K
R364 4.7K N.C.

LWE0 cfg_core1_pll[0]	UART_SOUT1 cfg_core1_pll[1]	READY_P1 cfg_core1_pll[2]	e500 core1:CCBCLK Ratio
1	0	0	2:1 533.328M : 266.664M

The value of LA[29:31] are latch during Power on reset and sets the CCB clock to SYSCLK PLL ratio.

VDD_3.3V VDD_3.3V VDD_3.3V

R347 4.7K N.C.
R348 4.7K N.C.
R1145 4.7K N.C.
R388 4.7K
R389 4.7K
R1146 4.7K

cfg_sys_pll0 LA29
cfg_sys_pll1 LA30
cfg_sys_pll2 LA31

LA29 cfg_sys_pll[0]	LA30 cfg_sys_pll[1]	LA31 cfg_sys_pll[2]	CCB Clock : SYSCLK Ratio
0	0	0	4:1 266.666M : 66.666M
0	0	1	5:1 333.33M : 66.666M

The value of LBCTL, LALE and LGPL2 are latch during Power on reset and sets the e500 core0 : CCBCLK Ratio.

VDD_3.3V VDD_3.3V VDD_3.3V

R438 4.7K
R355 4.7K N.C.
R354 4.7K N.C.
R474 4.7K N.C.
R397 4.7K
R394 4.7K

cfg_core0_pll0 LBCTL
cfg_core0_pll1 ALE
cfg_core0_pll2 LGPL2 nOE

LBCTL cfg_core0_pll[0]	LALE cfg_core0_pll[1]	LGPL2 cfg_core0_pll[2]	e500 core0 : CCBCLK Ratio
1	0	0	2:1 533.328M : 266.664M

BOM Change - Not used CS2, CS4, CS5, CS6 and Pull up also NC

CS0 - 8/16/32/64M/128M BYTE Flash - Boot & App.
CS1 - COMPANION (Ext. TA)
CS2 - Not used (NTU Cyclone-V (Ext. TA))
CS3 - Not used (COMPANION (Int. TA))
CS4 - Not used (SYNC-E (Ext.TA))
CS5 - Not used (Ext TA - CPLD)
CS6 - Not used (Int . TA - CPLD.)

U114F

LocalBus Interface (6 of 11)

LAD[0-15] LAD0 MSB B10 LAD00/USB2_D07
LAD1 C16 LAD01/USB2_D06
LAD2 A10 LAD02/USB2_D05
LAD3 A14 LAD03/USB2_D04
LAD4 C13 LAD04/USB2_D03
LAD5 C10 LAD05/USB2_D02
LAD6 A9 LAD06/USB2_D01
LAD7 A13 LAD07/USB2_D00
LAD8 E18 LAD08/USB2_NXT
LAD9 B3 LAD09/USB2_DIR
LAD10 D9 LAD10/USB2_STP
LAD11 E8 LAD11/USB2_PWRFULT
LAD12 D11 LAD12/USB2_CLK
LAD13 A3 LAD13/USB2_PCTL0
LAD14 E9 LAD14/USB2_PCTL1
LAD15 LSB A8 LAD15

R1141 4.7K
R356 4.7K
LDP0 A12 LDP0
LDP1 B11 LDP1

LA[16-31] cfg_cpu1_boot LA16 B16 LA16
cfg_host_agt1 LA17 B17 LA17
cfg_host_agt2 LA18 A15 LA18
cfg_eng_use0 LA19 A20 LA19
cfg_eng_use1 LA20 A5 LA20
cfg_eng_use2 LA21 C15 LA21
cfg_plat_speed LA22 B4 LA22
cfg_core0_speed LA23 B19 LA23
cfg_core1_speed LA24 D18 LA24
cfg_ddr_speed LA25 A17 LA25
cfg_cpu0_boot LA26 A18 LA26
cfg_sys_speed LA27 A16 LA27
cfg_sys_pll0 LA28 C18 LA28
cfg_sys_pll1 LA29 E19 LA29
cfg_sys_pll2 LA30 C19 LA30
LA31 LSB A19 LA31

P1015NXE5DFB

LCS0_B D15 nCS0_B R391 22 nCS0
LCS1_B C6 nCS1_B R402 22 nCS1_GPIO
LCS2_B D14 nCS2_B R392 22
LCS3_B D17 nCS3_B R390 22
LCS4_B D6 nCS4_B R401 22
LCS5_B B8 nCS5_B R398 22 spare nCS5_GP_FPGA
LCS6_B B7 nCS6_B R399 22 nCS6_HSI
LCS7_B C9 nCS7_B R396 22

LWE0_B B5 LWE0_B R403 33 cfg_core1_pll0 nWE0
LWE1_B C5 LWE1_B R404 33 cfg_host_agt0 nWE1 nWE[0-1]

LBCTL B13 LBCTL cfg_core0_pll0 Low read High Write
LALE E10 ALE R395 22 cfg_core0_pll1 LALE

LGPL0 A4
LGPL1 D8
LGPL2 B14 LGPL2 R393 22 cfg_core0_pll2 nOE
LGPL3 D5 LGPL3 /LGTA cfg_boot_seq0
LGPL4 C7 LGPL4 4.7K R360
LGPL5 C12 LGPL5 cfg_boot_seq1

LCLK0 A7 LCLK0 R400 N.C. 14.3 CPU_CLK_GP_FPGA
LCLK1 A6
NC80 E11
NC81 A11

BOM Change - Not used CPU_CLK at GP

VDD_3.3V

R351 4.7K
R362 4.7K
R360 4.7K
R361 4.7K
R358 4.7K
R359 4.7K
R357 4.7K

VDD_3.3V

C1038 0.1uF
R407 22 R_nW
U52 NC7SZ04
LALE

VDD_3.3V

R360 4.7K nOE

CPU_CLK_GP_FPGA

Designer : Zeev_L, Shimon_A, Ran_Z

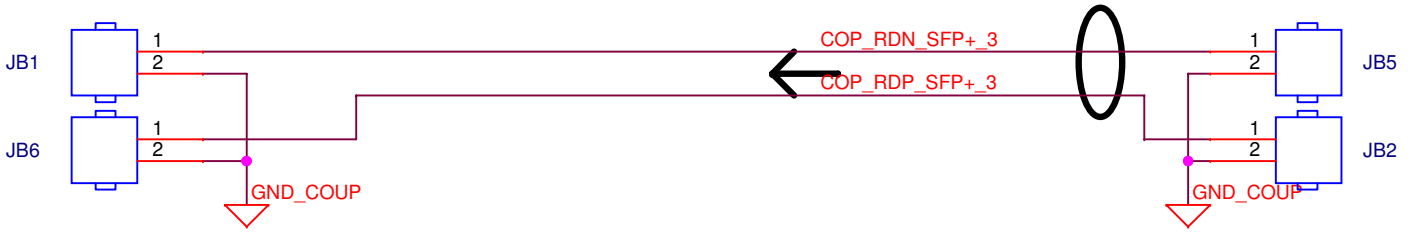
RAD data communications

Title: 10_QorIQ_1015_Local_Bus

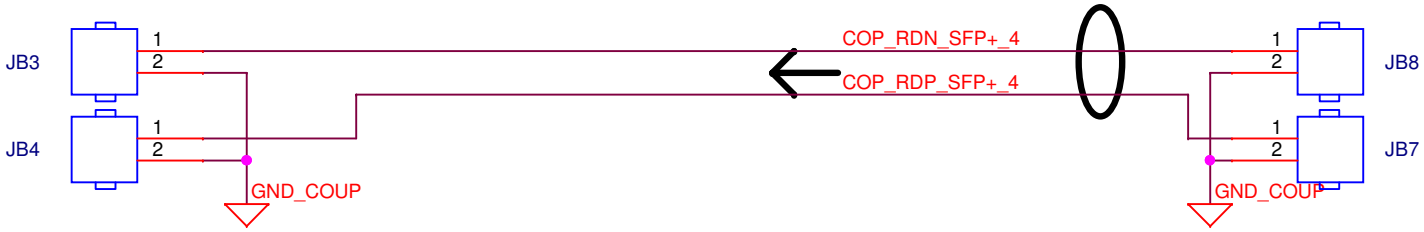
Size C | Design Name : ETX-2I-10G-LC.REV0.2I | Rev 0.0

Date: Friday, June 17, 2016 | Sheet 3 of 46

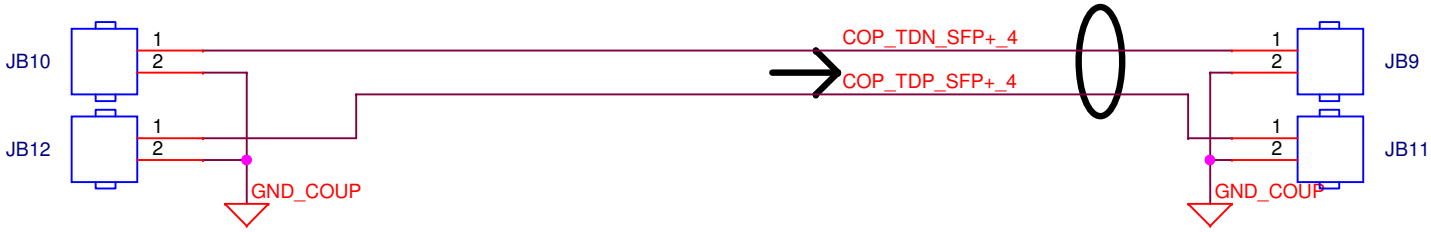
Toward ENTU <<-- -->> Toward SFP



SFP 3

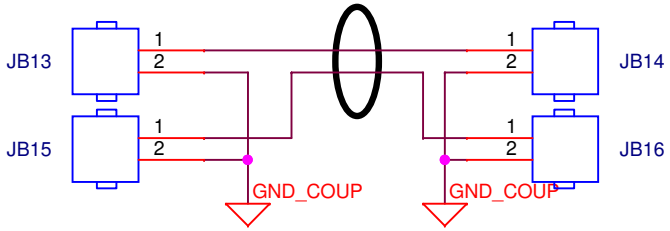


SFP 4



SFP 4

For Calibration



Designer : Zeev_L, Shimon_A, Ran_Z Project Name = ETX-2I/10G 1/2 19"		RAD data communications
Title: Coupon circuit		
Size: A	Design Name : ETX-2I-10G-LC.REV0.2I	Rev: 0.0
Date: Friday, June 17, 2016	Sheet 4 of 46	

CVDD = 3.3V

BVDD = 3.3V

LVDD = 2.5V

LVDD = 3.3V

operation for future to control functionality.

BOM change, add R463 For new BOOT

Debug information

P1015 SPI Interface

N.U.

The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is 2 × tCCB, and minimum clock low time is 2 × tCCB. There is no minimum RTC frequency; RTC may be grounded if not needed.

REV 0.2 Change SDHC CLK move to pull down instead of pull up

Change - added option for pull down as per Leonid K request

Change Logic (oposite logic)

Default (SW off) WD=ON , Debug=OFF

W.D On: '1' W.D Off: '0'

Debug Off:'1' Debug On: '0'

Change - Remove Debug GP, GBE FPGA, add resistors for future monitoring

Change - Remove Debug Port

CPU Device Assambled

The value of MSRCID0, during reset is used to set the eLBC ECC Enable settings.

MSRCID0 cfg_elbc_ecc	Meaning
0	eLBC ECC checking is disable.

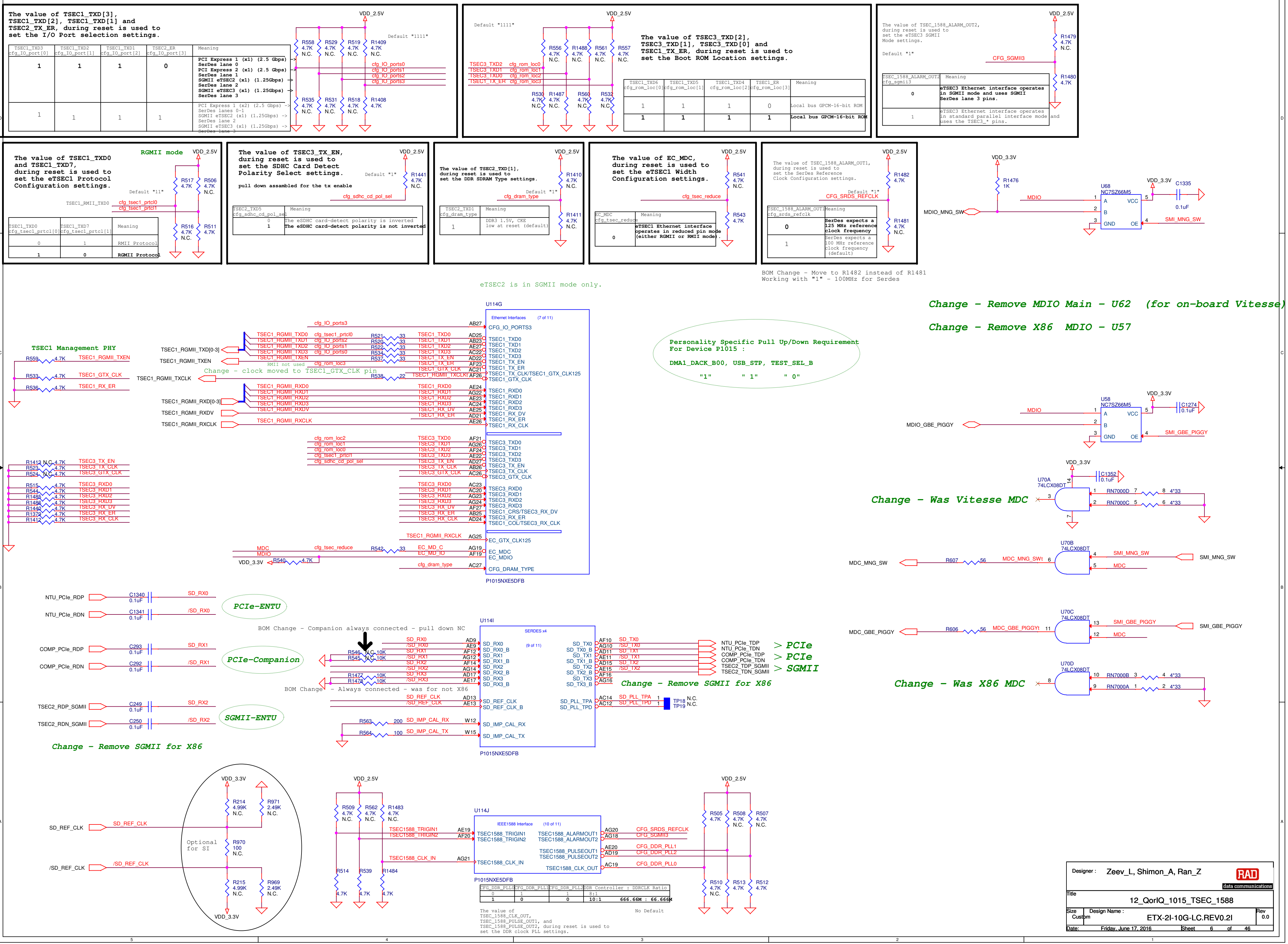
UART0_RTS cfg_tsec3_prtcl0	UART1_RTS cfg_tsec3_prtcl1	Meaning
0	0	Not configured to operate in SGMII mode Reserved
0	1	The eTSEC3 controller operates using the RMII protocol if not configured to operate in SGMII mode

The value of LWE0, UART_SOUT1 and READY_P1 during Power on reset sets the e500 corel : CCBCLK Ratio.

LWE0 cfg_core1_pll1[0]	UART_SOUT1 cfg_core1_pll1[1]	READY_P1 cfg_core1_pll1[2]	e500 core1 : CCBCLK Ratio
1	0	0	2:1 533.328M : 266.664M

Device	DMA1_DACK_B00	USB_STP	TEST_SEL_B
P1011 P1015	1	1	0
P1020	1	1	1
P2020 P1024	0	1	1

Designer :	Zeev_L, Shimon_A, Ran_Z
Title	11_QorIQ_1015_System_Logic
Size	Custom
Design Name :	ETX-2I-10G-LC.REV0.2I
Rev	0.0
Date:	Friday, June 17, 2016
Sheet	5 of 46



The value of TSEC1_TXD[3], TSEC1_TXD[2], TSEC1_TXD[1] and TSEC2_TX_ER, during reset is used to set the I/O Port selection settings.

Default "1111"

TSEC1_TXD3 cfg_IO_port[0]	TSEC1_TXD2 cfg_IO_port[1]	TSEC1_TXD1 cfg_IO_port[2]	TSEC2_ER cfg_IO_port[3]	Meaning
1	1	1	0	PCI Express 1 (x1) (2.5 Gbps) -> SerDes lane 0; PCI Express 2 (x1) (2.5 Gbps) -> SerDes lane 1; SGMII eTSEC2 (x1) (1.25Gbps) -> SerDes lane 2; SGMII eTSEC3 (x1) (1.25Gbps) -> SerDes lane 3
1	1	1	1	PCI Express 1 (x2) (2.5 Gbps) -> SerDes lanes 0-1; SGMII eTSEC2 (x1) (1.25Gbps) -> SerDes lane 2; SGMII eTSEC3 (x1) (1.25Gbps) -> SerDes lane 3

The value of TSEC3_TXD[2], TSEC3_TXD[1], TSEC3_TXD[0] and TSEC1_TX_ER, during reset is used to set the Boot ROM Location settings.

Default "1111"

TSEC1_TXD6 cfg_rom_loc[0]	TSEC1_TXD5 cfg_rom_loc[1]	TSEC1_TXD4 cfg_rom_loc[2]	TSEC1_ER cfg_rom_loc[3]	Meaning
1	1	1	0	Local bus GPCM-16-bit ROM
1	1	1	1	Local bus GPCM-16-bit ROM

The value of TSEC_1588_ALARM_OUT2, during reset is used to set the eTSEC3 SGMII Mode settings.

Default "1"

TSEC_1588_ALARM_OUT2 cfg_sgmii3	Meaning
0	eTSEC3 Ethernet interface operates in SGMII mode and uses SGMII SerDes lane 3 pins.
1	eTSEC3 Ethernet interface operates in standard parallel interface mode and uses the TSEC3_* pins.

The value of TSEC1_TXD0 and TSEC1_TXD7, during reset is used to set the eTSEC1 Protocol Configuration settings.

Default "11"

TSEC1_TXD0 cfg_tsec1_prtcl[0]	TSEC1_TXD7 cfg_tsec1_prtcl[1]	Meaning
0	1	RMII Protocol
1	0	RGMII Protocol

The value of TSEC3_TX_EN, during reset is used to set the SDHC Card Detect Polarity Select settings.

Default "1"

pull down assambled for the tx enable

TSEC2_TXD5 cfg_sdhc_cd_pol_sel	Meaning
0	The eSDHC card-detect polarity is inverted
1	The eSDHC card-detect polarity is not inverted

The value of TSEC2_TXD[1], during reset is used to set the DDR SDRAM Type settings.

Default "1"

TSEC2_TXD1 cfg_dram_type	Meaning
1	DDR3 1.5V, CKE low at reset (default)

The value of EC_MDC, during reset is used to set the eTSEC1 Width Configuration settings.

EC_MDC cfg_tsec_reduce	Meaning
0	eTSEC1 interface operates in reduced pin mode (either RGMII or RMII mode).

The value of TSEC_1588_ALARM_OUT1, during reset is used to set the SerDes Reference Clock Configuration settings.

Default "1"

TSEC_1588_ALARM_OUT1 cfg_srds_refclk	Meaning
0	SerDes expects a 125 MHz reference clock frequency
1	SerDes expects a 100 MHz reference clock frequency (default)

Personality Specific Pull Up/Down Requirement For Device P1015 :

DMA1_DACK_B00, USB_STP, TEST_SEL_B

"1" " 1" " 0"

CFG_DDR_PLL0	CFG_DDR_PLL1	CFG_DDR_PLL2	DDR Controller : DDRCLK Ratio
0	1	1	8:1
1	0	0	10:1 666.66M : 66.666M

The value of TSEC1588_CLK_OUT, TSEC1588_PULSE_OUT1, and TSEC1588_PULSE_OUT2, during reset is used to set the DDR clock PLL settings.

No Default

Designer :	Zeev_L, Shimon_A, Ran_Z
Title	12_QorIQ_1015_TSEC_1588
Size: Custom	Design Name : ETX-2I-10G-LC.REV0.2I
Rev	0.0
Date:	Friday, June 17, 2016
Sheet	6 of 46

RAD data communications

Personality Specific Pull Up/Down Requirement
For Device P1015 :

DMA1_DACK_B00, USB_STP, TEST_SEL_B

"1" " 1" " 0"

USB Interface

U114H

USB Interface

(8 of 11)

USB_D0 E22
USB_D1 A22
USB_D2 A23
USB_D3 D23
USB_D4 B22
USB_D5 A25
USB_D6 A24
USB_D7 E23
USB_DIR C22
USB_STP C23
USB_NXT B23
USB_CLK A26
PWRFAUL B25
USB_PWRFAULT

P1015NXE5DFB

VDD_3.3V
R660 4.7K

U78

USB3300-EZK

DATA0 24
DATA1 23
DATA2 22
DATA3 21
DATA4 20
DATA5 19
DATA6 18
DATA7 17
DIR 12
STP 13
NXT 11
CLKOUT 14
RESET 9
CPEN 3
GND 1
GND 2
GND FLAG 33
VDD1.8 15
VDD1.8 26
VDDA1.8 29
VDD3.3 6
VDD3.3 16
VDD3.3 25
VDD3.3 30
REG_EN 31
XI 28
XO 27
DM 8
DP 7
ID 5
VBUS 4
EXTVBUS 10
RBIAS 32

USB_D0 … USB_D7
USB_DIR
USB_STP
USB_NXT
USB_CLK_B
USB_CLK_Bt
R659 22
RST_USB
USB_DM
USB_DP
VBUS
EXTVBUS

VDD18
C1401 0.1uF
C1393 4.7uF

VDD18A
C1402 0.1uF
C1405 4.7uF

VDD_3.3V
C1394 0.1uF
C1400 10nF
C1403 1nF
C1399 0.1uF

C1404 0.1uF
R658 1M
C351 33pF
C338 33pF
Y9 24MHZ
XTAL_IN
XTAL_OUT

R639 4.7K
C1392 0.1uF
USB_CLK
39.2
R640
USB_CLKt
U75 NC7SZ125
0 N.C. R7096

Bypass option

Disconnect for direct enable without SW

R7095 0

R685 12.1K
R686 820

R1533 4.7K
C1411 0.1uF
U79 NC7SZ04
PWRFAUL

R7097 4.7K N.C.

Connect for direct enable without SW

U126 MIC2075-1YM

EN 1
FLG 2
GND 3
N.C. 4
OUT 8
IN 7
OUT 6
N.C. 5
CPEN_IN
USB_FLG

V5V
V_USB
TP24 N.C.
L11
USB_5V
C1410 0.1uF
C1435 0.1uF
C379 22uF
C377 100uF N.C.
C378 100uF
C389 22uF
C380 10nF
C388 0.1uF
C387 47nF

Capacitors in overlap.

12V_Vin
C1395 Cin 10uF C1
C1406 0.1uF
R1529 100K R3
Enable
EN=high to enable the module.
Float EN pin or connect it to gnd
will disable the converter.

4.5V-to-24V

3mm x 5mm x 1.6mm
Total solution size 6.7mmx6.3mm

U124 MPM3620GQV

IN 16
EN 17
AAM 18
PGND 12
PGND 13
PGND 14
AGND 3
N.C. 10
VCC 2
BST 11
SW 6
SW 5
SW 4
OUT 9
OUT 8
OUT 7
FB 1
N.C. 15

TP23 N.C. VCC_Test
VCC_INT

Bootstrap. Bootstrap capacitor is integrated internally. External connection is not needed.

Switch Output. Large copper plane is recommended on pin 4, 5 and 6 for better heat sink.

AAM
External AAM pin for Power-Save Mode Programming
R1528 63.4K

AGND

pins 10,15,19,20
DO NOT CONNECT.
Pin must be left floating.

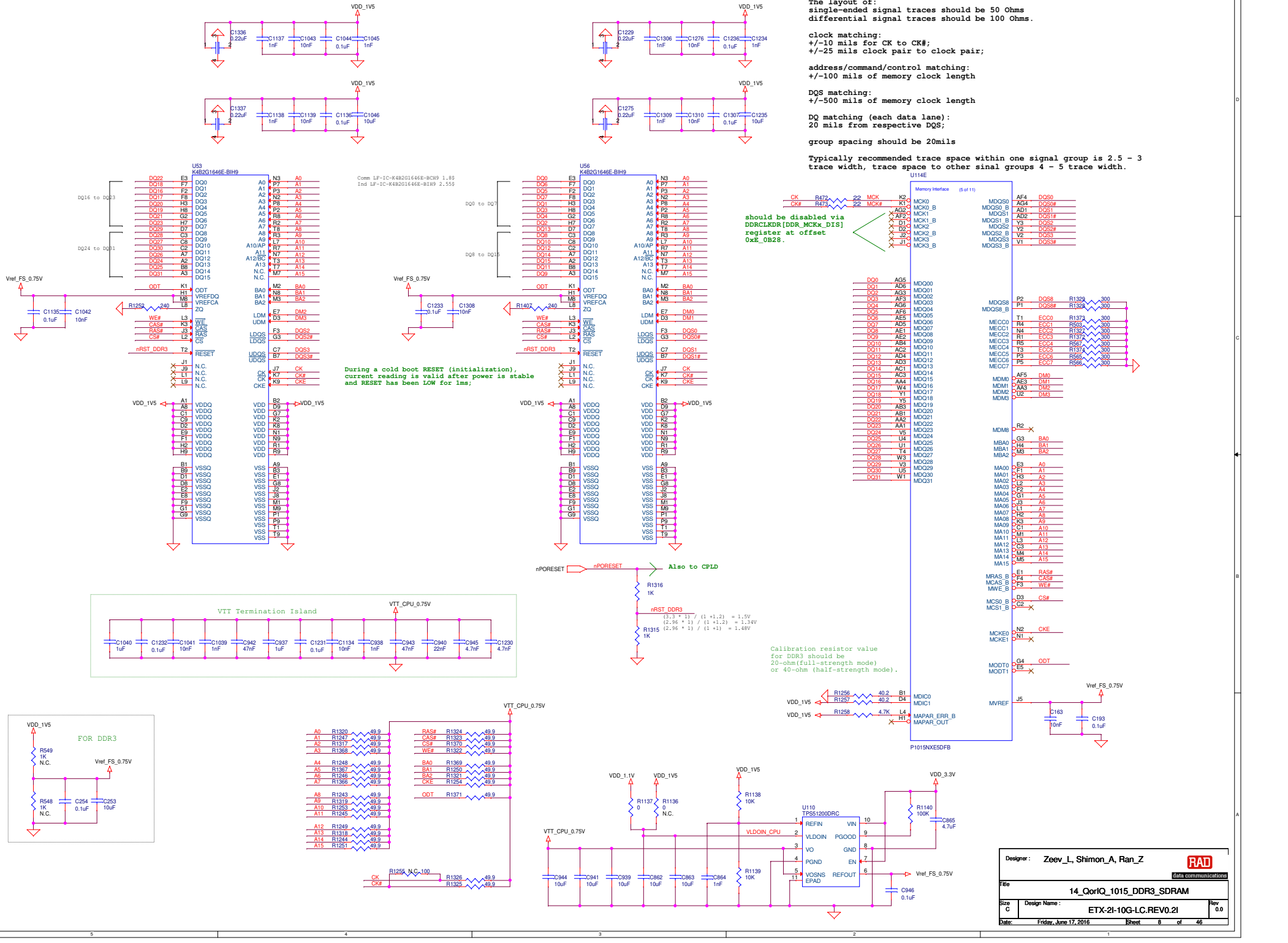
Analog Ground

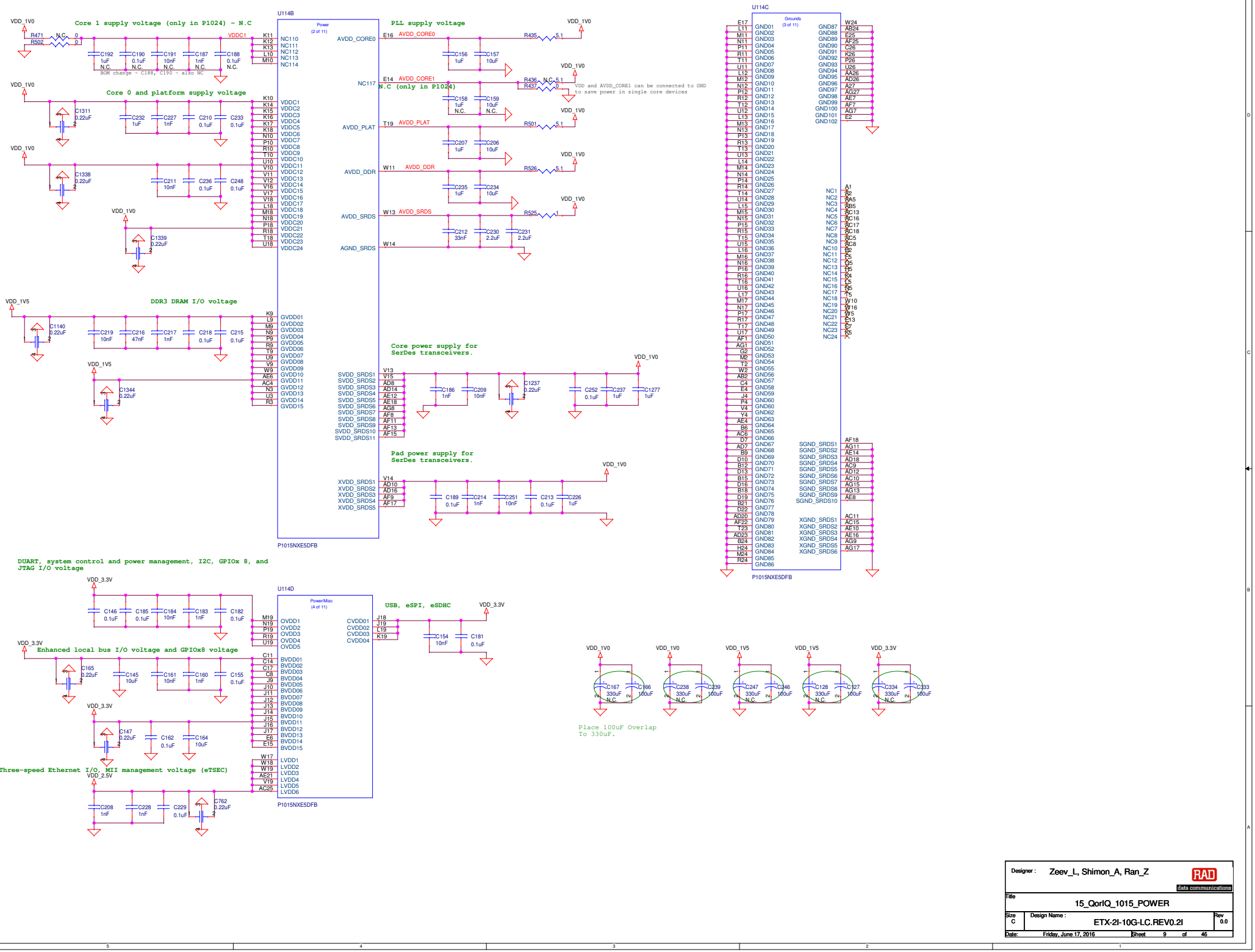
R1 R1527 158K
C1412 Cout 22uF C2
R2 R1534 29.8K
FB
resistor divider close to FB

R2= R1 / [Vout/0.798 - 1]
Vout = 0.798 * [(R1/R2) +1]

R1=158k
R2=29.8k
Vout = 0.798 * (158/29.8 +1] = 5.029v

Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications
Title	13_QorIQ_1015_USB	
Size: Custom	Design Name : ETX-2I-10G-LC.REV0.2I	Rev 0.0
Date: Friday, June 17, 2016	Sheet 7 of 46	


The layout of:
single-ended signal traces should be 50 Ohms
differential signal traces should be 100 Ohms.
clock matching:
+/-10 mils for CK to CK#;
+/-25 mils clock pair to clock pair;
address/command/control matching:
+/-100 mils of memory clock length
DQS matching:
+/-500 mils of memory clock length
DQ matching (each data lane):
20 mils from respective DQS;
group spacing should be 20mils
Typically recommended trace space within one signal group is 2.5 - 3
trace width, trace space to other sinal groups 4 - 5 trace width.
U53
K4B2G1646E-BIH9
U56
K4B2G1646E-BIH9
U114E
Memory Interface
(5 of 11)
P1015NXE5DFB
should be disabled via
DDRCLKDR[DDR_MCKx_DIS]
register at offset
0xE_0B28.
During a cold boot RESET (initialization),
current reading is valid after power is stable
and RESET has been LOW for 1ms;
Also to CPLD
VTT Termination Island
VTT_CPU_0.75V
FOR DDR3
Calibration resistor value
for DDR3 should be
20-ohm(full-strength mode)
or 40-ohm (half-strength mode).
U110
TPS51200DRC
Designer : Zeev_L, Shimon_A, Ran_Z
RAD
data communications
Title
14_QorIQ_1015_DDR3_SDRAM
Size C
Design Name : ETX-2I-10G-LC.REV0.2I
Rev 0.0
Date: Friday, June 17, 2016
Sheet 8 of 46


Core 1 supply voltage (only in P1024) - N.C
Core 0 and platform supply voltage
DDR3 DRAM I/O voltage
PLL supply voltage
Core power supply for SerDes transceivers.
Pad power supply for SerDes transceivers.
DUART, system control and power management, I2C, GPIOx 8, and JTAG I/O voltage
Enhanced local bus I/O voltage and GPIOx8 voltage
Three-speed Ethernet I/O, MII management voltage (eTSEC)
USB, eSPI, eSDHC
VDD and AVDD_CORE1 can be connected to GND to save power in single core devices
Place 100uF Overlap To 330uF.
U114B
U114C
U114D
P1015NXE5DFB
Designer : Zeev_L, Shimon_A, Ran_Z
Title
15_QorIQ_1015_POWER
Design Name : ETX-2I-10G-LC.REV0.2I
Size C
Rev 0.0
Date: Friday, June 17, 2016
Sheet 9 of 46

Connector for COMMUNICATION

BOM - Always connected
No special BOM for comm/alra, piggy

HOLE3.2
MH18
N.C.
C7022 0.1uF N.C.
C7020 10nF N.C.
C7021 1nF N.C.

J19
20PIN(2X10)
FPGA_JTAG_EN
USB_DP
USB_DM
Change removed TERMINAL_TXD
Change removed TERMINAL_RXD
COM_I2Cdata
COM_EXIST
COM_I2Cclk
VDD_3.3V
ALM_INPUT1
ALM_INPUT2
ALM_INPUT3
ALM_INPUT4
ALM_INPUT[1-4]
ALM_OUTPUT
Magor_ALM
12V_Vin
Was RST_PANEL
USB_5V
VDD_3.3V

ALM_INPUT[1-4]

VDD_3.3V
4.7K R1562 COM_EXIST
4.7K N.C. R1622 RST_PANEL

HOLE3.2
MH12
N.C.

BOM Change - Remove RST_Panel pull up (another pull up at CPU scheme)

Place close to Communication/ALM Piggy

Place close to Panel (RS232 connector)

Change - Added, check

U7000
MAX3221ECAE
C1+ C1- C2+ C2- VCC V+ V- T_IN R_OUT T_OUT R_IN EN FORCEOFF FORCEON GND INVALID
C7005 0.1uF
C7007 0.1uF
C7000 0.1uF
C7001 0.1uF
C7002 10nF
C7003 0.1uF
C7004 10nF
C7006 0.1uF
C7008 0.1uF
3V3_Terminal
L7000 220
L7001 600OHM/AC
L7002 600OHM/AC
L7003 600OHM/AC
C7010 100pF
C7011 100pF
C7012 100pF
C7013 100pF
TERMINAL_TXD
TERMINAL_RXD
COM_TXD
COM_RXD
R7048 22
RS232_TXD
RS232_RXD
RS232_TXD_
RS232_RXD_
J7000
5 PIN
M1
M2

RS232 Control Port

Change - Added, check

RST_PANEL
RST_PANEL
C7009 0.1uF
SW7000
TP11-H9-AV-B
M1

Factory default
Low active

JTAG_1G_INTF_TDO
TOD_TDI
VDD_3.3V
EXT_CLK_EXIST
R1545 4.7K
C7049 0.1uF
U7003
NC7SZ126
R719 0 N.C.
JTDO_EXT_CLK
R718 0 TOD_TDO

Change - Option for automatically chain bypass when no Timing piggy ('1')

Connector for EEC

J18
40PIN(2X20)
CLK_1PPS_RJ_IN
CLK_1PPS_RJ_OUT
TXDIS_1PPS_RJ
EXT_CLK_BNC_IN
EXT_CLK_BNC_OUT
EXT_CLK_RJ_IN
EXT_CLK_RJ_OUT
SPI_CLK4
TOD_SPI_CS
nRST_GPS
EXT_CLK_I2Cdata
EXT_CLK_I2Cclk
JTCK_EXT_CLK
R1561 CLK_1PPS_RJ_OUTb
R739 EXT_CLK_BNC_OUTb
R1559 EXT_CLK_RJ_OUTb
CLK_1PPS_BNC_IN
CLK_1PPS_BNC_OUTb
R1560 CLK_1PPS_BNC_OUT
TOD_TXD
TOD_RXD
EXT_CLK_EXIST
RCL
E1_SYNC_LED
nRST_FR
E1_nINT
SPI_MISO
SPI_MOSI4
FPGA_JTAG_EN
GPS_EXTCLK
TOD_TDO
JTMS_EXT_CLK
nTRST
TOD_TDI

Place close to EEC/Timing Piggy

HOLE3.2
MH10
VDD_3.3V
N.C.

VDD_3.3V
C382 10uF
C368 1uF
C381 0.1uF
C367 10nF

Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications	
Title	16_UART_and_TOD		
Size B	Design Name : ETX-2I-10G-LC.REV0.2I		Rev 0.0
Date: Friday, June 17, 2016	Sheet 10 of 46		

Change - 2md, 3rd mux removed

Change - BP PS removed

Change - Moved power Monitor

Change - X86 Interface removed

Change - FAN Controller 2 removed

PIGGY BACK P13-P16

Timing Piggy

Jitter Attenuator PLL

PCIe CLOCK GENERATOR

PLL clock generator

Fan controler 1

Comm / Alarm Piggy

Change - Added Power Sequencer and Monitor

Stencil ready for R7062, R7063 option

Bypass normally

Option buffer in case of bad SI

Device address is 1110000

Don't bypass normally

Connect buffer to improve SI

Rev 0.2 - Change stencil to be ready for bypass U127 option

Rev 0.1 - Stencil ready for U127 option

Option to drive from 2nd I2C CPU BUS

Rev 0.2 - Change SCL/SDA of SFP PU to VDD_SFP_3.3V (was VDD_3.3V)

Device address is 1110010

Designer :	Zeev_L, Shimon_A, Ran_Z
Title	17_I2C_and_Thermometer
Size	C
Design Name :	ETX-2I-10G-LC.REV0.2I
Rev	0.0
Date:	Friday, June 17, 2016
Sheet	11 of 46

BOM - Change to non bus hold device IC-74LCX16244TPV
Was IC-74LVT16244BDGG

IC-74LVT16244BDGG 0.18$ IC, SMD,!MS!,TSSOP-48,(I),16BIT BUFFER/LINE DRIVER
IC-74LVT16244TPV 0.1570 IC, SMD,!MS!,TSSOP-48,(I),16BIT BUFFER/LINE DRIVER

U107 74LCX16244
LA[16-31]
Buf_Addr0 LSB
Buf_Addr15
VDD_3.3V
C124 1uF
C119 47nF
C118 0.1uF
C123 0.1uF
R_nW

U109
LAD[0-15]
Buf_Addr16
Buf_Addr31
Addr_LE
74LVT16373
C861 1uF
C129 47nF
C136 0.1uF
C817 0.1uF

C130 1uF
C860 47nF
C816 0.1uF
C137 0.1uF

U4A 74LVT16245
U4B 74LVT16245
Buf_Data0 MSB
Buf_Data15 LSB
direction:
"1" A --> B
"0" B --> A

C194 0.1uF
C168 1nF
C169 0.1uF

U113
PC28F00BM29EWH
Buf_Addr1
Buf_Addr27
Buf_Data15 LSB
Buf_Data0 MSB
R1239 0_A23
R1237 0_A24
R1314 0_A25

Flash WRITE PROTECT
WP# low enables the lock-down mechanism.
WP# high overrides the lock-down function
enabling blocks to be erased or programmed
using software commands.

R1405 10K
VPP
FLASH_WE
FLASH_OE
nRST_FL
RY/BY 10K R1404
nBYTE_FL 10K R1238
nCS0
nPORESET

256 MBIT (16M*16), A[24:1], RAD P/N = LF-IC-PC28F256M29EWH
512 MBIT (32M*16), A[25:1], RAD P/N = LF-IC-PC28F512M29EWH
1 GBIT (64M*16), A[26:1], RAD P/N = LF-IC-PC28F00AM29EWH
2 GBIT (128M*16), A[27:1], RAD P/N = LF-IC-PC28F00BM29EWH

U82 NC7SBU3157P6
FL_LALE
LALE
DRIVE_HIGH
Addr_LE
S = "0" B0 connected to A
S = "1" B1 connected to A
R847 N.C. 0
LALE 540 mil
ADDR_LE 2588 mil
LAD15 2553 mil
LAD0 3174 mil

Split BUF_SPI_CLK from one via with same length to all pins and on same layer
BUF_SPI_CLK
BUF_SPI_MOSI

U3 74LCX16244
SPI_B_CLK1
SPI_B_CLK2
SPI_B_CLK4
SPI_B_CLK5
SPI_B_CLK7
SPI_B_CLK8
SPI_CLK1
SPI_CLK2
SPI_CLK4
SPI_CLK5
SPI_CLK7
SPI_CLK8
SPI_MOSI1
SPI_MOSI2
SPI_MOSI4
SPI_MOSI5
SPI_MOSI7
SPI_MOSI8

SPI_CLK1 for Cyclone_V ENTU
SPI_CLK2 for Cyclone_V COMP
SPI_CLK3 for X86 (removed) - Change
SPI_CLK4 for EXT. CLK(E1 framer)
SPI_CLK5 for GBE_Piggy
SPI_CLK6 for GP FPGA (removed) - Change
SPI_CLK7 for MACSEC PHYs 2,3
SPI_CLK8 for MACSEC PHY 1

C427 1uF
C429 47nF
C426 0.1uF
C428 0.1uF

BOM - Change to non bus hold device IC-74LCX16244TPV
Was IC-74LVT16244BDGG

Change - Added 2 capacitor that remove at ETX-2i due to joint assembly at PS/CS

C7014 1uF
C7015 47nF
C131 0.1uF
C859 0.1uF

U108 74LCX16244
Buf_Data15
Buf_Data0
SPR_ID7
SPR_ID0
CONF_DONE_COMP
nSTATUS_COMP
Change - was conf_done for GP GBE_Piggy X86
Change - was nStatus for GP GBE_Piggy X86

U36 NC7SV32P5
ncS1_GPIO
nOE
GPIO_OEN
C775 0.1uF

BOM - Change to non bus hold device IC-74LCX16244TPV
Was IC-74LVT16244BDGG

SPI_CLK[1-8]
SPI_MOSI[1-8]

U10B 74LCX125A
U10A 74LCX125A
U10D 74LCX125A
U10C 74LCX125A
FL_WE
DRIVE_LOW
FL_OE
nWE[0-1]
DRIVE_HIGH
nOE
FROM JTAG
Default High Exist PD
Default Low Exist PD
C467 1nF
Works during JTAG
Works normally
RN9 4*22
JWE
JOE
MWE
MOE
WE_N
OE_N
FLASH_WE
FLASH_OE

Change - Added 2 capacitor that remove at ETX-2i due to joint assembly at PS/CS

C7016 1uF
C7017 47nF
C815 0.1uF
C138 0.1uF

U45 74LCX16374
Change - Companion Reset + PCIe RST comes from external GPIO (was from GP)
RESETn_COMP
COMP_PCIe_CPU_RST
GBE_VSC8574_COMA
Change - Added Vitesse COMA (on 1G Piggy)
Change - Remove SPI_CS_1..3 of Vitesse
Change - Remove GP_FPGA_RST
Change - Remove SMI_Main (Vitesse) & SMI_X86
SMI_GBE_PIGGY
SMI_MNG_SW
DIS_WD
Change - Remove GBE/GP/X86 FPGAs nConfig

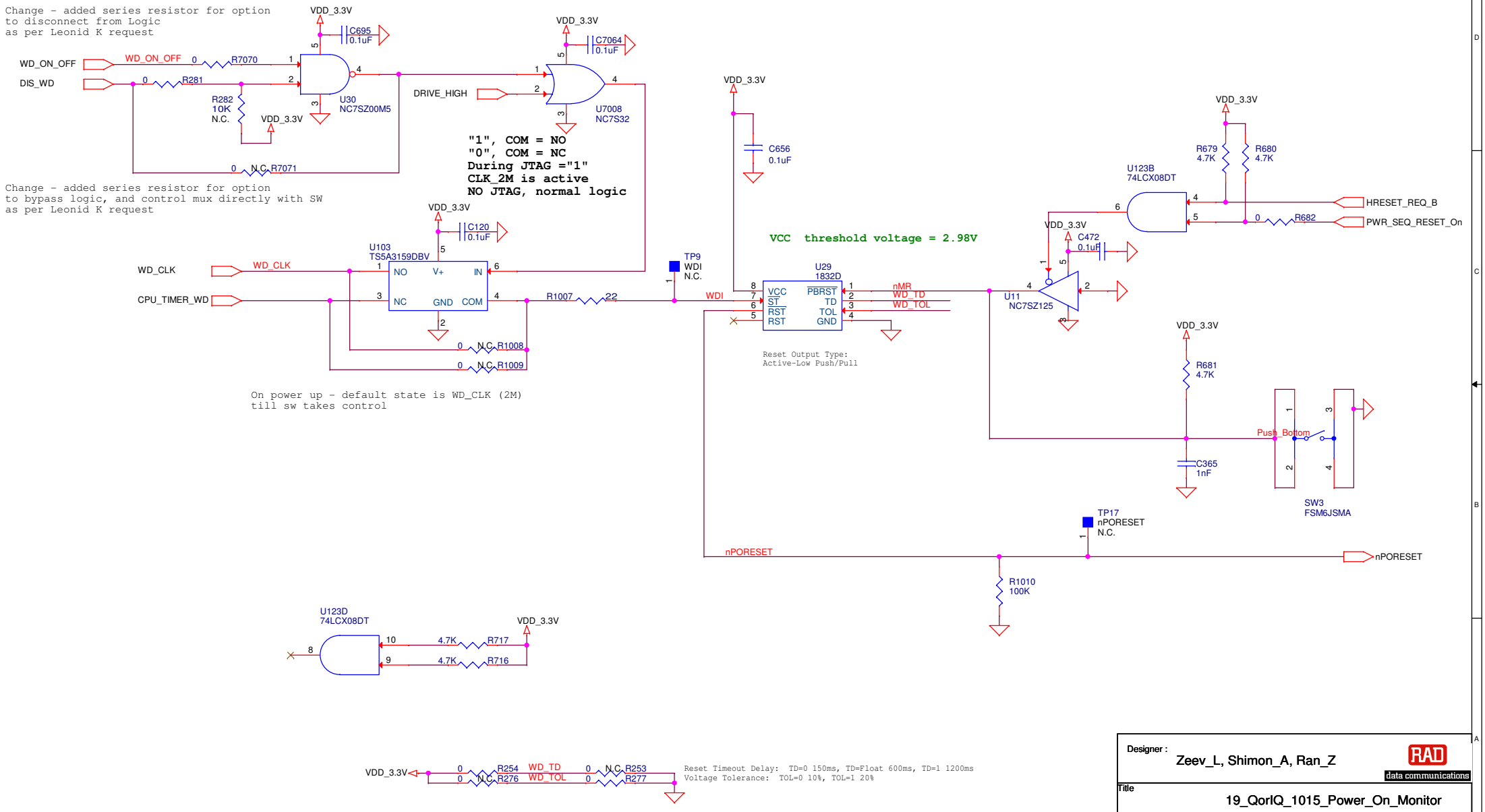
U37 NC7SV32P5
U38 NC7SV32P5
GPIO_WEN_L
GPIO_WEN_H
R7073 4.7K N.C.
Change - Connect just for debug
OE1
4.7K R7074

BOM change
Pull up not relevant since OE is always on
SMI_MNG_SW 10K N.C. R1475
RESETn_COMP 4.7K N.C. R448
COMP_PCIe_CPU_RST 4.7K N.C. R1360
SMI_GBE_PIGGY 10K N.C. R1437

HW ID
LC 0.5 19" --> 0xBC (CPU 16M)
LC 0.5 19" --> 0xBD (CPU 64M)
LC 0.5 19" --> 0xBE (CPU 64M), PCB Rev0.1, 0.2
MAIN 19" --> 0x9C

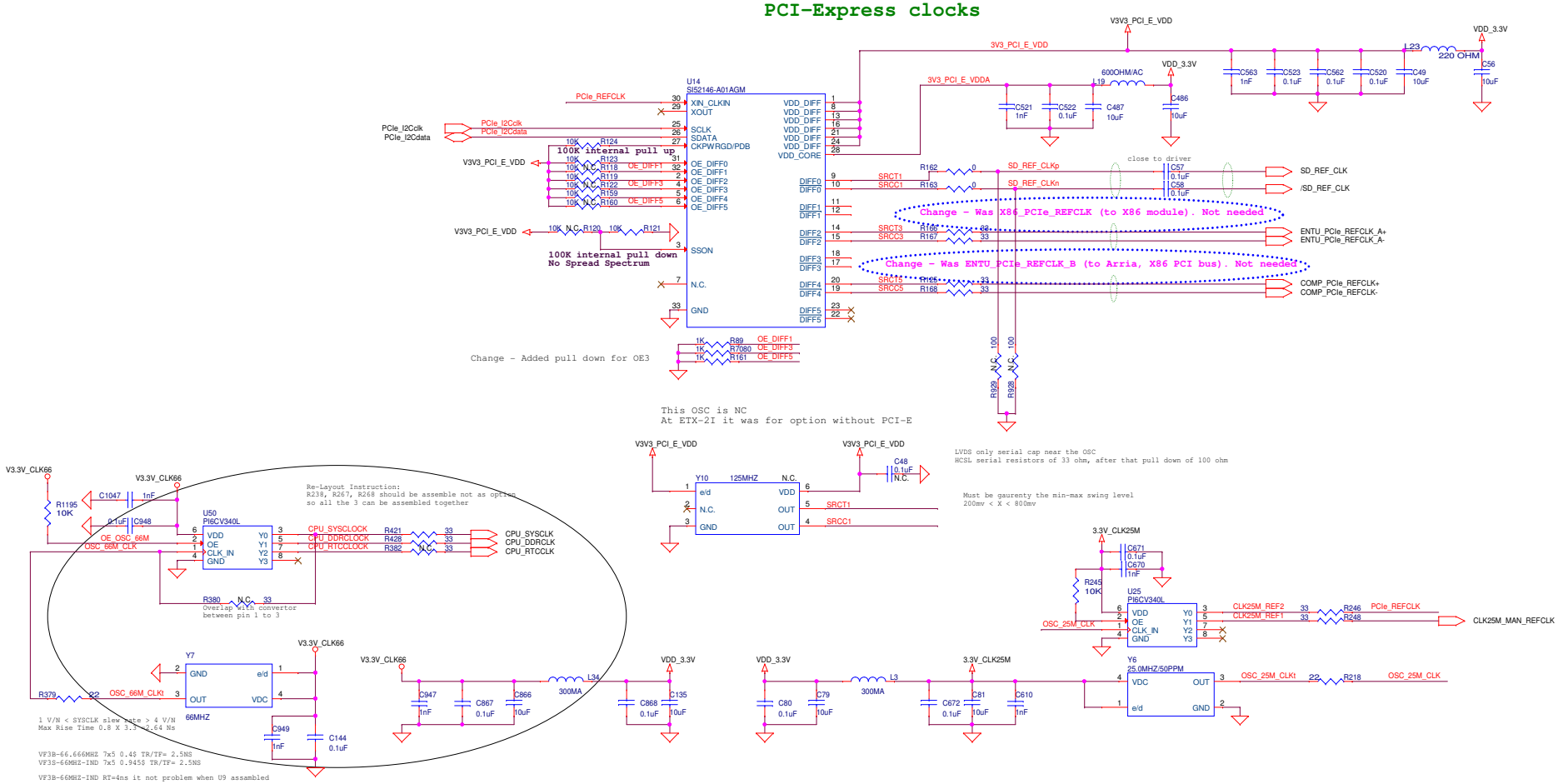
R439 10K N.C. R408
R440 10K N.C. R409
R441 10K N.C. R410
R442 10K N.C. R411
R443 10K N.C. R412
R444 10K N.C. R413
R445 10K N.C. R414
R447 10K N.C. R415

Designer : Zeev_L, Shimon_A, Ran_Z
RAD data communications
Title : 18_FLASH_EPROM
Size : Custom
Design Name : ETX-2I-10G-LC.REV0.2I
Rev : 0.0
Date : Friday, June 17, 2016
Sheet 12 of 46

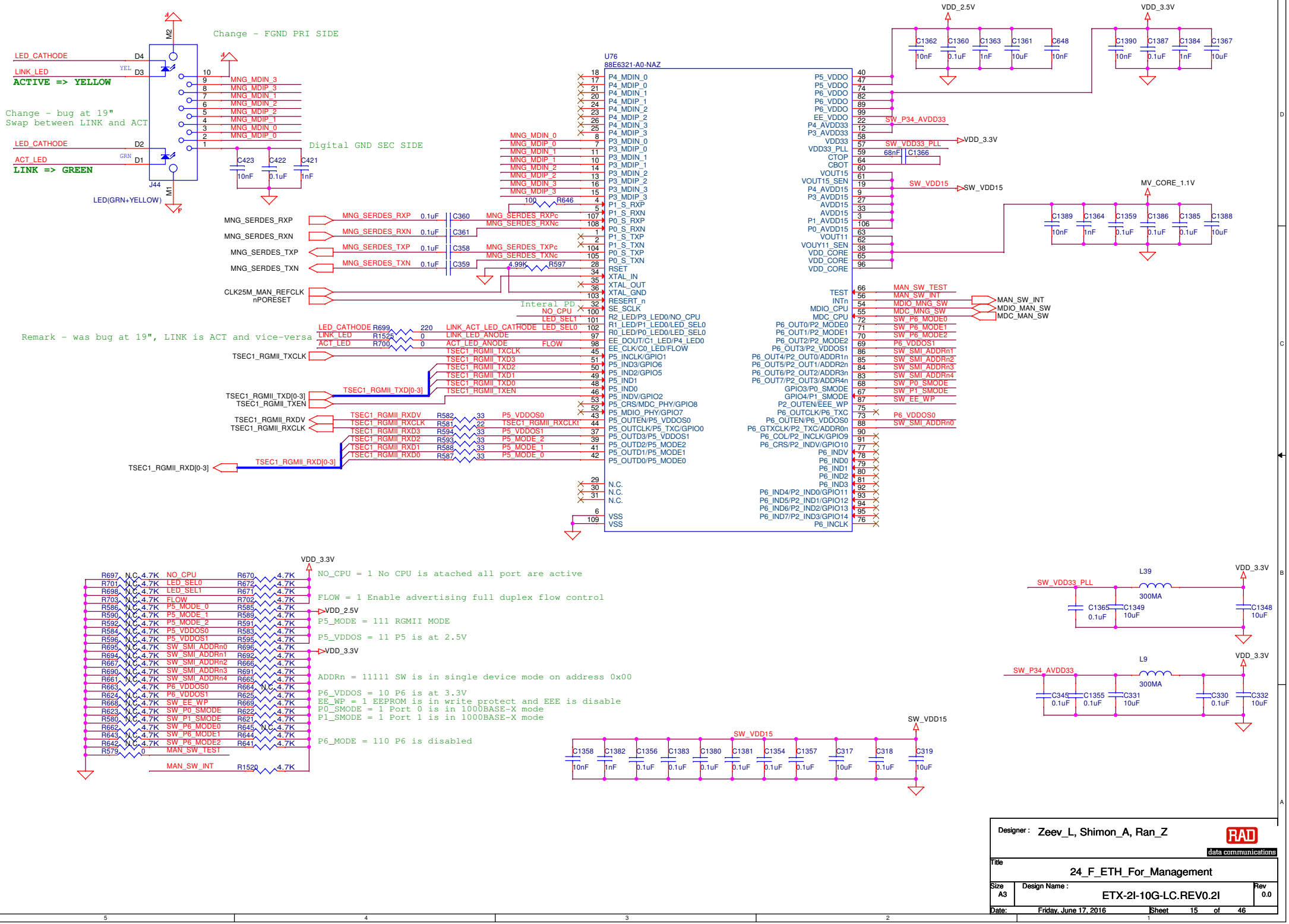


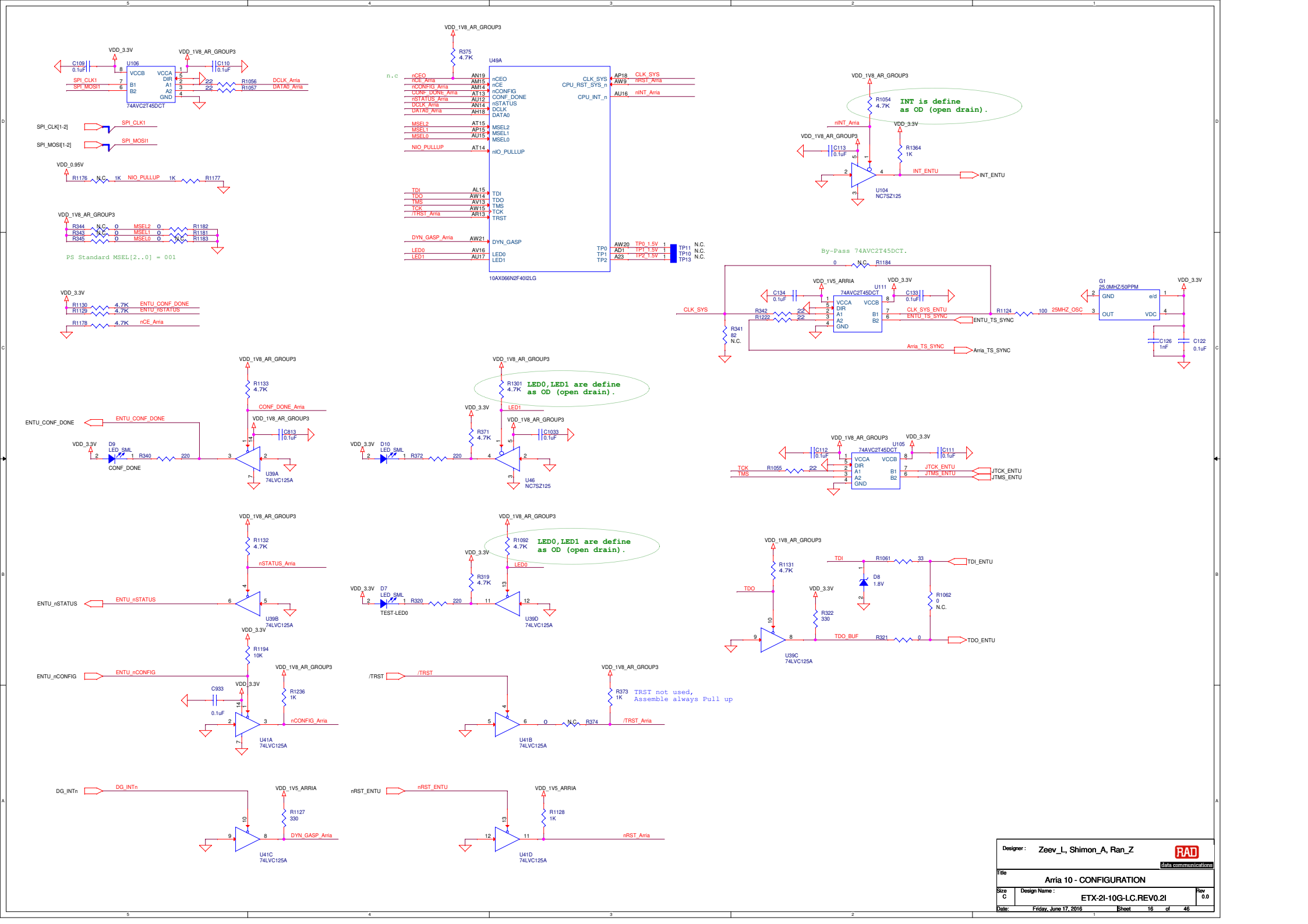
Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications
Title	19_QorIQ_1015_Power_On_Monitor	
Size B	Design Name : ETX-2I-10G-LC.REV0.2I	Rev 0.0
Date: Friday, June 17, 2016	Sheet 13 of 46	

PCI-Express clocks



Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications	
Title	20_QorIQ_1015_CLOCKS		
Size C	Design Name : ETX-2I-10G-LC.REV0.2I		Rev 0.0
Date: Friday, June 17, 2016	Sheet 14 of 46		


Change - FGND PRI SIDE
LED_CATHODE
LINK_LED
ACTIVE => YELLOW
Change - bug at 19"
Swap between LINK and ACT
LED_CATHODE
ACT_LED
LINK => GREEN
LED(GRN+YELLOW)
Digital GND SEC SIDE
U76
88E6321-A0-NAZ
MNG_SERDES_RXP
MNG_SERDES_RXN
MNG_SERDES_TXP
MNG_SERDES_TXN
CLK25M_MAN_REFCLK
nPORESET
Interal PD
Remark - was bug at 19", LINK is ACT and vice-versa
TSEC1_RGMII_TXCLK
TSEC1_RGMII_TXD[0-3]
TSEC1_RGMII_TXEN
TSEC1_RGMII_RXDV
TSEC1_RGMII_RXCLK
TSEC1_RGMII_RXD[0-3]
VDD_2.5V
VDD_3.3V
MV_CORE_1.1V
SW_VDD15
SW_P34_AVDD33
SW_VDD33_PLL
MAN_SW_INT
MDIO_MAN_SW
MDC_MAN_SW
NO_CPU = 1 No CPU is atached all port are active
FLOW = 1 Enable advertising full duplex flow control
P5_MODE = 111 RGMII MODE
P5_VDDOS = 11 P5 is at 2.5V
ADDRn = 11111 SW is in single device mode on address 0x00
P6_VDDOS = 10 P6 is at 3.3V
EE_WP = 1 EEPROM is in write protect and EEE is disable
P0_SMODE = 1 Port 0 is in 1000BASE-X mode
P1_SMODE = 1 Port 1 is in 1000BASE-X mode
P6_MODE = 110 P6 is disabled
L39
L9
300MA
Designer : Zeev_L, Shimon_A, Ran_Z
RAD
data communications
Title
24_F_ETH_For_Management
Size A3
Design Name : ETX-2I-10G-LC.REV0.2I
Rev 0.0
Date: Friday, June 17, 2016
Sheet 15 of 46


VDD_3.3V
VDD_1V8_AR_GROUP3
C109 0.1uF
C110 0.1uF
U106
74AVC2T45DCT
SPI_CLK1
SPI_MOSI1
R1056
R1057
DCLK_Arria
DATA0_Arria
SPI_CLK[1-2]
SPI_MOSI[1-2]
VDD_0.95V
R1176
R1177
NIO_PULLUP
PS Standard MSEL[2..0] = 001
R344
R343
R345
MSEL2
MSEL1
MSEL0
R1182
R1181
R1183
R1130
R1129
R1178
ENTU_CONF_DONE
ENTU_nSTATUS
nCE_Arria
U49A
10AX066N2F40I2LG
R375 4.7K
nCEO
nCONFIG_Arria
CONF_DONE_Arria
nSTATUS_Arria
DCLK_Arria
DATA0_Arria
MSEL2
MSEL1
MSEL0
NIO_PULLUP
TDI
TDO
TMS
TCK
/TRST_Arria
DYN_GASP_Arria
LED0
LED1
CLK_SYS
CPU_RST_SYS_n
CPU_INT_n
nRST_Arria
nINT_Arria
TP0
TP1
TP2
TP10
TP11
TP13
N.C.
R1054 4.7K
INT is define as OD (open drain).
nINT_Arria
C113 0.1uF
R1364 1K
INT_ENTU
U104
NC7SZ125
By-Pass 74AVC2T45DCT.
R1184
U111
C134 0.1uF
C133 0.1uF
CLK_SYS
R342
R1222
R341 82 N.C.
CLK_SYS_ENTU
ENTU_TS_SYNC
Arria_TS_SYNC
R1124
100
25MHZ_OSC
G1 25.0MHZ/50PPM
C126 1nF
C122 0.1uF
R1133 4.7K
CONF_DONE_Arria
C813 0.1uF
D9 LED_SML
R340
220
CONF_DONE
U39A 74LVC125A
R1301 4.7K
LED0,LED1 are define as OD (open drain).
LED1
D10 LED_SML
R372
R371 4.7K
C1033 0.1uF
U46 NC7SZ125
C112 0.1uF
U105
C111 0.1uF
TCK
TMS
R1055
JTCK_ENTU
JTMS_ENTU
R1132 4.7K
nSTATUS_Arria
U39B 74LVC125A
R1092 4.7K
LED0,LED1 are define as OD (open drain).
D7 LED_SML
R320
R319 4.7K
TEST-LED0
U39D 74LVC125A
R1131 4.7K
TDI
TDO
R1061
33
TDI_ENTU
D8 1.8V
R322 330
R1062 0 N.C.
TDO_BUF
R321
TDO_ENTU
U39C 74LVC125A
R1194 10K
ENTU_nCONFIG
C933 0.1uF
R1236 1K
nCONFIG_Arria
U41A 74LVC125A
/TRST
R373 1K
TRST not used, Assemble always Pull up
R374
/TRST_Arria
U41B 74LVC125A
DG_INTn
R1127 330
DYN_GASP_Arria
U41C 74LVC125A
nRST_ENTU
R1128 1K
nRST_Arria
U41D 74LVC125A
Designer : Zeev_L, Shimon_A, Ran_Z
RAD
data communications
Title
Arria 10 - CONFIGURATION
Size C
Design Name : ETX-2I-10G-LC.REV0.2I
Rev 0.0
Date: Friday, June 17, 2016
Sheet 16 of 46

exist in RAD:
LF-IC-IS43TR16128B-093NBL - DDR3 128M*16,1066/2132,1.5V,ROHS,COMMERTIAL.
LF-IC-IS43TR16128B-093NBLI - DDR3 128M*16,1066/2132,1.5V,ROHS,INDUSTRIAL.

SDRAM DDR3
2Gb/256MByte

Address/
Command

Control

Clock

VREFDQ & VREFCA
come from the same power source
but should be routed to and then
decoupled separately at DDR3.

2.2 pf compensation cap
before the first component

BOM change of DM to 2xODT(120) = 240 ohm,
Vil=0.5V<VilMax=0.65V
Changed from 0 ohm with higher current consumption

Place it
near by SI

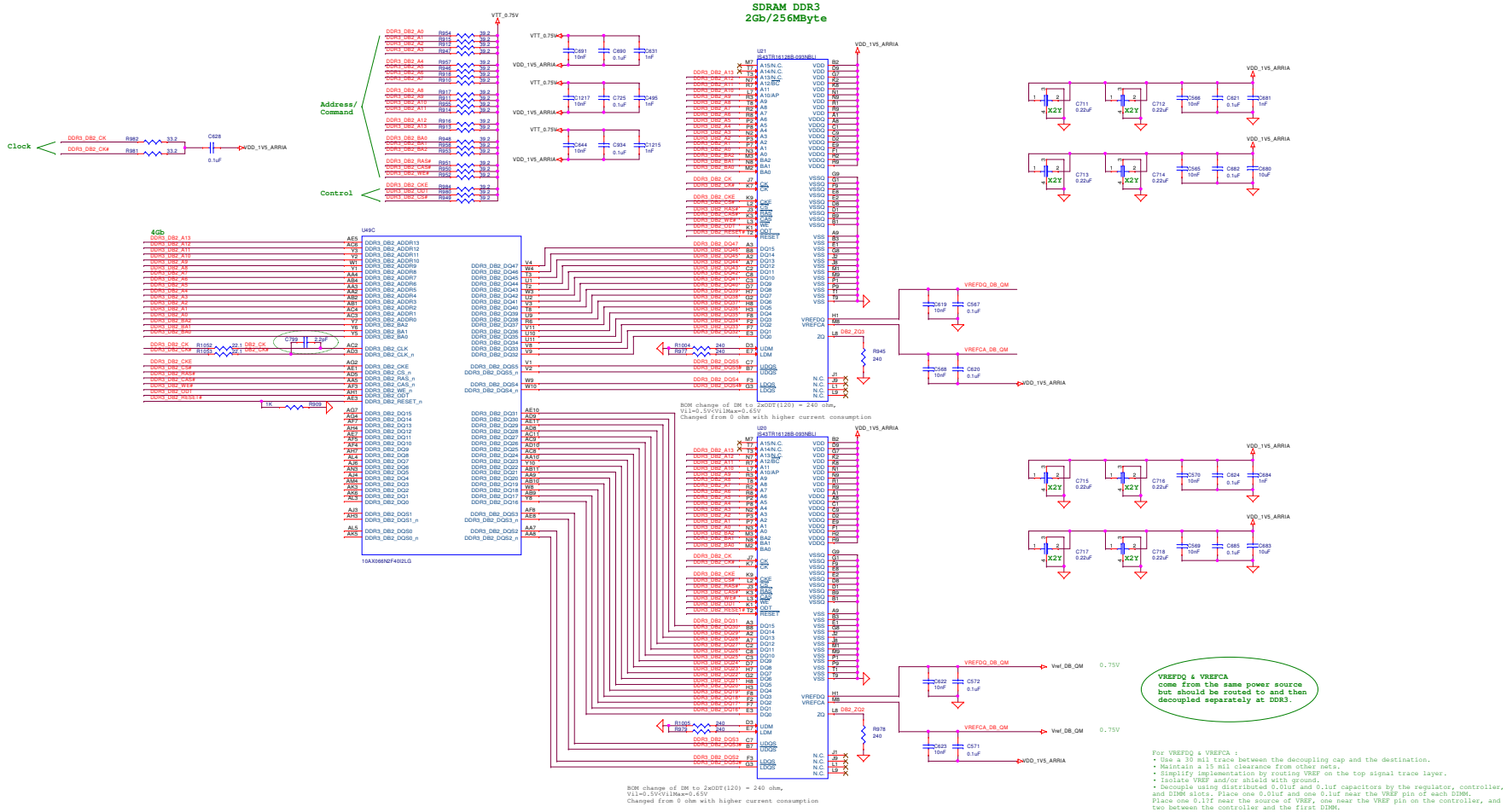
Short trace

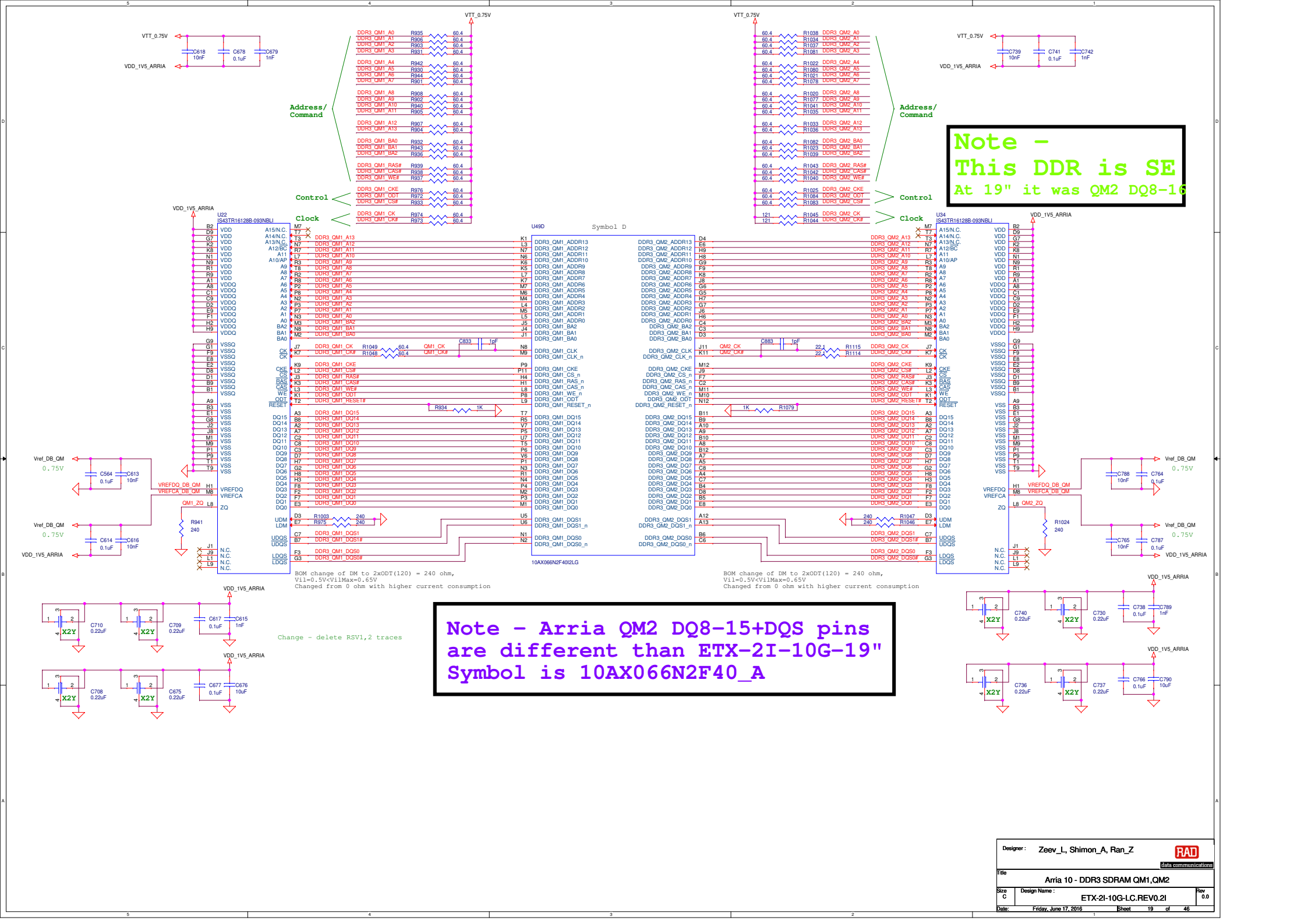
For VREFDQ & VREFCA :
• Use a 30 mil trace between the decoupling cap and the destination.
• Maintain a 15 mil clearance from other nets.
• Simplify implementation by routing VREF on the top signal trace layer.
• Isolate VREF and/or shield with ground.
• Decouple using distributed 0.01uf and 0.1uf capacitors by the regulator, controller,
and DIMM slots. Place one 0.01uf and one 0.1uf near the VREF pin of each DIMM.
Place one 0.1?f near the source of VREF, one near the VREF pin on the controller, and
two between the controller and the first DIMM.

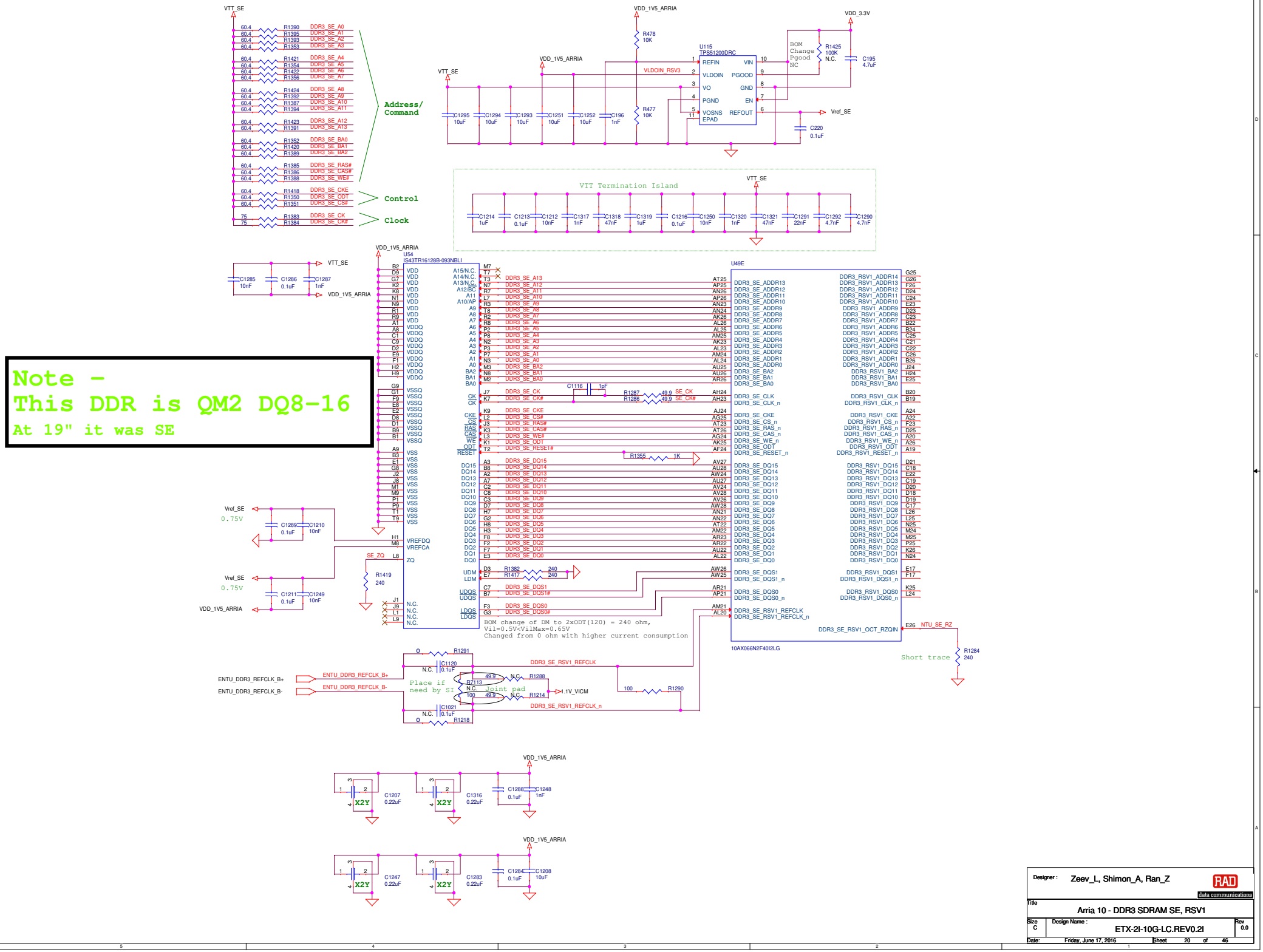
If 1.1_VICM will be used,
assemble the inductor instead of the resistor, to get PI filter

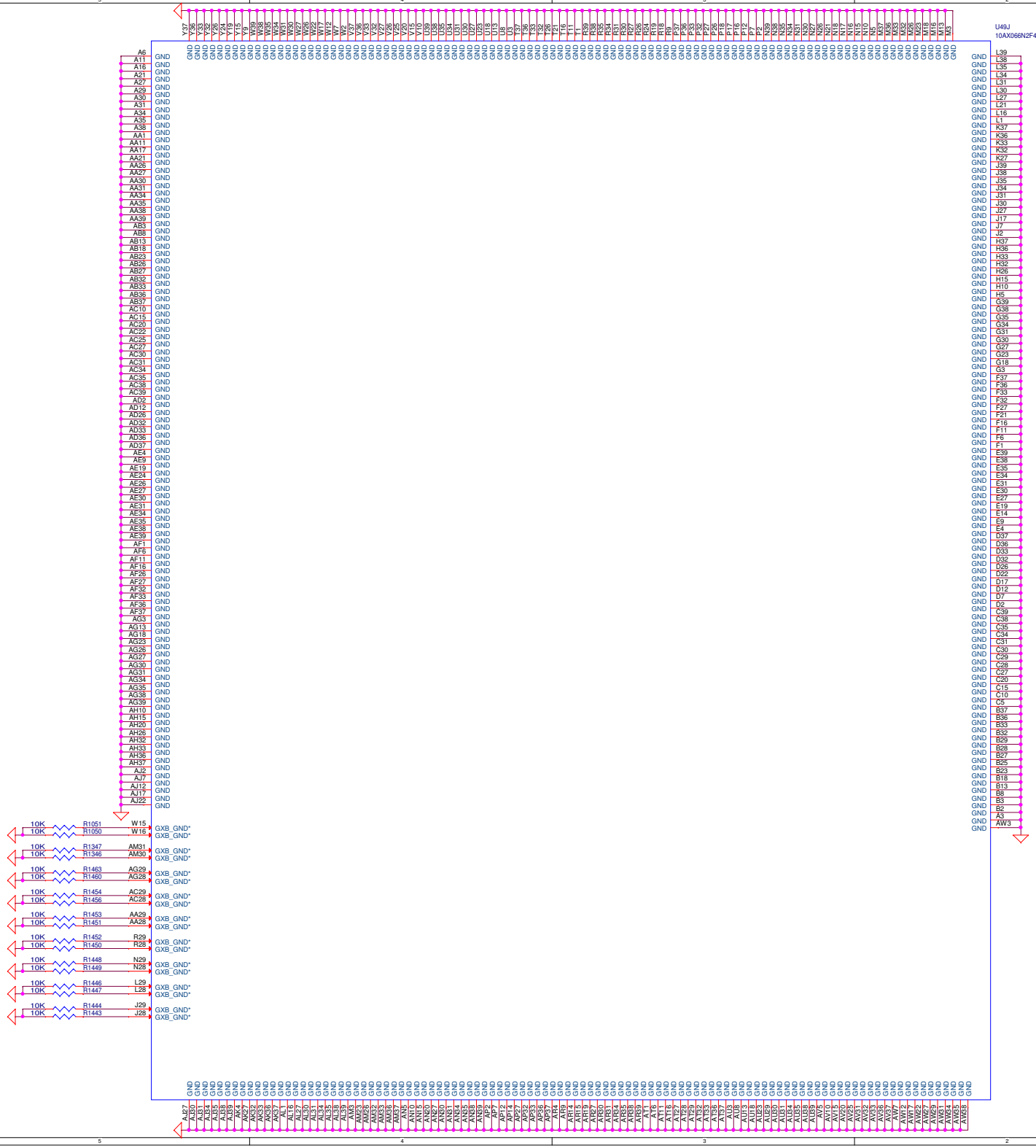
BOM change of DM to 2xODT(120) = 240 ohm,
Vil=0.5V<VilMax=0.65V
Changed from 0 ohm with higher current consumption

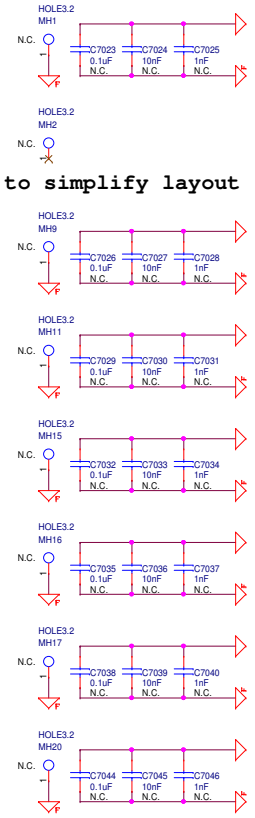
Designer: Zeev_L, Shimon_A, Ran_Z			RAD
			data communications
Title: Arria 10 - DDR3 SDRAM DB1			
Size: D	Design Name: ETX-2I-10G-LC.REV0.2I		Rev: 0.0
Date: Friday, June 17, 2016	Sheet 17 of 46		


SDRAM DDR3
2Gb/256MByte
Address/
Command
Control
Clock
VTT_0.75V
VDD_1V5_ARRIA
U49C
4Gb
10AX066N2F40I2LG
U21
U20
IS43TR16128B-093NBLI
BOM change of DM to 2xODT(120) = 240 ohm,
Vil=0.5V<VilMax=0.65V
Changed from 0 ohm with higher current consumption
VREFDQ_DB_QM
VREFCA_DB_QM
Vref_DB_QM
0.75V
VREFDQ & VREFCA
come from the same power source
but should be routed to and then
decoupled separately at DDR3.
For VREFDQ & VREFCA :
• Use a 30 mil trace between the decoupling cap and the destination.
• Maintain a 15 mil clearance from other nets.
• Simplify implementation by routing VREF on the top signal trace layer.
• Isolate VREF and/or shield with ground.
• Decouple using distributed 0.01uf and 0.1uf capacitors by the regulator, controller, and DIMM slots. Place one 0.01uf and one 0.1uf near the VREF pin of each DIMM. Place one 0.1ff near the source of VREF, one near the VREF pin on the controller, and two between the controller and the first DIMM.
Designer : Zeev_L, Shimon_A, Ran_Z
RAD
data communications
Title
Arria 10 - DDR3 SDRAM DB2
Size D
Design Name : ETX-2I-10G-LC.REV0.2I
Rev 0.0
Date: Friday, June 17, 2016
Sheet 19 of 46


Address/
Command
Control
Clock
Note -
This DDR is SE
At 19" it was QM2 DQ8-16
Note - Arria QM2 DQ8-15+DQS pins
are different than ETX-2I-10G-19"
Symbol is 10AX066N2F40_A
BOM change of DM to 2xODT(120) = 240 ohm,
Vil=0.5V<VilMax=0.65V
Changed from 0 ohm with higher current consumption
Change - delete RSV1,2 traces
10AX066N2F40I2LG
Designer : Zeev_L, Shimon_A, Ran_Z
Title
Arria 10 - DDR3 SDRAM QM1,QM2
Design Name : ETX-2I-10G-LC.REV0.2I
Rev 0.0
Date: Friday, June 17, 2016
Sheet 19 of 46


Note –
This DDR is QM2 DQ8-16
At 19" it was SE
Address/
Command
Control
Clock
VTT Termination Island
U115
TPS51200DRC
U54
IS43TR16128B-093NBLI
U49E
10AX066N2F40I2LG
BOM change of DM to 2xODT(120) = 240 ohm,
Vil=0.5V<VilMax=0.65V
Changed from 0 ohm with higher current consumption
Place if need by SI
Joint pad
Short trace
Designer : Zeev_L, Shimon_A, Ran_Z
data communications
Title
Arria 10 - DDR3 SDRAM SE, RSV1
Design Name : ETX-2I-10G-LC.REV0.2I
Rev 0.0
Date: Friday, June 17, 2016
Sheet 20 of 46



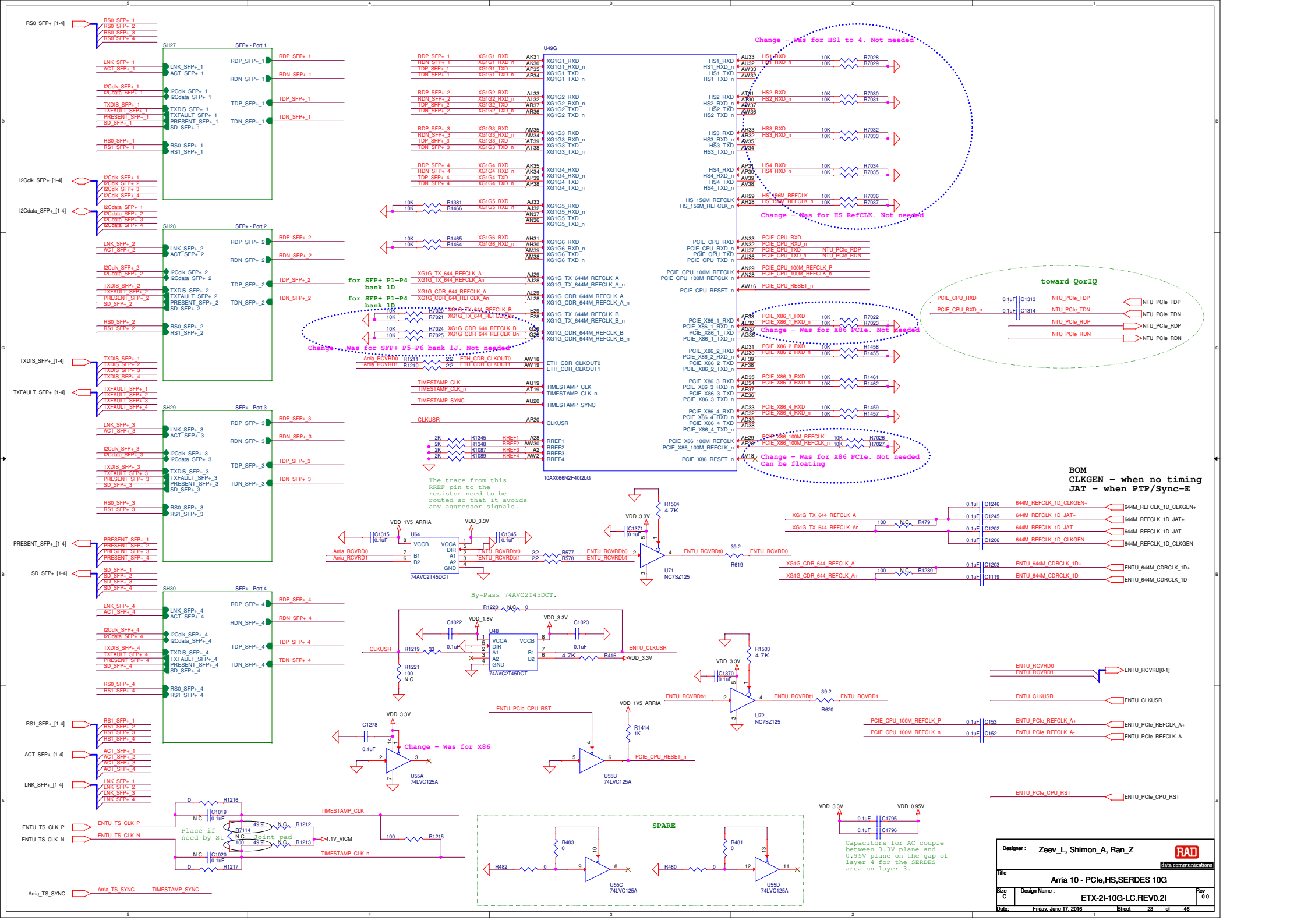


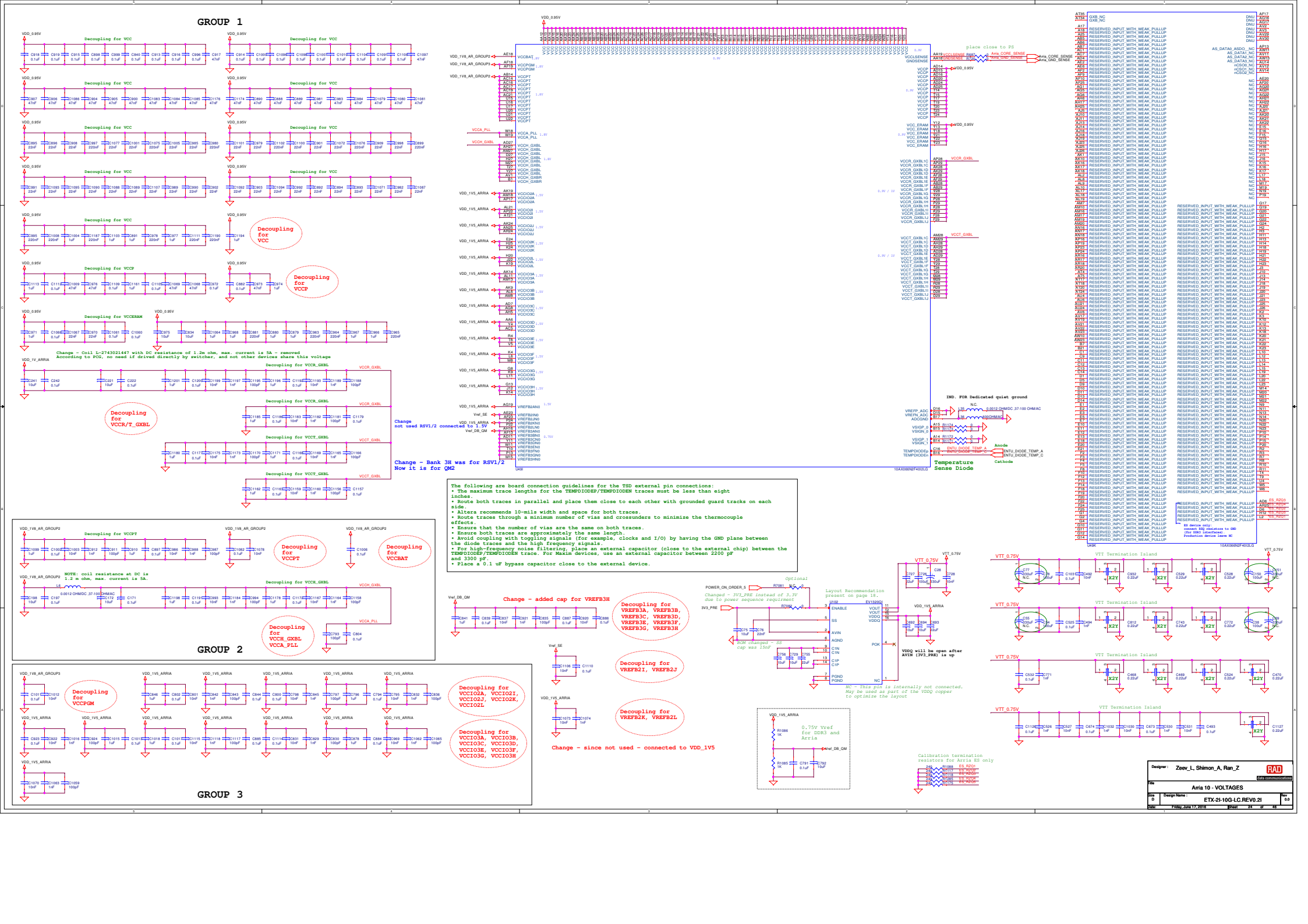
Change
MH2 is FGND
Keep floating to simplify layout

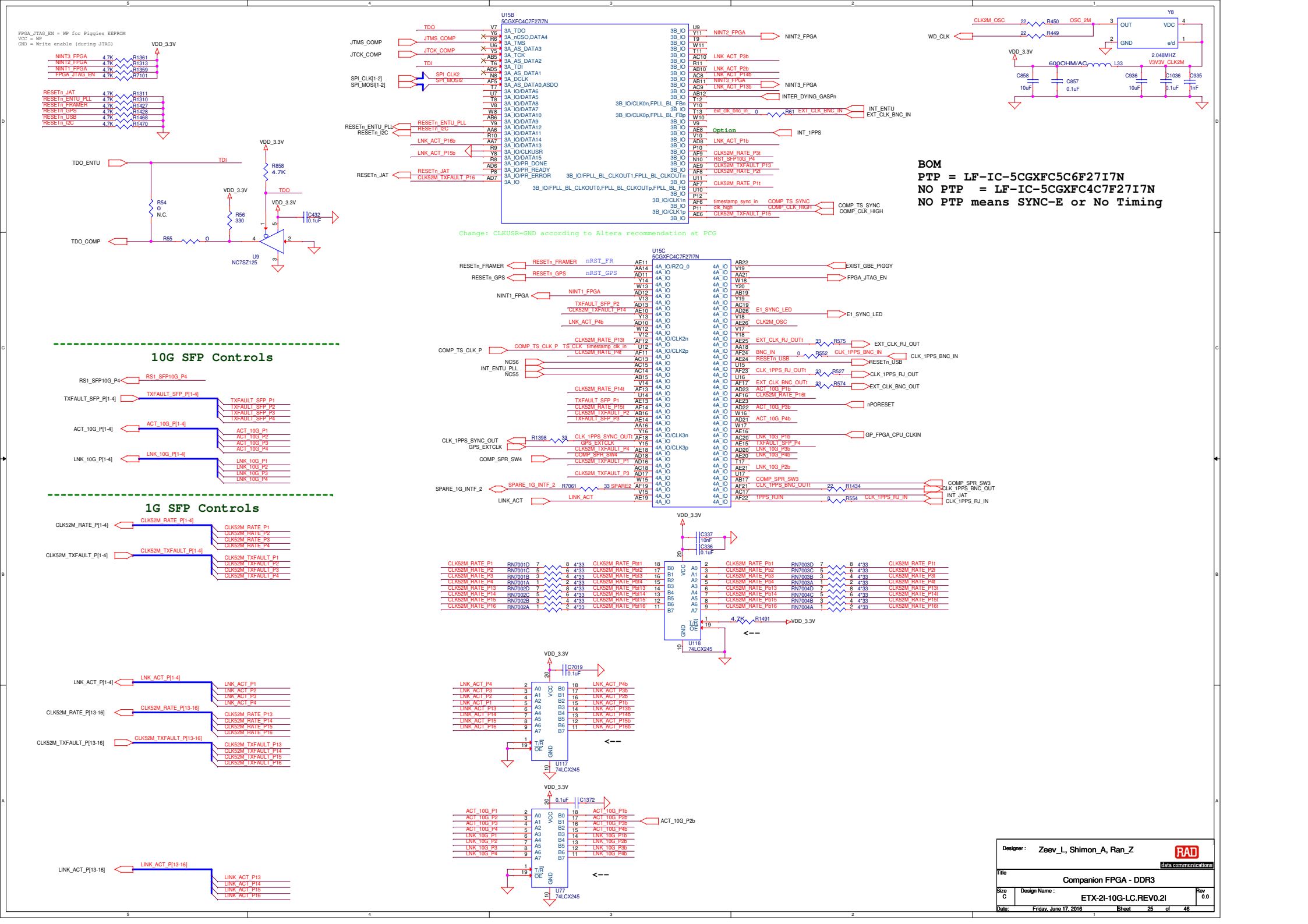
Change
Adding FGND with capacitors to GND

Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications	
Title	Arria 10 - GND		
Size C	Design Name : ETX-2I-10G-LC.REV0.2I		Rev 0.0
Date:	Friday, June 17, 2016	Sheet 21 of 46	


TSEC2_TDP_SGMII
TSEC2_TDP_SGMII
C1243 0.1uF
SGMII_CPU_RXD
CPU
TSEC2_TDN_SGMII
TSEC2_TDN_SGMII
C1242 0.1uF
SGMII_CPU_RXD_n
COMP_SGMII_TDP
COMP_SGMII_TDP
C180 0.1uF
SGMII_COMP_RXD
COMP
COMP_SGMII_TDN
COMP_SGMII_TDN
C179 0.1uF
SGMII_COMP_RXD_n
RDP_USER1
SGMII1_RXD
RDN_USER1
SGMII1_RXD_n
RDP_USER[1-4]
RDP_USER1
RDP_USER2
RDP_USER3
RDP_USER4
RDN_USER[1-4]
RDN_USER1
RDN_USER2
RDN_USER3
RDN_USER4
RDP_USER2
SGMII2_RXD
RDN_USER2
SGMII2_RXD_n
RDP_USER[13-16]
RDP_USER13
RDP_USER14
RDP_USER15
RDP_USER16
RDN_USER[13-16]
RDN_USER13
RDN_USER14
RDN_USER15
RDN_USER16
RDP_USER3
SGMII3_RXD
RDN_USER3
SGMII3_RXD_n
RDP_USER4
SGMII4_RXD
RDN_USER4
SGMII4_RXD_n
RDP_USER13
SGMII13_RXD
RDN_USER13
SGMII13_RXD_n
RDP_USER14
SGMII14_RXD
RDN_USER14
SGMII14_RXD_n
RDP_USER15
SGMII15_RXD
RDN_USER15
SGMII15_RXD_n
RDP_USER16
SGMII16_RXD
RDN_USER16
SGMII16_RXD_n
Change
Remove series capacitors on serdes
(no PHY, SFP will terminate),
on 1G piggy:
If there is PHY capacitors assembled
If not - SFP have them
MNG_SERDES_TXP
MNG_SERDES_TXP
C225 0.1uF
SGMII26_RXD
Marvell
88E6321
MNG_SERDES_TXN
MNG_SERDES_TXN
C224 0.1uF
SGMII26_RXD_n
ENTU_125M_REFCLK+
ENTU_125M_REFCLK+
C1155 0.1uF
SGMII_TX_125M_REFCLK
FROM JAT.
100
N.C
R1282
ENTU_125M_REFCLK-
ENTU_125M_REFCLK-
C1154 0.1uF
SGMII_TX_125M_REFCLK_n
Signal pairs routed with
100 ohm diff impedance.
ENTU_125M_CDRCLK+
ENTU_125M_CDRCLK+
C1057 0.1uF
SGMII_CDR_125_REFCLK
FROM CLK-
GENERATOR
100
N.C
R1283
ENTU_125M_CDRCLK-
ENTU_125M_CDRCLK-
C1058 0.1uF
SGMII_CDR_125_REFCLKn
Signal pairs routed with
100 ohm diff impedance.
U49H
SGMII_CPU_RXD
SGMII_CPU_RXD_n
SGMII_CPU_TXD
SGMII_CPU_TXD_n
G33
G32
B39
B38
SGMII_CPU_RXD
SGMII_CPU_RXD_n
SGMII_CPU_TXD
SGMII_CPU_TXD_n
SGMII_COMP_RXD
SGMII_COMP_RXD_n
SGMII_COMP_TXD
SGMII_COMP_TXD_n
H31
H30
C37
C36
SGMII_COMP_RXD
SGMII_COMP_RXD_n
SGMII_COMP_TXD
SGMII_COMP_TXD_n
SGMII1_RXD
SGMII1_RXD_n
SGMII1_TXD
SGMII1_TXD_n
AH35
AH34
AL37
AL36
SGMII1_RXD
SGMII1_RXD_n
SGMII1_TXD
SGMII1_TXD_n
SGMII2_RXD
SGMII2_RXD_n
SGMII2_TXD
SGMII2_TXD_n
AG33
AG32
AK39
AK38
SGMII2_RXD
SGMII2_RXD_n
SGMII2_TXD
SGMII2_TXD_n
SGMII3_RXD
SGMII3_RXD_n
SGMII3_TXD
SGMII3_TXD_n
AF31
AF30
AJ37
AJ36
SGMII3_RXD
SGMII3_RXD_n
SGMII3_TXD
SGMII3_TXD_n
SGMII4_RXD
SGMII4_RXD_n
SGMII4_TXD
SGMII4_TXD_n
AF35
AF34
AH39
AH38
SGMII4_RXD
SGMII4_RXD_n
SGMII4_TXD
SGMII4_TXD_n
R7004
10K
SGMII5_RXD
SGMII5_RXD_n
AB31
AB30
AC37
AC36
SGMII5_RXD
SGMII5_RXD_n
SGMII5_TXD
SGMII5_TXD_n
R7005
10K
SGMII6_RXD
SGMII6_RXD_n
AA33
AA32
AA37
AA36
SGMII6_RXD
SGMII6_RXD_n
SGMII6_TXD
SGMII6_TXD_n
R7006
10K
SGMII7_RXD
SGMII7_RXD_n
AB35
AB34
AB39
AB38
SGMII7_RXD
SGMII7_RXD_n
SGMII7_TXD
SGMII7_TXD_n
R7008
10K
SGMII8_RXD
SGMII8_RXD_n
Y31
Y30
W37
W36
SGMII8_RXD
SGMII8_RXD_n
SGMII8_TXD
SGMII8_TXD_n
R7010
10K
SGMII9_RXD
SGMII9_RXD_n
M31
M30
G37
G36
SGMII9_RXD
SGMII9_RXD_n
SGMII9_TXD
SGMII9_TXD_n
R7012
10K
SGMII10_RXD
SGMII10_RXD_n
L33
L32
F39
F38
SGMII10_RXD
SGMII10_RXD_n
SGMII10_TXD
SGMII10_TXD_n
R7014
10K
SGMII11_RXD
SGMII11_RXD_n
K35
K34
F35
F34
SGMII11_RXD
SGMII11_RXD_n
SGMII11_TXD
SGMII11_TXD_n
R7016
10K
SGMII12_RXD
SGMII12_RXD_n
K31
K30
E37
E36
SGMII12_RXD
SGMII12_RXD_n
SGMII12_TXD
SGMII12_TXD_n
SGMII13_RXD
SGMII13_RXD_n
SGMII13_TXD
SGMII13_TXD_n
Y35
Y34
Y39
Y38
SGMII13_RXD
SGMII13_RXD_n
SGMII13_TXD
SGMII13_TXD_n
SGMII14_RXD
SGMII14_RXD_n
SGMII14_TXD
SGMII14_TXD_n
W33
W32
V39
V38
SGMII14_RXD
SGMII14_RXD_n
SGMII14_TXD
SGMII14_TXD_n
SGMII15_RXD
SGMII15_RXD_n
SGMII15_TXD
SGMII15_TXD_n
V35
V34
U37
U36
SGMII15_RXD
SGMII15_RXD_n
SGMII15_TXD
SGMII15_TXD_n
LINKACT
AH19
LINK_ACT
SGMII_TX_125M_REFCLK
SGMII_TX_125M_REFCLK_n
U29
U28
SGMII_TX_125M_REFCLK
SGMII_TX_125M_REFCLK_n
SGMII_CDR_125_REFCLK
SGMII_CDR_125_REFCLKn
W29
W28
SGMII_CDR_125_REFCLK
SGMII_CDR_125_REFCLK_n
10AX066N2F40I2LG
SGMII30_RXD
SGMII30_RXD_n
SGMII30_TXD
SGMII30_TXD_n
B31
B30
A33
A32
SGMII30_RXD
SGMII30_RXD_n
R7000
10K
SGMII29_RXD
SGMII29_RXD_n
SGMII29_TXD
SGMII29_TXD_n
D31
D30
C33
C32
SGMII29_RXD
SGMII29_RXD_n
R7001
10K
SGMII28_RXD
SGMII28_RXD_n
SGMII28_TXD
SGMII28_TXD_n
E33
E32
B35
B34
SGMII28_RXD
SGMII28_RXD_n
R7002
10K
SGMII27_RXD
SGMII27_RXD_n
SGMII27_TXD
SGMII27_TXD_n
F31
F30
A37
A36
SGMII27_RXD
SGMII27_RXD_n
R7003
10K
SGMII26_RXD
SGMII26_RXD_n
SGMII26_TXD
SGMII26_TXD_n
H35
H34
D35
D34
SGMII26_RXD_n
SGMII26_TXD
SGMII26_TXD_n
SGMII25_RXD
SGMII25_RXD_n
SGMII25_TXD
SGMII25_TXD_n
J33
J32
D39
D38
SGMII25_RXD
SGMII25_RXD_n
R1445
10K
SGMII24_RXD
SGMII24_RXD_n
SGMII24_TXD
SGMII24_TXD_n
M35
M34
H39
H38
SGMII24_RXD
SGMII24_RXD_n
R7007
10K
SGMII23_RXD
SGMII23_RXD_n
SGMII23_TXD
SGMII23_TXD_n
N33
N32
J37
J36
SGMII23_RXD
SGMII23_RXD_n
R7009
10K
SGMII22_RXD
SGMII22_RXD_n
SGMII22_TXD
SGMII22_TXD_n
P31
P30
K39
K38
SGMII22_RXD
SGMII22_RXD_n
R7011
10K
SGMII21_RXD
SGMII21_RXD_n
SGMII21_TXD
SGMII21_TXD_n
P35
P34
L37
L36
SGMII21_RXD
SGMII21_RXD_n
R7013
10K
SGMII20_RXD
SGMII20_RXD_n
SGMII20_TXD
SGMII20_TXD_n
R33
R32
M39
M38
SGMII20_RXD
SGMII20_RXD_n
R7015
10K
SGMII19_RXD
SGMII19_RXD_n
SGMII19_TXD
SGMII19_TXD_n
T31
T30
N37
N36
SGMII19_RXD
SGMII19_RXD_n
R7017
10K
SGMII18_RXD
SGMII18_RXD_n
SGMII18_TXD
SGMII18_TXD_n
T35
T34
P39
P38
SGMII18_RXD
SGMII18_RXD_n
R7018
10K
SGMII17_RXD
SGMII17_RXD_n
SGMII17_TXD
SGMII17_TXD_n
U33
U32
R37
R36
SGMII17_RXD
SGMII17_RXD_n
R7019
10K
SGMII16_RXD
SGMII16_RXD_n
SGMII16_TXD
SGMII16_TXD_n
V31
V30
T39
T38
SGMII16_RXD
SGMII16_RXD_n
SGMII16_TXD
SGMII16_TXD_n
C347
0.1uF
VDD_1V5
U122
VCCB
B1
B2
GND
VCCA
DIR
A1
A2
74AVC2T45DCT
VDD_3.3V
C348
0.1uF
LINKACT
10K
R1523
22
R1522
LINK_ACT
LINK_ACT
Note - Can be drived from VDD_1.5V of Arria,
Due to planes, it uses 1.5V of CPU
SGMII_CPU_TXD
SGMII_CPU_TXD_n
TSEC2_RDP_SGMII
TSEC2_RDN_SGMII
TSEC2_RDP_SGMII
TSEC2_RDN_SGMII
SGMII_COMP_TXD
SGMII_COMP_TXD_n
COMP_SGMII_RDP
COMP_SGMII_RDN
COMP_SGMII_RDP
COMP_SGMII_RDN
SGMII1_TXD
SGMII2_TXD
SGMII3_TXD
SGMII4_TXD
TDP_USER1
TDP_USER2
TDP_USER3
TDP_USER4
TDP_USER[1-4]
SGMII1_TXD_n
SGMII2_TXD_n
SGMII3_TXD_n
SGMII4_TXD_n
TDN_USER1
TDN_USER2
TDN_USER3
TDN_USER4
TDN_USER[1-4]
SGMII13_TXD
SGMII14_TXD
SGMII15_TXD
SGMII16_TXD
TDP_USER13
TDP_USER14
TDP_USER15
TDP_USER16
TDP_USER[13-16]
SGMII13_TXD_n
SGMII14_TXD_n
SGMII15_TXD_n
SGMII16_TXD_n
TDN_USER13
TDN_USER14
TDN_USER15
TDN_USER16
TDN_USER[13-16]
SGMII26_TXD
SGMII26_TXD_n
MNG_SERDES_RXP
MNG_SERDES_RXN
MNG_SERDES_RXP
MNG_SERDES_RXN
Change
Remove ports 5-12, X86, etc.
Designer : Zeev_L, Shimon_A, Ran_Z
RAD
data communications
Title
Arria 10 - MAC SGMII
Size C
Design Name : ETX-2I-10G-LC.REV0.2I
Rev 0.0
Date: Friday, June 17, 2016
Sheet 22 of 46


SH27
SH28
SH29
SH30
SFP+ - Port 1
SFP+ - Port 2
SFP+ - Port 3
SFP+ - Port 4
U49G
10AX066N2F40I2LG
Change - Was for HS1 to 4. Not needed
Change - Was for HS RefCLK. Not needed
Change - Was for SFP+ P5-P6 bank 1J. Not needed
for SFP+ P1-P4 bank 1D
for SFP+ P1-P4 bank 1D
Change - Was for X86 PCIe. Not needed
Change - Was for X86 PCIe. Not needed Can be floating
toward QorIQ
The trace from this RREF pin to the resistor need to be routed so that it avoids any aggressor signals.
By-Pass 74AVC2T45DCT.
Change - Was for X86
SPARE
Capacitors for AC couple between 3.3V plane and 0.95V plane on the gap of layer 4 for the SERDES area on layer 3.
Place if need by SI
Joint pad
BOM
CLKGEN - when no timing
JAT - when PTP/Sync-E
Designer : Zeev_L, Shimon_A, Ran_Z
data communications
Title
Arria 10 - PCIe,HS,SERDES 10G
Size C
Design Name : ETX-2I-10G-LC.REV0.2I
Rev 0.0
Date: Friday, June 17, 2016
Sheet 23 of 46


GROUP 1
Decoupling for VCC
Decoupling for VCCP
Decoupling for VCCERAM
Decoupling for VCCR/T_GXBL
Decoupling for VCCPT
Decoupling for VCCBAT
Decoupling for VCCH_GXBL VCCA_PLL
GROUP 2
Decoupling for VCCPGM
GROUP 3
Change - Coil L=2743021447 with DC resistance of 1.2m ohm, max. current is 5A - removed
According to PCG, no need if drived directly by switcher, and not other devices share this voltage
Change - Bank 3H was for RSV1/2
Now it is for QM2
Change not used RSV1/2 connected to 1.5V
Change - added cap for VREFB3H
Decoupling for VREFB3A, VREFB3B, VREFB3C, VREFB3D, VREFB3E, VREFB3F, VREFB3G, VREFB3H
Decoupling for VREFB2I, VREFB2J
Decoupling for VREFB2K, VREFB2L
Change - since not used - connected to VDD_1V5
Decoupling for VCCIO2A, VCCIO2I, VCCIO2J, VCCIO2K, VCCIO2L
Decoupling for VCCIO3A, VCCIO3B, VCCIO3C, VCCIO3D, VCCIO3E, VCCIO3F, VCCIO3G, VCCIO3H
The following are board connection guidelines for the TSD external pin connections:
• The maximum trace lengths for the TEMPDIODEP/TEMPDIODEN traces must be less than eight inches.
• Route both traces in parallel and place them close to each other with grounded guard tracks on each side.
• Altera recommends 10-mils width and space for both traces.
• Route traces through a minimum number of vias and crossunders to minimize the thermocouple effects.
• Ensure that the number of vias are the same on both traces.
• Ensure both traces are approximately the same length.
• Avoid coupling with toggling signals (for example, clocks and I/O) by having the GND plane between the diode traces and the high frequency signals.
• For high-frequency noise filtering, place an external capacitor (close to the external chip) between the TEMPDIODEP/TEMPDIODEN trace. For Maxim devices, use an external capacitor between 2200 pF and 3300 pF.
• Place a 0.1 uF bypass capacitor close to the external device.
place close to PS
IND. FOR Dedicated quiet ground
Temperature Sense Diode
Anode
Cathode
Layout Recommendation present on page 18.
Optional
Changed - 3V3_PRE instead of 3.3V due to power sequence requirment
VDDQ will be open after AVIN (3V3_PRE) is up
NC - This pin is internally not connected. May be used as part of the VDDQ copper to optimize the layout
0.75V Vref for DDR3 and Arria
Calibration termination resistors for Arria ES only
VTT Termination Island
Designer : Zeev_L, Shimon_A, Ran_Z
RAD
Title
Arria 10 - VOLTAGES
Size D
Design Name : ETX-2I-10G-LC.REV0.2I
Rev 0.0
Date: Friday, June 17, 2016
Sheet 24 of 46



Designer :	Zeev_L, Shimon_A, Ran_Z
Title	Companion FPGA - DDR3
Size C	Design Name : ETX-2I-10G-LC.REV0.2I
Rev	0.0
Date:	Friday, June 17, 2016
Sheet	25 of 46

Change - remove - connected just to GP, will be directly inside companion
COMP_GPS_CLK_IN, COMP_1PPS_IN
PRI, SEC, Third, Forth
CLK_2M_from_1PPS
Cleaner_1PPS
COMP_GPS_CLK_IN

BOM
PTP = LF-IC-5CGXFC5C6F27I7N
NO PTP = LF-IC-5CGXFC4C7F27I7N
NO PTP means SYNC-E or No Timing

U1SE 5CGXFC4C7F27I7N

U1SF 5CGXFC4C7F27I7N

U1SD 5CGXFC4C7F27I7N

BOM remark
RCVCLK weak pull up assembled always
when there is clock from piggy and when there is no clock

Debug is for future use

Change - MSEL directly

Passive Serial with
Voltage standard 3.3V
PS Standard MSEL[4..0] = 10001

MSEL0
'0' - fast POR (4ms)
'1' - slow POR (100ms)

10G SFP Controls

1G SFP Controls

Change - Rubidium CLK removed (came from X86)

After SI simulaion, decided to bypass clock buffer and DFF

CLK_RIGH used for the clock recovery machines in SYNC-CLK core, also used for REFCLK in SYNC-E core.

BOM, if DFF not assembled 0 ohm
Otherwise simulate the value

for bypass

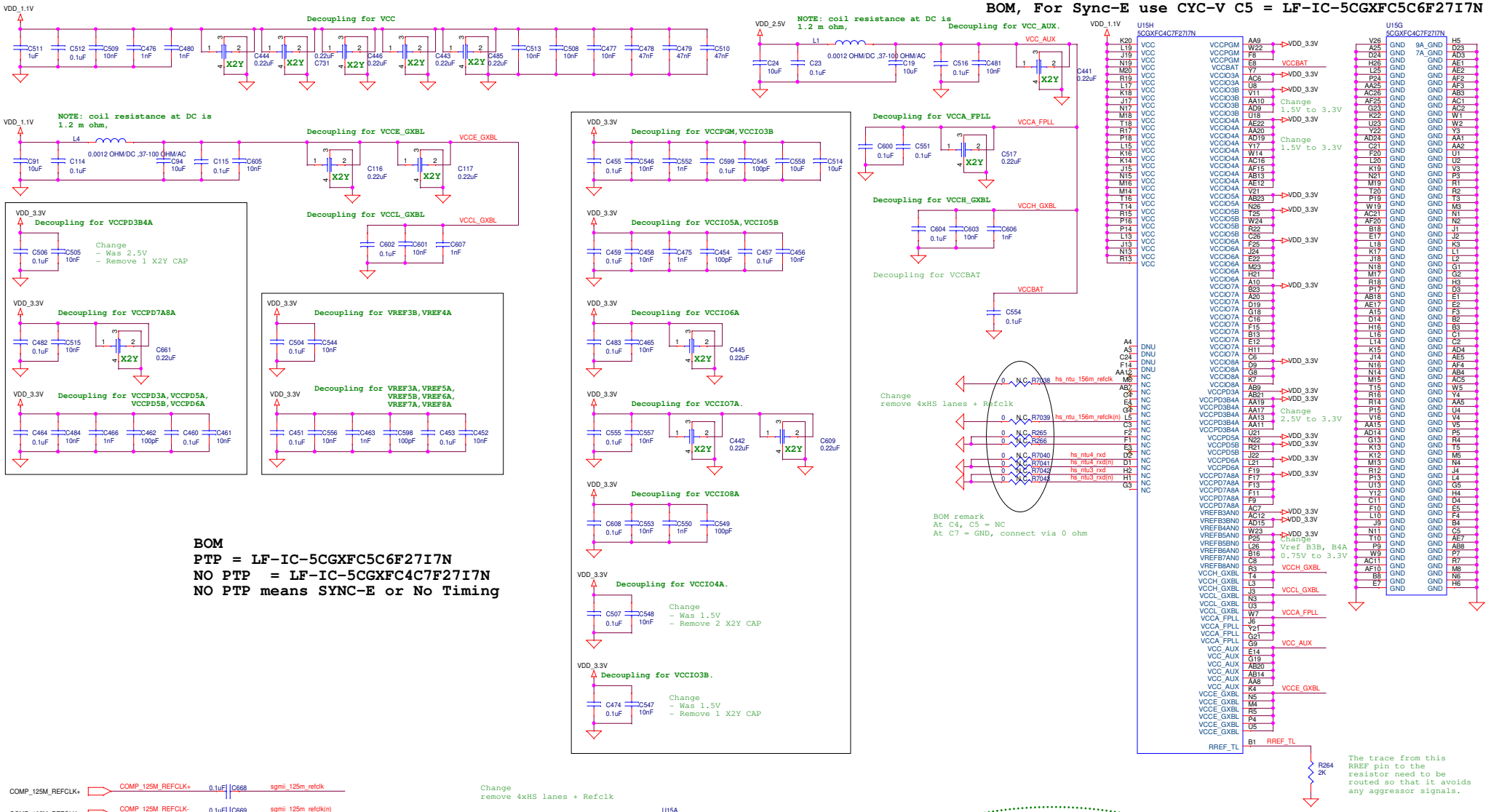
for bypass
place inside chip

DFF Assemble when OCXO/TCXO is 38.88MHz. pin Comp_CLK_HIGH must get 19.44MHz.

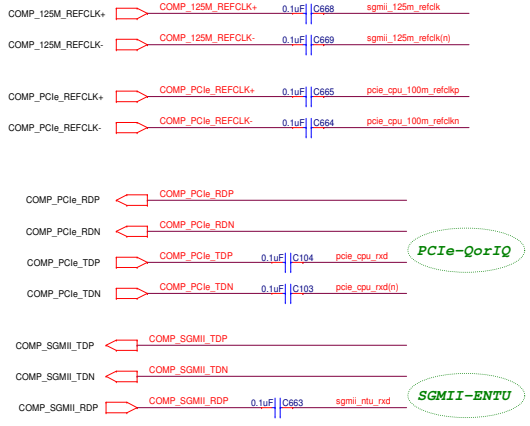
layout wide plane
for VDD_CXO

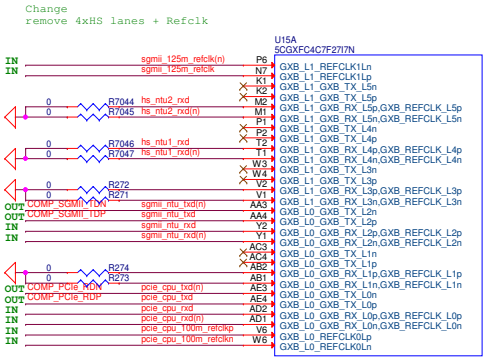
Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications	
Title	Companion FPGA - SYNCLK SYNCE		
Size: D	Design Name : ETX-2I-10G-LC.REV0.2I		Rev: 0.0
Date: Friday, June 17, 2016	Sheet 26 of 46		

BOM, For Sync-E use CYC-V C5 = LF-IC-5CGXFC5C6F27I7N



BOM
PTP = LF-IC-5CGXFC5C6F27I7N
NO PTP = LF-IC-5CGXFC4C7F27I7N
NO PTP means SYNC-E or No Timing

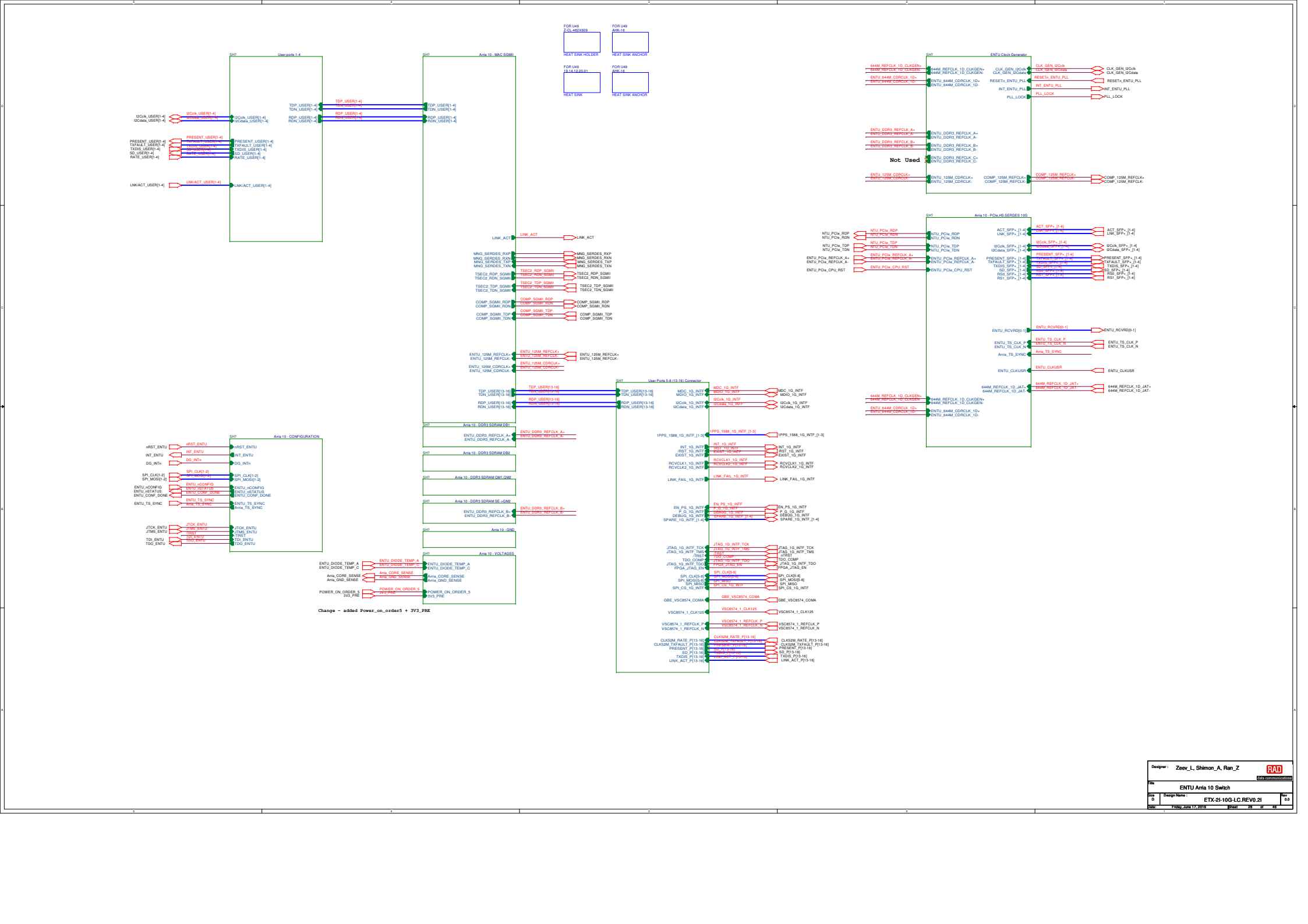


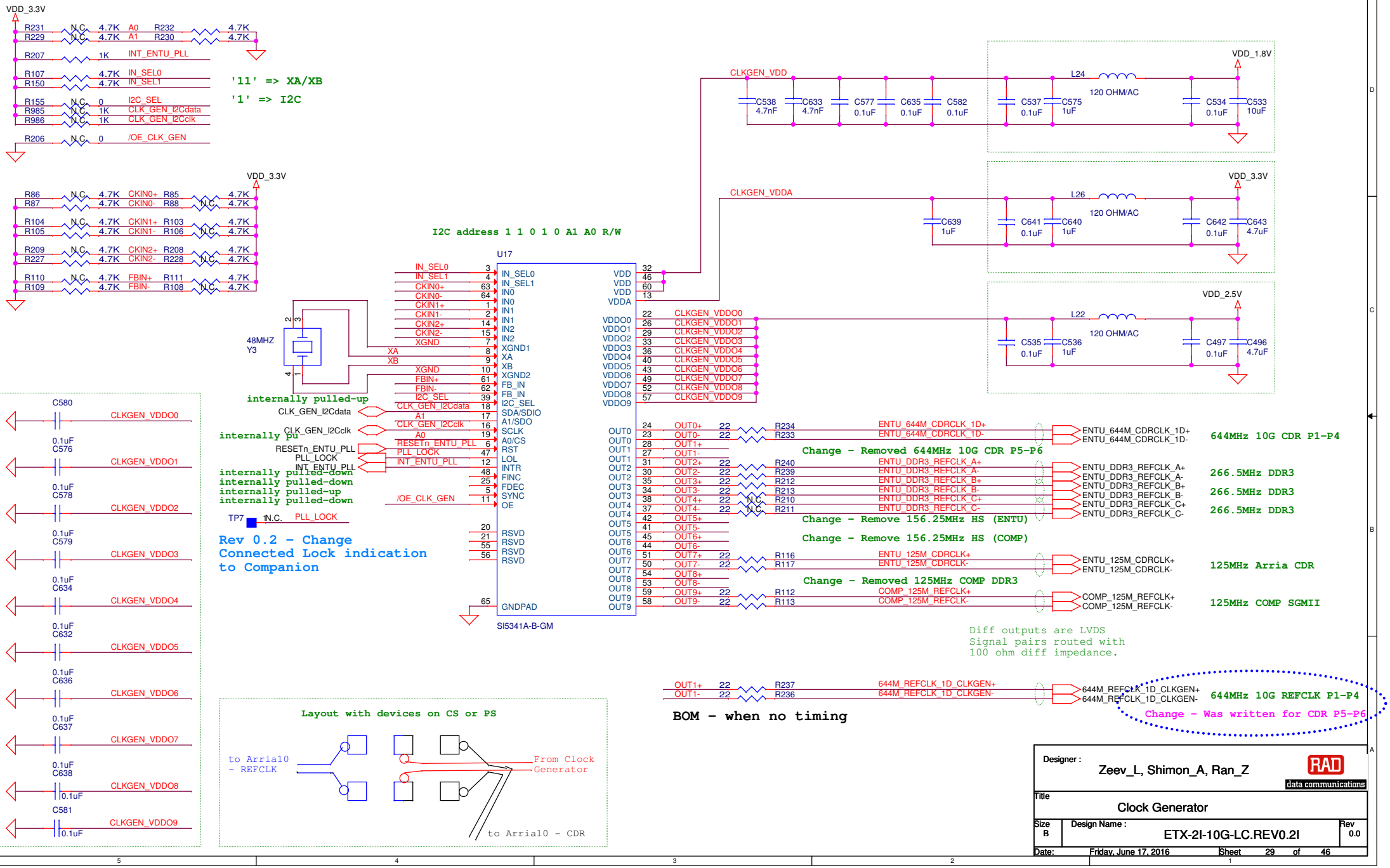


* At Cyclone® V 5CGXFC4 Device SERDES and PLL clock share same pins so, DDR3 device will assemble only with Cyclone® V 5CGXFC7 Device and Cyclone® V 5CGXFC9 Device. in these devices quantity of SERDES are large.

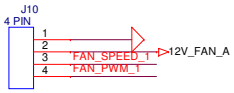
* HS Bus communicate between ENTU and COMPANION. It require x4 lanes. so, another x2 lanes locate on symbol H.

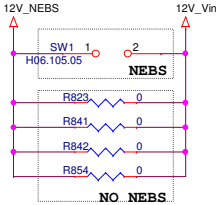
Designer :	Zeev_L, Shimon_A, Ran_Z
Title	Companion FPGA - TRANSCEIVER & POWER
Size	C
Design Name :	ETX-2I-10G-LC.REV0.2I
Rev	0.0
Date:	Friday, June 17, 2016
Sheet	27 of 46


SH? User ports 1-4
SH? Arria 10 - MAC SGMII
SH? ENTU Clock Generator
SH? Arria 10 - PCIe,HS,SERDES 10G
SH? Arria 10 - CONFIGURATION
SH? Arria 10 - DDR3 SDRAM DB1
SH? Arria 10 - DDR3 SDRAM DB2
SH? Arria 10 - DDR3 SDRAM QM1,QM2
SH? Arria 10 - DDR3 SDRAM SE->QM2
SH? Arria 10 - GND
SH? Arria 10 - VOLTAGES
SH? User Ports 5-8 (13-16) Connector
FOR U49 Z-CL-482X609
HEAT SINK HOLDER
FOR U49 AHK-18
HEAT SINK ANCHOR
FOR U49 13,14,12,20,01
HEAT SINK
FOR U49 AHK-18
HEAT SINK ANCHOR
Not Used
Change - added Power_on_order5 + 3V3_PRE
Designer : Zeev_L, Shimon_A, Ran_Z
RAD data communications
Title
ENTU Aria 10 Switch
Size D
Design Name : ETX-2I-10G-LC.REV0.2I
Rev 0.0
Date: Friday, June 17, 2016
Sheet 29 of 46

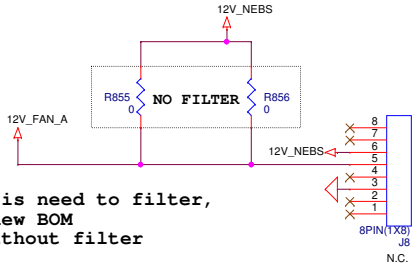

VDD_3.3V
R231 N.C. 4.7K A0 R232 4.7K
R229 N.C. 4.7K A1 R230 4.7K
R207 1K INT_ENTU_PLL
R107 4.7K IN_SEL0
R150 4.7K IN_SEL1
R155 N.C. 0 I2C_SEL
R985 N.C. 1K CLK_GEN_I2Cdata
R986 N.C. 1K CLK_GEN_I2Cclk
R206 N.C. 0 /OE_CLK_GEN
'11' => XA/XB
'1' => I2C
R86 N.C. 4.7K CKIN0+ R85 4.7K
R87 4.7K CKIN0- R88 N.C. 4.7K
R104 N.C. 4.7K CKIN1+ R103 4.7K
R105 4.7K CKIN1- R106 N.C. 4.7K
R209 N.C. 4.7K CKIN2+ R208 4.7K
R227 4.7K CKIN2- R228 N.C. 4.7K
R110 N.C. 4.7K FBIN+ R111 4.7K
R109 4.7K FBIN- R108 N.C. 4.7K
I2C address 1 1 0 1 0 A1 A0 R/W
U17
48MHZ
Y3
XA
XB
internally pulled-up
CLK_GEN_I2Cdata
CLK_GEN_I2Cclk
internally pu
RESETn_ENTU_PLL
PLL_LOCK
INT_ENTU_PLL
internally pulled-down
internally pulled-down
internally pulled-up
internally pulled-down
/OE_CLK_GEN
TP7
N.C.
PLL_LOCK
IN_SEL0 3
IN_SEL1 4
CKIN0+ 63
CKIN0- 64
CKIN1+ 1
CKIN1- 2
CKIN2+ 14
CKIN2- 15
XGND 7
XA 8
XB 9
XGND 10
FBIN+ 61
FBIN- 62
I2C_SEL 39
CLK_GEN_I2Cdata 18
A1 17
CLK_GEN_I2Cclk 16
A0 19
RESETn_ENTU_PLL 6
PLL_LOCK 47
INT_ENTU_PLL 12
48
25
5
/OE_CLK_GEN 11
20
21
55
56
65
IN_SEL0
IN_SEL1
IN0
IN0
IN1
IN1
IN2
IN2
XGND1
XA
XB
XGND2
FB_IN
FB_IN
I2C_SEL
SDA/SDIO
A1/SDO
SCLK
A0/CS
RST
LOL
INTR
FINC
FDEC
SYNC
OE
RSVD
RSVD
RSVD
RSVD
GNDPAD
SI5341A-B-GM
VDD 32
VDD 46
VDD 60
VDDA 13
VDDO0 22
VDDO1 26
VDDO2 29
VDDO3 33
VDDO4 36
VDDO5 40
VDDO6 43
VDDO7 49
VDDO8 52
VDDO9 57
CLKGEN_VDDO0
CLKGEN_VDDO1
CLKGEN_VDDO2
CLKGEN_VDDO3
CLKGEN_VDDO4
CLKGEN_VDDO5
CLKGEN_VDDO6
CLKGEN_VDDO7
CLKGEN_VDDO8
CLKGEN_VDDO9
OUT0 24 OUT0+ 22 R234 ENTU_644M_CDRCLK_1D+ ENTU_644M_CDRCLK_1D+
OUT0 23 OUT0- 22 R233 ENTU_644M_CDRCLK_1D- ENTU_644M_CDRCLK_1D-
644MHz 10G CDR P1-P4
OUT1 28 OUT1+
OUT1 27 OUT1-
Change - Removed 644MHz 10G CDR P5-P6
OUT2 31 OUT2+ 22 R240 ENTU_DDR3_REFCLK_A+ ENTU_DDR3_REFCLK_A+
OUT2 30 OUT2- 22 R239 ENTU_DDR3_REFCLK_A- ENTU_DDR3_REFCLK_A-
266.5MHz DDR3
OUT3 35 OUT3+ 22 R212 ENTU_DDR3_REFCLK_B+ ENTU_DDR3_REFCLK_B+
OUT3 34 OUT3- 22 R213 ENTU_DDR3_REFCLK_B- ENTU_DDR3_REFCLK_B-
266.5MHz DDR3
OUT4 38 OUT4+ 22 N.C. R210 ENTU_DDR3_REFCLK_C+ ENTU_DDR3_REFCLK_C+
OUT4 37 OUT4- 22 N.C. R211 ENTU_DDR3_REFCLK_C- ENTU_DDR3_REFCLK_C-
266.5MHz DDR3
OUT5 42 OUT5+
OUT5 41 OUT5-
Change - Remove 156.25MHz HS (ENTU)
OUT6 45 OUT6+
OUT6 44 OUT6-
Change - Remove 156.25MHz HS (COMP)
OUT7 51 OUT7+ 22 R116 ENTU_125M_CDRCLK+ ENTU_125M_CDRCLK+
OUT7 50 OUT7- 22 R117 ENTU_125M_CDRCLK- ENTU_125M_CDRCLK-
125MHz Arria CDR
OUT8 54 OUT8+
OUT8 53 OUT8-
Change - Removed 125MHz COMP DDR3
OUT9 59 OUT9+ 22 R112 COMP_125M_REFCLK+ COMP_125M_REFCLK+
OUT9 58 OUT9- 22 R113 COMP_125M_REFCLK- COMP_125M_REFCLK-
125MHz COMP SGMII
Diff outputs are LVDS
Signal pairs routed with
100 ohm diff impedance.
OUT1+ 22 R237 644M_REFCLK_1D_CLKGEN+ 644M_REFCLK_1D_CLKGEN+
OUT1- 22 R236 644M_REFCLK_1D_CLKGEN- 644M_REFCLK_1D_CLKGEN-
644MHz 10G REFCLK P1-P4
Change - Was written for CDR P5-P6
BOM - when no timing
CLKGEN_VDD
C538 4.7nF
C633 4.7nF
C577 0.1uF
C635 0.1uF
C582 0.1uF
L24
120 OHM/AC
C537 0.1uF
C575 1uF
C534 0.1uF
C533 10uF
VDD_1.8V
CLKGEN_VDDA
C639 1uF
L26
120 OHM/AC
C641 0.1uF
C640 1uF
C642 0.1uF
C643 4.7uF
VDD_3.3V
VDD_2.5V
L22
120 OHM/AC
C535 0.1uF
C536 1uF
C497 0.1uF
C496 4.7uF
C580 0.1uF CLKGEN_VDDO0
C576 0.1uF CLKGEN_VDDO1
C578 0.1uF CLKGEN_VDDO2
C579 0.1uF CLKGEN_VDDO3
C634 0.1uF CLKGEN_VDDO4
C632 0.1uF CLKGEN_VDDO5
C636 0.1uF CLKGEN_VDDO6
C637 0.1uF CLKGEN_VDDO7
C638 0.1uF CLKGEN_VDDO8
C581 0.1uF CLKGEN_VDDO9
Rev 0.2 - Change
Connected Lock indication
to Companion
Layout with devices on CS or PS
to Arria10
- REFCLK
From Clock
Generator
to Arria10 - CDR
Designer :
Zeev_L, Shimon_A, Ran_Z
RAD
data communications
Title
Clock Generator
Size
B
Design Name :
ETX-2I-10G-LC.REV0.2I
Rev
0.0
Date:
Friday, June 17, 2016
Sheet
29
of
46

UP SIDE





FAN FILTER CONNECTOR

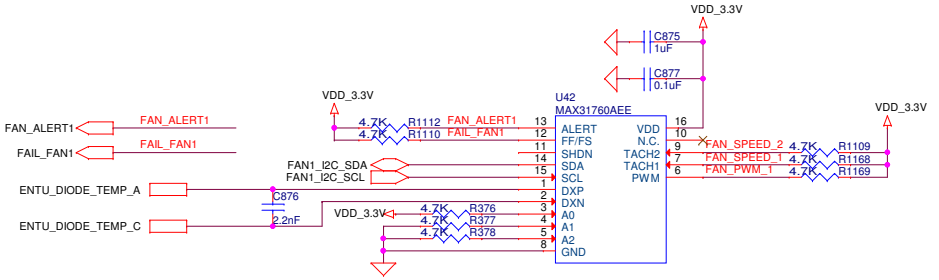


If there is need to filter,
prepare new BOM
with / without filter

For now no filter resistor
always assemble

If filter is needed Assemble special filter 12V-FAN-SIP

Fan Controlers

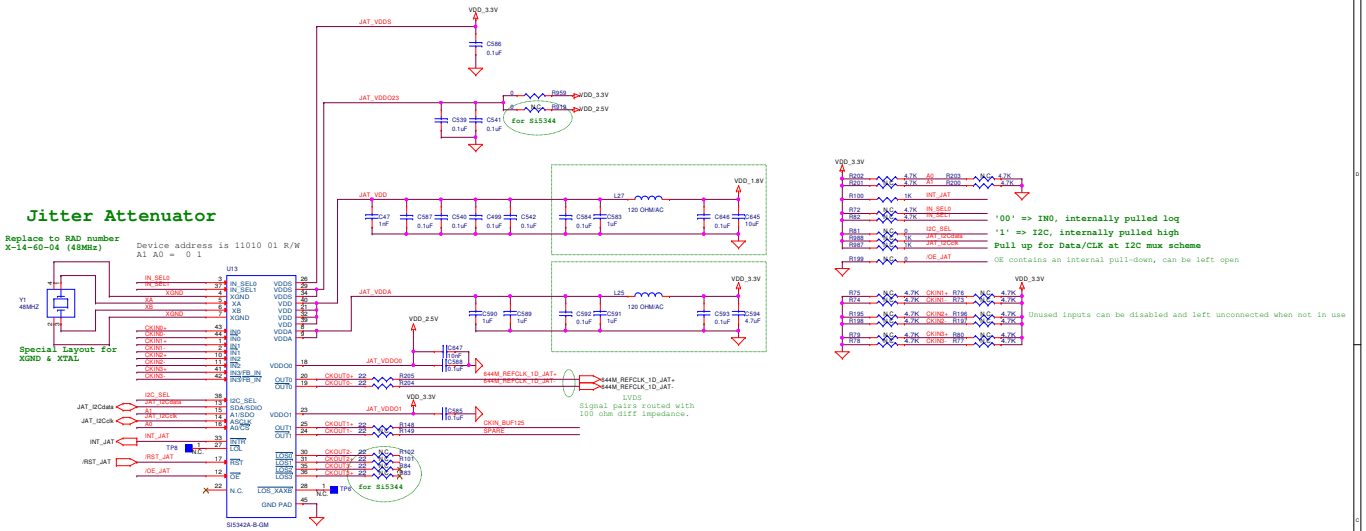


Device address is 1010 001 R/W
A2 A1 A0 = 0 0 1

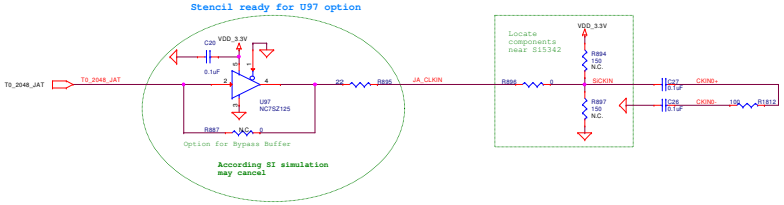
Designer : Zeev_L, Shimon_A, Ran_Z			RAD data communications
Title: Fan Controlers			
Size: Custom	Design Name : ETX-2I-10G-LC.REV0.2I		Rev: 0.0
Date: Friday, June 17, 2016	Sheet 30 of 46		

REV 0.2 Change
Removing not used 48MHZ oscillator and semi planes

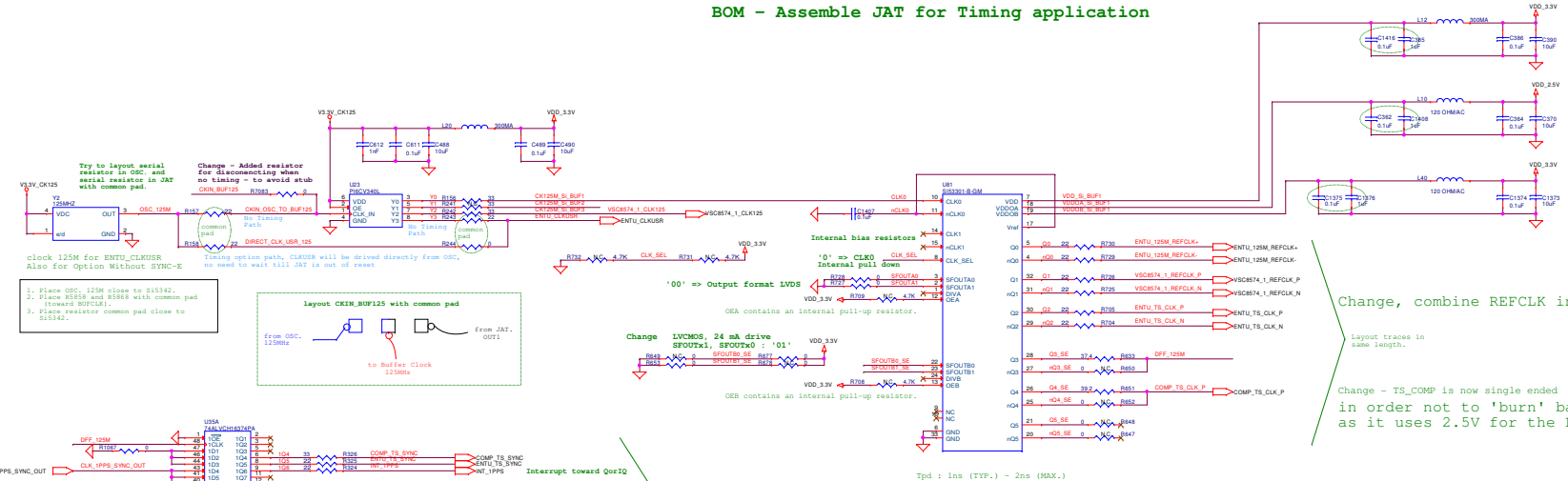
Jitter Attenuator

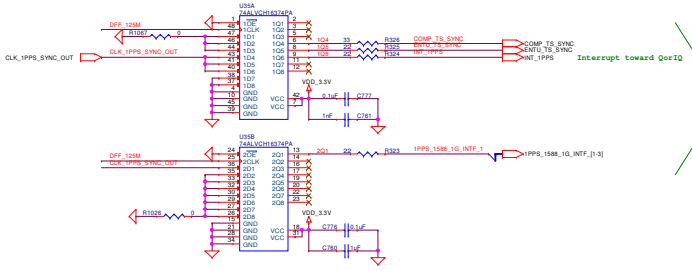


Stencil ready for U97 option



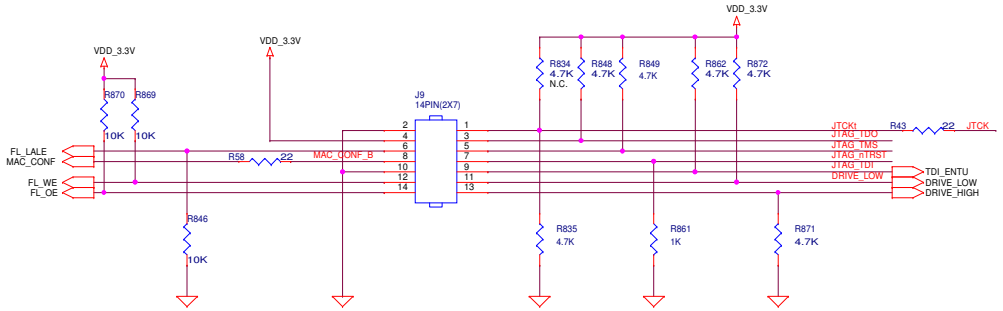
BOM – Assemble JAT for Timing application

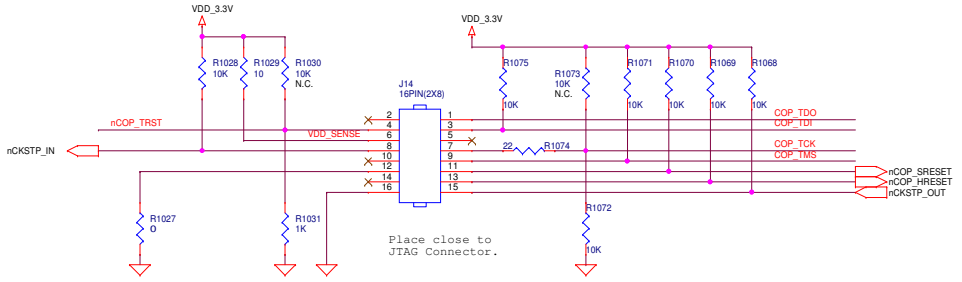


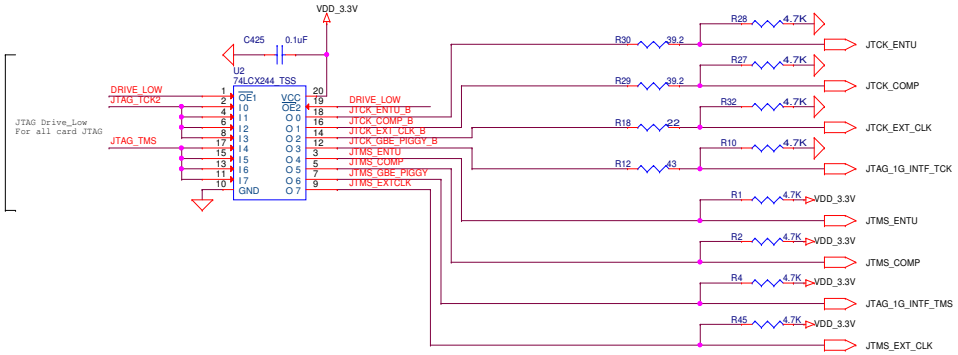


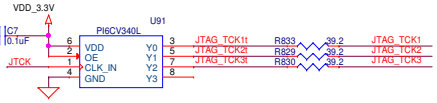
BOM – Assemble 1PPS buffer for Timing application

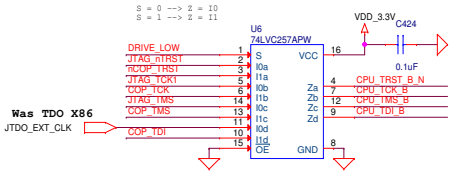
Designer :	Zeev_L, Shimon_A, Ran_Z
Title	Jitter Attenuator
Size: D	Design Name : ETX-2I-10G-LC.REV0.2I
Rev: 0.0	
Date: Friday, June 17, 2016	Sheet 31 of 46

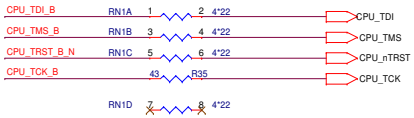


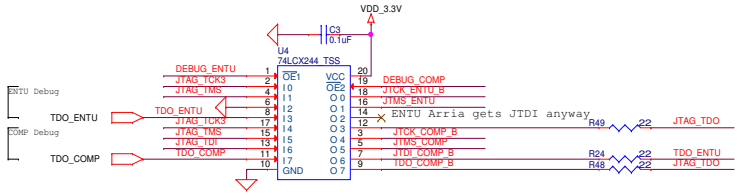


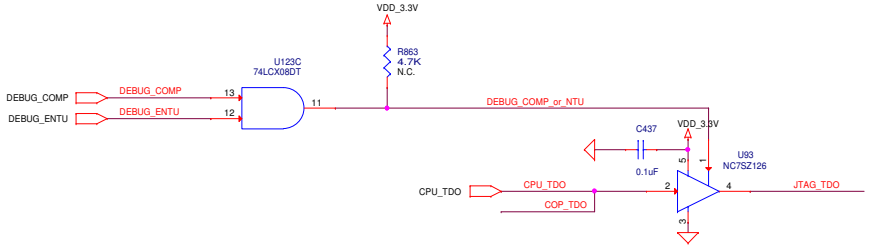


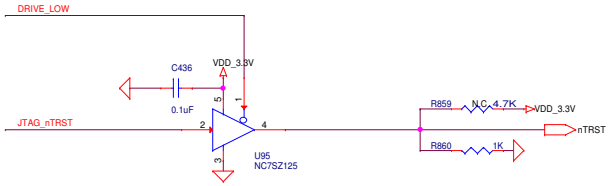


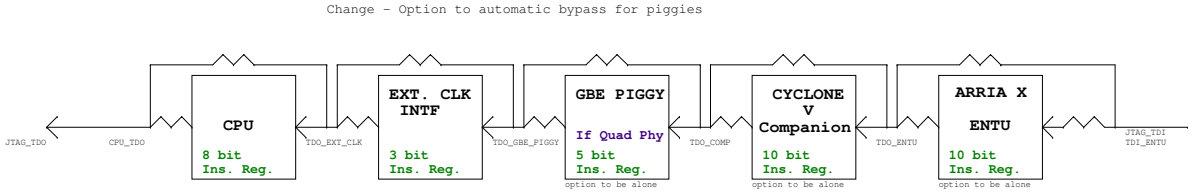




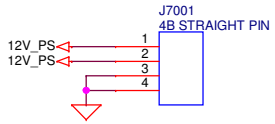


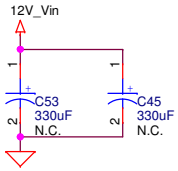




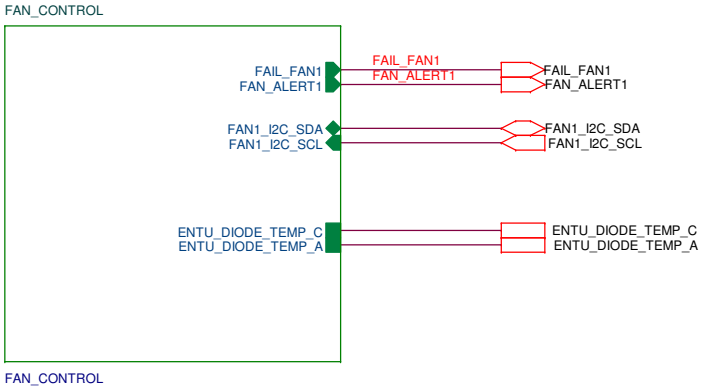


Designer : Zeev_L, Shimon_A, Ran_Z			RAD data communications
Title: 09_JTAG_and_COP			
Size: C	Design Name : ETX-2I-10G-LC.REV0.2I		Rev: 0.0
Date: Friday, June 17, 2016	Sheet 32 of 46		

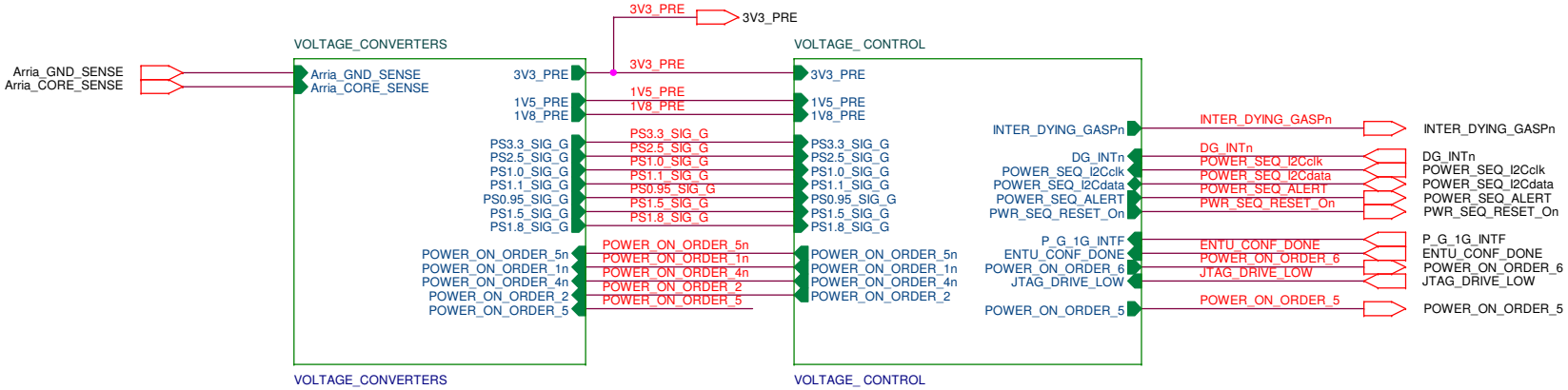




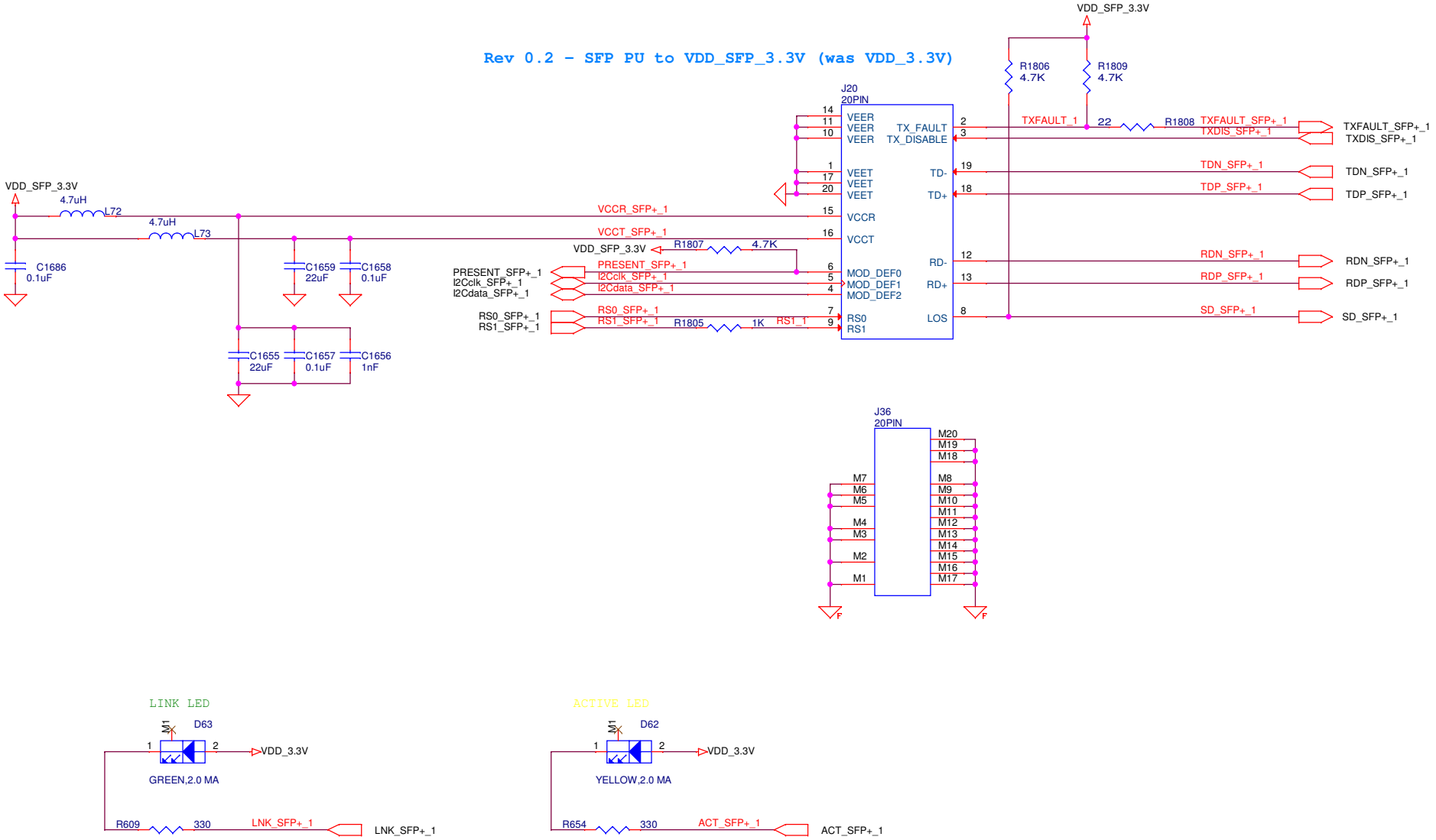
No need for cap is enough (in terms of PI and 12V PS simulation)



Change - Added for Arria DDR VTT termination

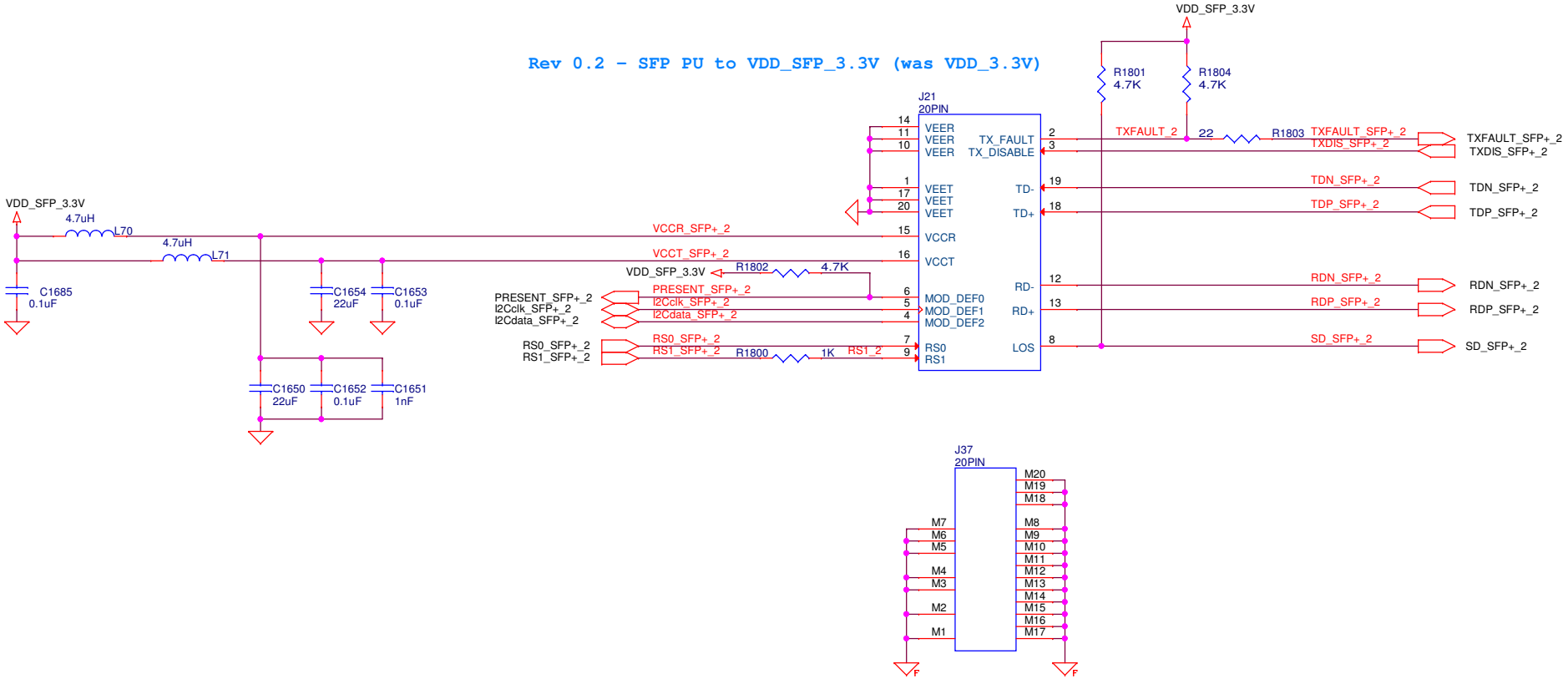


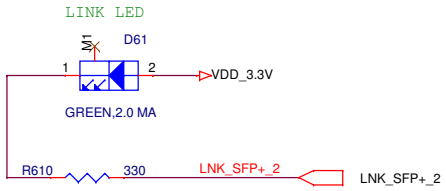
Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications
Title	MAIN POWER	
Size B	Design Name : ETX-2I-10G-LC.REV0.2I	Rev 0.0
Date: Friday, June 17, 2016	Sheet 33 of 46	

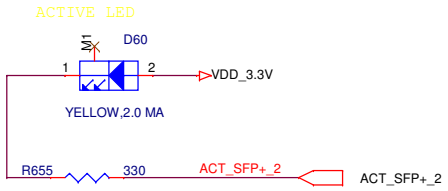


Designer :	Zeev_L, Shimon_A, Ran_Z		
Title	SFP+ - Port 1		
Size B	Design Name : ETX-2I-10G-LC.REV0.2I		Rev 0.0
Date: Friday, June 17, 2016	Sheet 34 of 46		

Rev 0.2 – SFP PU to VDD_SFP_3.3V (was VDD_3.3V)



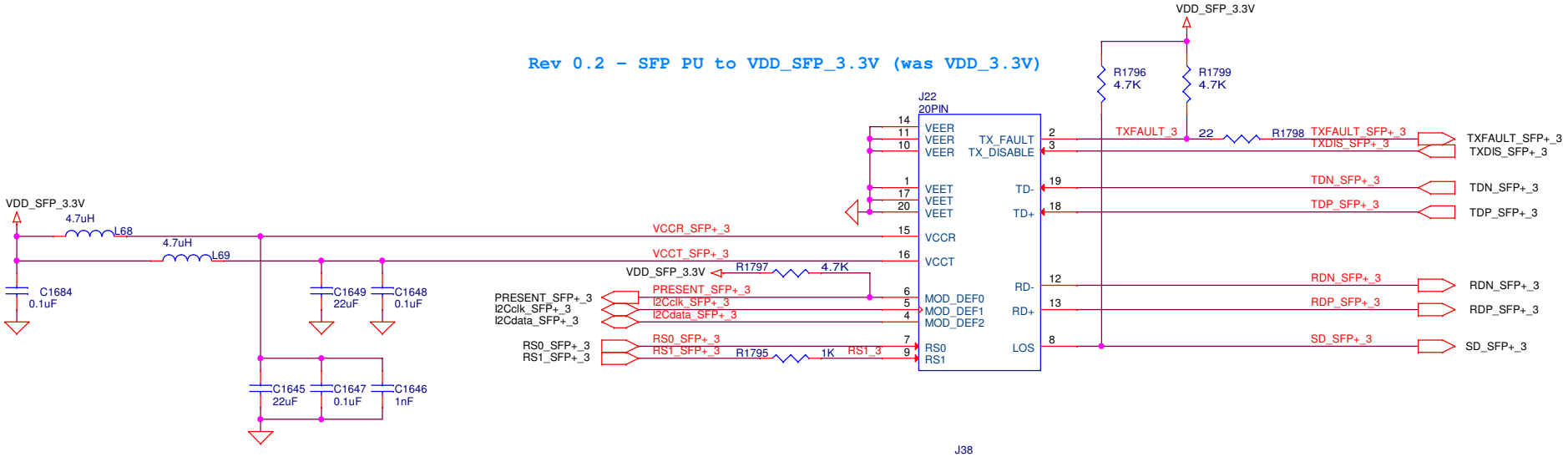


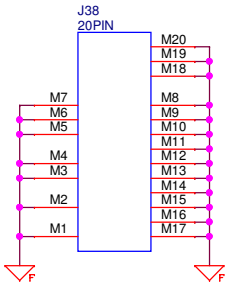


LNK and ACT derived From Arria 10

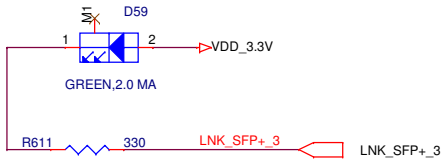
Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications	
Title	SFP+ - Port 2		
Size B	Design Name : ETX-2I-10G-LC.REV0.2I		Rev 0.0
Date: Friday, June 17, 2016	Sheet 35 of 46		

Rev 0.2 – SFP PU to VDD_SFP_3.3V (was VDD_3.3V)

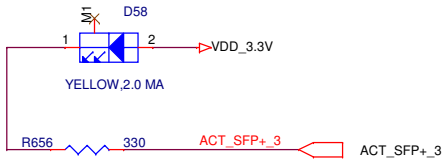




LINK LED



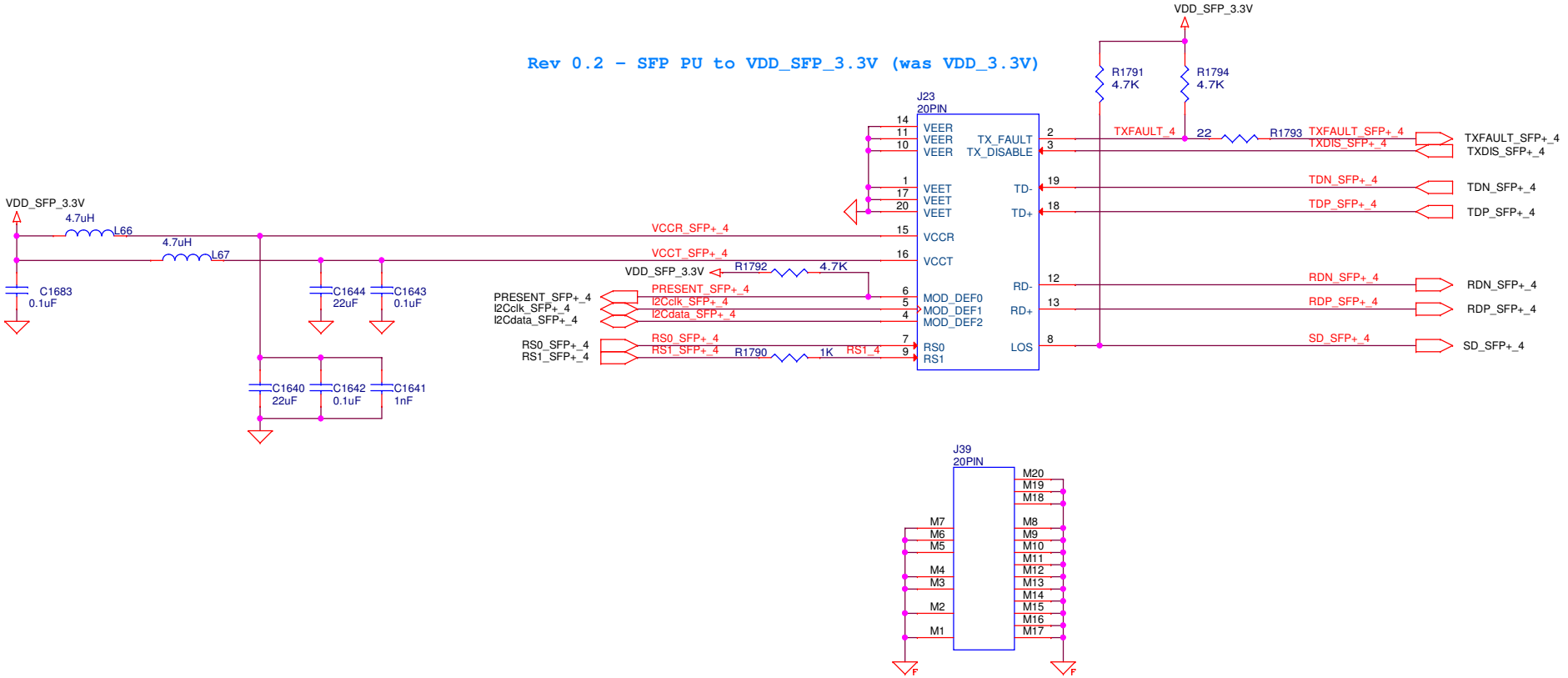
ACTIVE LED

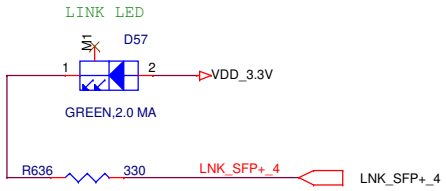


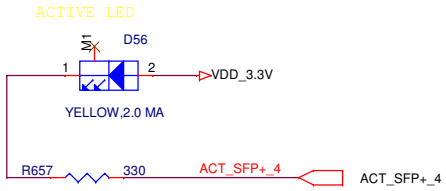
LNK and ACT derived From Arria 10

Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications	
Title	SFP+ - Port 3		
Size B	Design Name : ETX-2I-10G-LC.REV0.2I		Rev 0.0
Date: Friday, June 17, 2016	Sheet 36 of 46		

Rev 0.2 – SFP PU to VDD_SFP_3.3V (was VDD_3.3V)



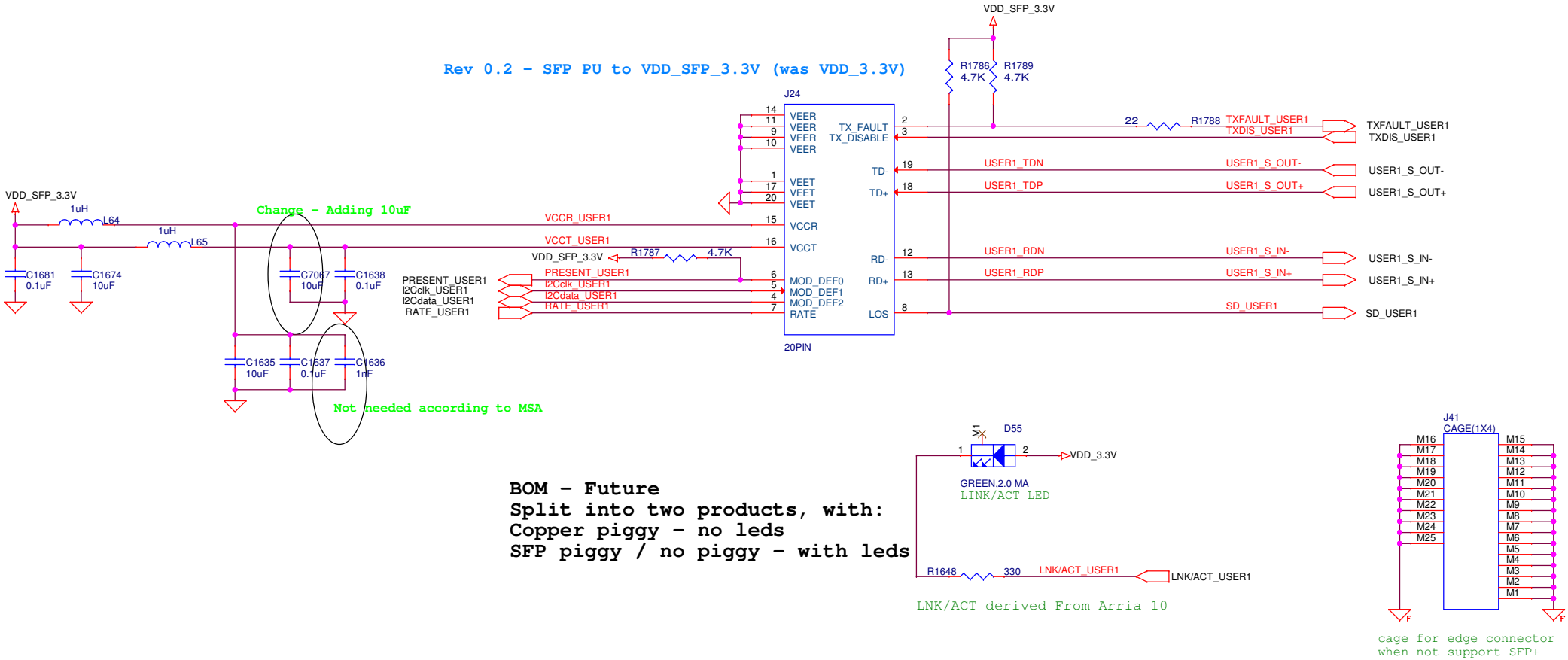




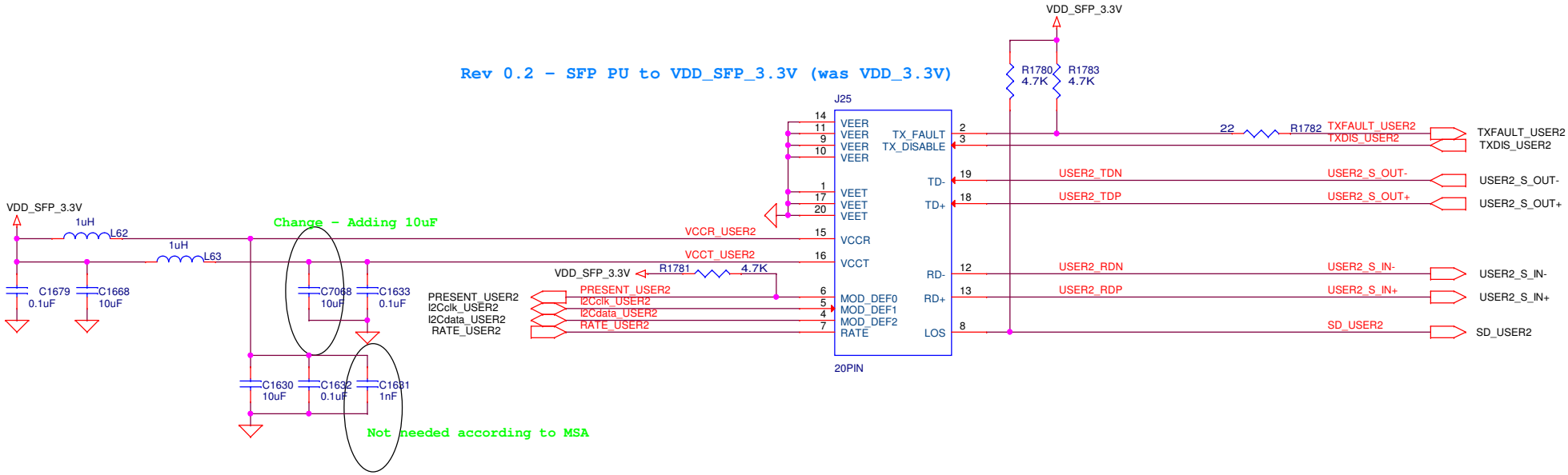
LNK and ACT derived From Arria 10

Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications	
Title	SFP+ - Port 4		
Size B	Design Name : ETX-2I-10G-LC.REV0.2I		Rev 0.0
Date: Friday, June 17, 2016	Sheet 37 of 46		

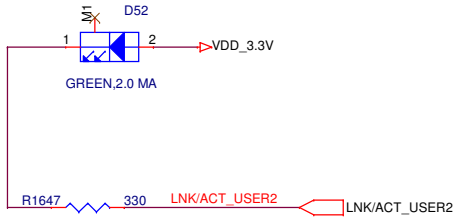

new mean that need to add signal in GP FPGA
SH53
Jitter Attenuator
SH50
Companion FPGA - SYNCLK SYNCE
SH52
Companion FPGA - TRANS & POWER
SH51
Companion FPGA - DDR3
Change - ENTU_TS_CLK_N removed - now is is S.E.
FOR U15
BDN12-5CB/A01
HEAT SINK
Designer : Zeev_L, Shimon_A, Ran_Z
data communications
Title
Synchronous Ethernet
Size C
Design Name : ETX-2I-10G-LC.REV0.2I
Rev 0.0
Date: Friday, June 17, 2016
Sheet 38 of 46



Designer :	Zeev_L, Shimon_A, Ran_Z		
Title	User Magnetic - Port 1		
Size B	Design Name : ETX-2I-10G-LC.REV0.2I		Rev 0.0
Date: Friday, June 17, 2016	Sheet 39 of 46		

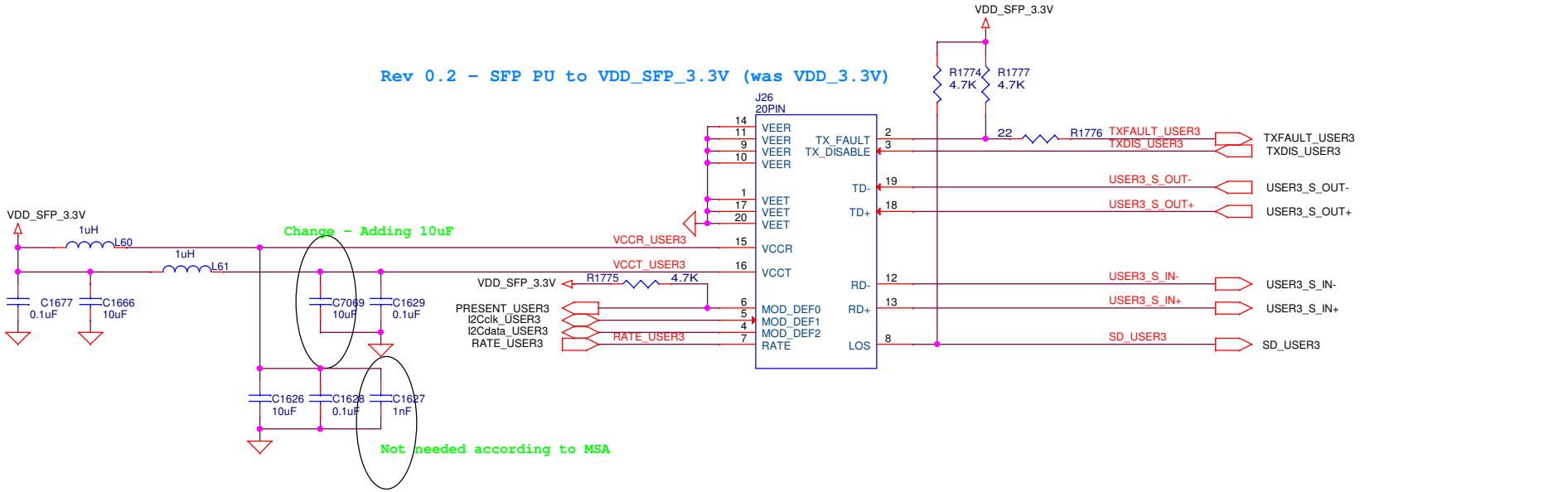


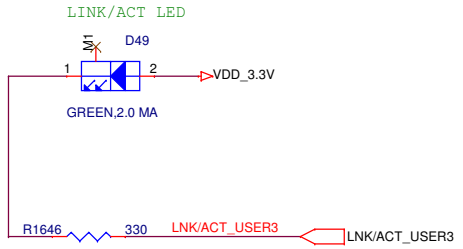
BOM – Future
Split into two products, with:
Copper piggy – no leds
SFP piggy / no piggy – with leds



LNK/ACT derived From Arria 10

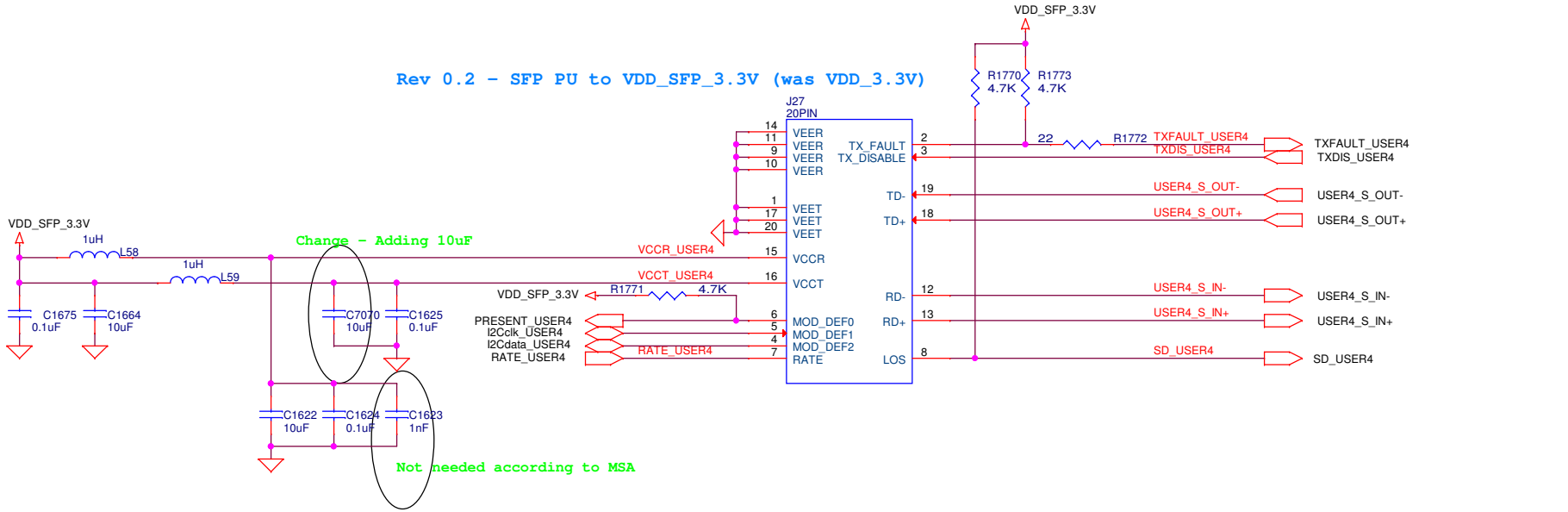
Designer : Zeev_L, Shimon_A, Ran_Z		RAD data communications
Title: User Magnetic - Port 2		
Size: B	Design Name : ETX-2I-10G-LC.REV0.2I	Rev: 0.0
Date: Friday, June 17, 2016	Sheet 40 of 46	

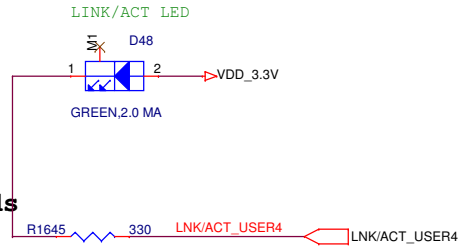




LNK/ACT derived From Arria 10

Designer : Zeev_L, Shimon_A, Ran_Z			
Title: User Magnetic - Port 3			
Size: B	Design Name : ETX-2I-10G-LC.REV0.2I		Rev: 0.0
Date: Friday, June 17, 2016	Sheet 41 of 46		



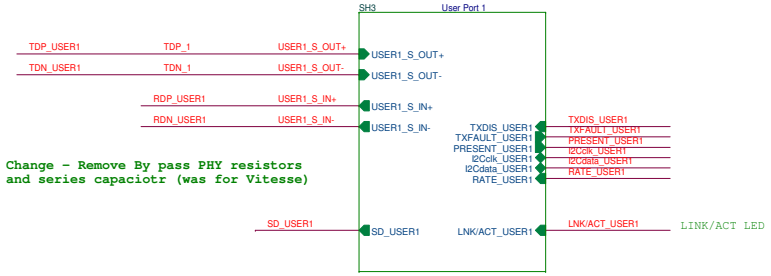


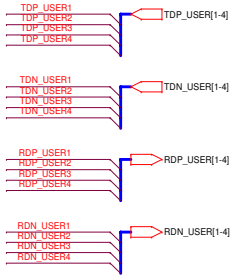
BOM – Future
Split into two products, with:
Copper piggy – no leds
SFP piggy / no piggy – with leds

LNK/ACT derived From Arria 10

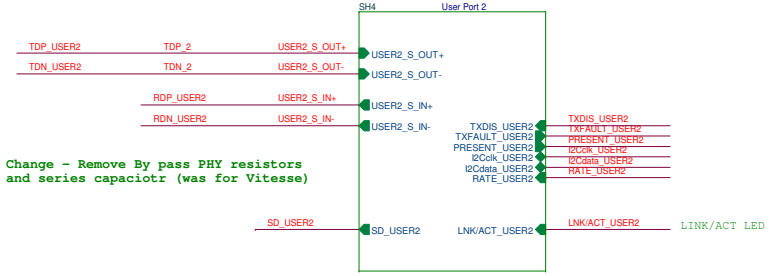
Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications
Title	User Magnetic - Port 4	
Size B	Design Name : ETX-2I-10G-LC.REV0.2I	Rev 0.0
Date: Friday, June 17, 2016	Sheet 42 of 46	

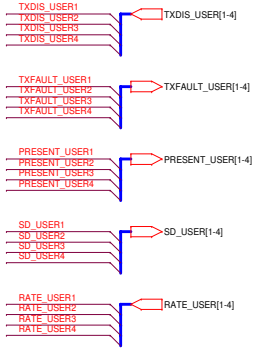
PORT 1 in the panel



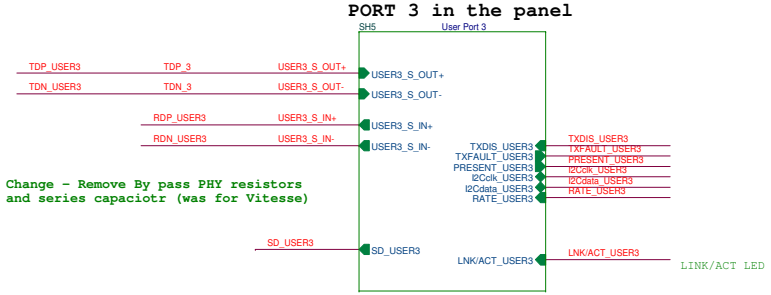


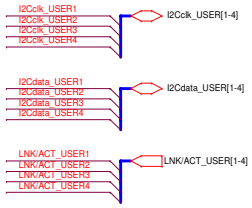
PORT 2 in the panel



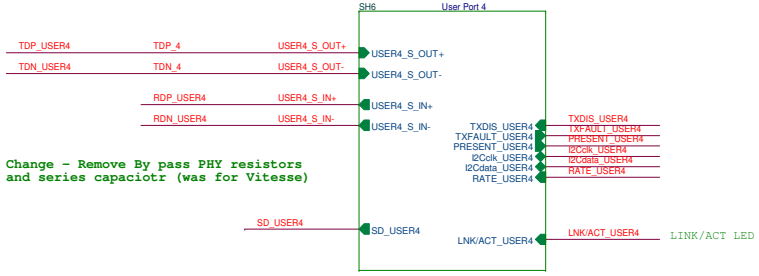


PORT 3 in the panel

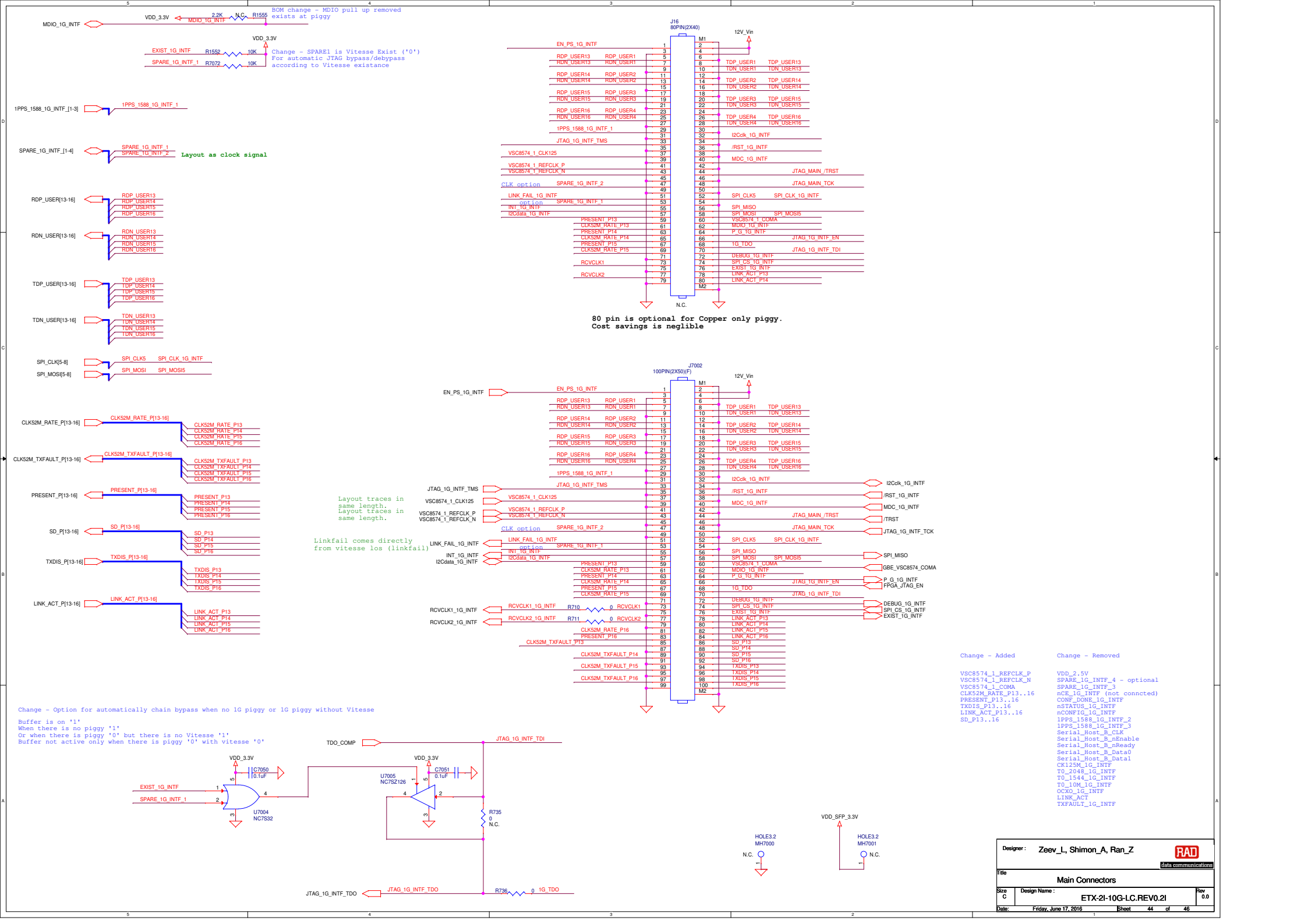


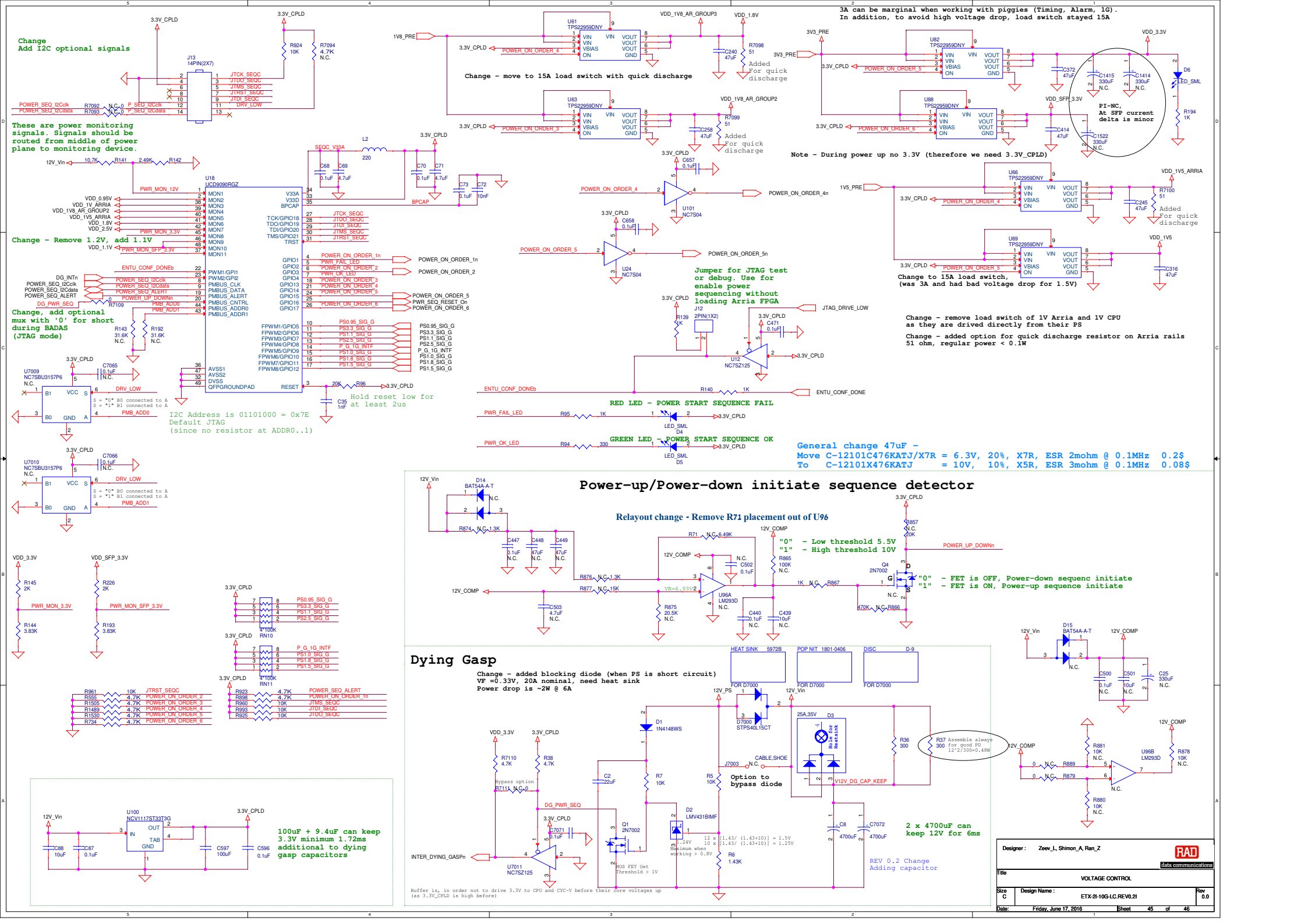


PORT 4 in the panel



Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications	
Title	VSC8574 - User ports 1-4		
Size C	Design Name : ETX-2I-10G-LC.REV0.2I		Rev 0.0
Date:	Friday, June 17, 2016	Sheet 43 of 46	


MDIO_1G_INTF
VDD_3.3V
2.2K
N.C.
R1555
MDIO_1G_INTF
BOM change - MDIO pull up removed exists at piggy
VDD_3.3V
EXIST_1G_INTF
R1552
10K
SPARE_1G_INTF_1
R7072
10K
Change - SPARE1 is Vitesse Exist ('0')
For automatic JTAG bypass/debypass
according to Vitesse existance
1PPS_1588_1G_INTF_[1-3]
1PPS_1588_1G_INTF_1
SPARE_1G_INTF_[1-4]
SPARE_1G_INTF_1
SPARE_1G_INTF_2
Layout as clock signal
RDP_USER[13-16]
RDP_USER13
RDP_USER14
RDP_USER15
RDP_USER16
RDN_USER[13-16]
RDN_USER13
RDN_USER14
RDN_USER15
RDN_USER16
TDP_USER[13-16]
TDP_USER13
TDP_USER14
TDP_USER15
TDP_USER16
TDN_USER[13-16]
TDN_USER13
TDN_USER14
TDN_USER15
TDN_USER16
SPI_CLK[5-8]
SPI_CLK5
SPI_CLK_1G_INTF
SPI_MOSI[5-8]
SPI_MOSI
SPI_MOSI5
CLK52M_RATE_P[13-16]
CLK52M_RATE_P13
CLK52M_RATE_P14
CLK52M_RATE_P15
CLK52M_RATE_P16
CLK52M_TXFAULT_P[13-16]
CLK52M_TXFAULT_P13
CLK52M_TXFAULT_P14
CLK52M_TXFAULT_P15
CLK52M_TXFAULT_P16
PRESENT_P[13-16]
PRESENT_P13
PRESENT_P14
PRESENT_P15
PRESENT_P16
SD_P[13-16]
SD_P13
SD_P14
SD_P15
SD_P16
TXDIS_P[13-16]
TXDIS_P13
TXDIS_P14
TXDIS_P15
TXDIS_P16
LINK_ACT_P[13-16]
LINK_ACT_P13
LINK_ACT_P14
LINK_ACT_P15
LINK_ACT_P16
J16
80PIN(2X40)
12V_Vin
M1
EN_PS_1G_INTF
RDP_USER13
RDN_USER13
RDP_USER1
RDN_USER1
RDP_USER14
RDN_USER14
RDP_USER2
RDN_USER2
RDP_USER15
RDN_USER15
RDP_USER3
RDN_USER3
RDP_USER16
RDN_USER16
RDP_USER4
RDN_USER4
1PPS_1588_1G_INTF_1
JTAG_1G_INTF_TMS
VSC8574_1_CLK125
VSC8574_1_REFCLK_P
VSC8574_1_REFCLK_N
CLK option
SPARE_1G_INTF_2
LINK_FAIL_1G_INTF
option
SPARE_1G_INTF_1
INT_1G_INTF
I2Cdata_1G_INTF
PRESENT_P13
CLK52M_RATE_P13
PRESENT_P14
CLK52M_RATE_P14
PRESENT_P15
CLK52M_RATE_P15
RCVCLK1
RCVCLK2
TDP_USER1
TDN_USER1
TDP_USER13
TDN_USER13
TDP_USER2
TDN_USER2
TDP_USER14
TDN_USER14
TDP_USER3
TDN_USER3
TDP_USER15
TDN_USER15
TDP_USER4
TDN_USER4
TDP_USER16
TDN_USER16
I2Cclk_1G_INTF
/RST_1G_INTF
MDC_1G_INTF
JTAG_MAIN_/TRST
JTAG_MAIN_TCK
SPI_CLK5
SPI_CLK_1G_INTF
SPI_MISO
SPI_MOSI
SPI_MOSI5
VSC8574_1_COMA
MDIO_1G_INTF
P_G_1G_INTF
JTAG_1G_INTF_EN
1G_TDO
JTAG_1G_INTF_TDI
DEBUG_1G_INTF
SPI_CS_1G_INTF
EXIST_1G_INTF
LINK_ACT_P13
LINK_ACT_P14
M2
N.C.
80 pin is optional for Copper only piggy.
Cost savings is neglible
J7002
100PIN(2X50)(F)
Layout traces in same length.
Layout traces in same length.
Linkfail comes directly from vitesse los (linkfail)
R710
R711
0
RCVCLK1
RCVCLK2
LINK_ACT_P16
SD_P13
SD_P14
SD_P15
SD_P16
CLK52M_TXFAULT_P13
CLK52M_TXFAULT_P14
CLK52M_TXFAULT_P15
CLK52M_TXFAULT_P16
I2Cclk_1G_INTF
/RST_1G_INTF
MDC_1G_INTF
/TRST
JTAG_1G_INTF_TCK
SPI_MISO
GBE_VSC8574_COMA
P_G_1G_INTF
FPGA_JTAG_EN
JTAG_1G_INTF_EN
JTAG_1G_INTF_TDI
DEBUG_1G_INTF
SPI_CS_1G_INTF
EXIST_1G_INTF
Change - Added
VSC8574_1_REFCLK_P
VSC8574_1_REFCLK_N
VSC8574_1_COMA
CLK52M_RATE_P13..16
PRESENT_P13..16
TXDIS_P13..16
LINK_ACT_P13..16
SD_P13..16
Change - Removed
VDD_2.5V
SPARE_1G_INTF_4 - optional
SPARE_1G_INTF_3
nCE_1G_INTF (not connected)
CONF_DONE_1G_INTF
nSTATUS_1G_INTF
nCONFIG_1G_INTF
1PPS_1588_1G_INTF_2
1PPS_1588_1G_INTF_3
Serial_Host_B_CLK
Serial_Host_B_nEnable
Serial_Host_B_nReady
Serial_Host_B_Data0
Serial_Host_B_Data1
CK125M_1G_INTF
T0_2048_1G_INTF
T0_1544_1G_INTF
T0_10M_1G_INTF
OCXO_1G_INTF
LINK_ACT
TXFAULT_1G_INTF
Change - Option for automatically chain bypass when no 1G piggy or 1G piggy without Vitesse
Buffer is on '1'
When there is no piggy '1'
Or when there is piggy '0' but there is no Vitesse '1'
Buffer not active only when there is piggy '0' with vitesse '0'
TDO_COMP
JTAG_1G_INTF_TDI
VDD_3.3V
C7050
0.1uF
EXIST_1G_INTF
SPARE_1G_INTF_1
U7004
NC7S32
U7005
NC7S2126
C7051
0.1uF
R735
0
N.C.
JTAG_1G_INTF_TDO
R736
0
1G_TDO
HOLE3.2
MH7000
N.C.
VDD_SFP_3.3V
HOLE3.2
MH7001
N.C.
Designer : Zeev_L, Shimon_A, Ran_Z
RAD
data communications
Title
Main Connectors
Size C
Design Name : ETX-2I-10G-LC.REV0.2I
Rev 0.0
Date: Friday, June 17, 2016
Sheet 44 of 46


Change
Add I2C optional signals
These are power monitoring signals. Signals should be routed from middle of power plane to monitoring device.
Change - Remove 1.2V, add 1.1V
Change, add optional mux with '0' for short during BADAS (JTAG mode)
I2C Address is 01101000 = 0x7E
Default JTAG
(since no resistor at ADDR0..1)
Hold reset low for at least 2us
Change - move to 15A load switch with quick discharge
Added For quick discharge
3A can be marginal when working with piggies (Timing, Alarm, 1G).
In addition, to avoid high voltage drop, load switch stayed 15A
PI-NC, At SFP current delta is minor
Note - During power up no 3.3V (therefore we need 3.3V_CPLD)
Change to 15A load switch, (was 3A and had bad voltage drop for 1.5V)
Jumper for JTAG test or debug. Use for enable power sequencing without loading Arria FPGA
Change - remove load switch of 1V Arria and 1V CPU as they are drived directly from their PS
Change - added option for quick discharge resistor on Arria rails 51 ohm, regular power < 0.1W
RED LED - POWER START SEQUENCE FAIL
GREEN LED - POWER START SEQUENCE OK
General change 47uF -
Move C-12101C476KATJ/X7R = 6.3V, 20%, X7R, ESR 2mohm @ 0.1MHz 0.2$
To C-12101X476KATJ = 10V, 10%, X5R, ESR 3mohm @ 0.1MHz 0.08$
Power-up/Power-down initiate sequence detector
Relayout change - Remove R71 placement out of U96
"0" - Low threshold 5.5V
"1" - High threshold 10V
"0" - FET is OFF, Power-down sequenc initiate
"1" - FET is ON, Power-up sequence initiate
Dying Gasp
Change - added blocking diode (when PS is short circuit)
VF =0.33V, 20A nominal, need heat sink
Power drop is ~2W @ 6A
Option to bypass diode
2 x 4700uF can keep 12V for 6ms
REV 0.2 Change
Adding capacitor
100uF + 9.4uF can keep 3.3V minimum 1.72ms additional to dying gasp capacitors
Designer : Zeev_L, Shimon_A, Ran_Z
data communications
Title
VOLTAGE CONTROL
Size C
Design Name : ETX-2I-10G-LC.REV0.2I
Rev 0.0
Date: Friday, June 17, 2016
Sheet 45 of 46

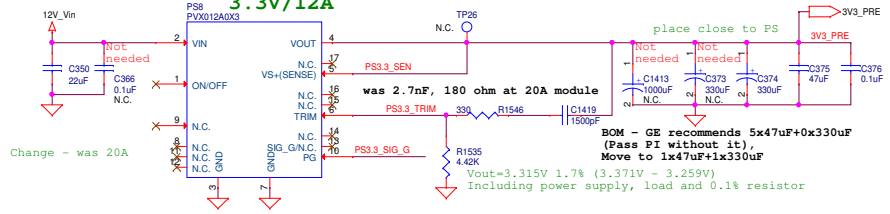
Change - Remove 1.2V (was for GP FPGA)

Main board max consumption 9A, Calculated with 9.5A, 50mV delta, 3A delta

Main board max consumption ~6A
1G Piggy up to 1.8A (in case of 4x1.5W MiRIC)
Timing piggy 0.75A (up to 1.35A during OCXO warm up)
Alarm piggy 0.2A

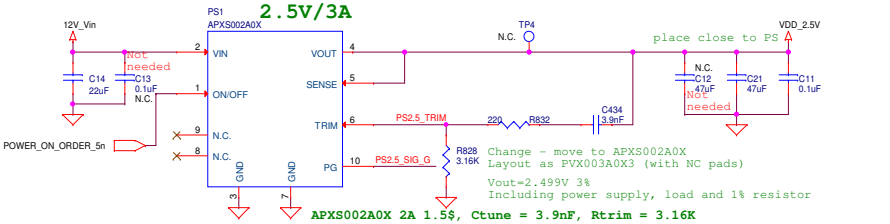
No Piggy - Simulation, Max 6A, 50mV delta, 2A delta
With Piggy - Simulation, Max 9A, 50mV delta, 3A delta

3.3V/12A



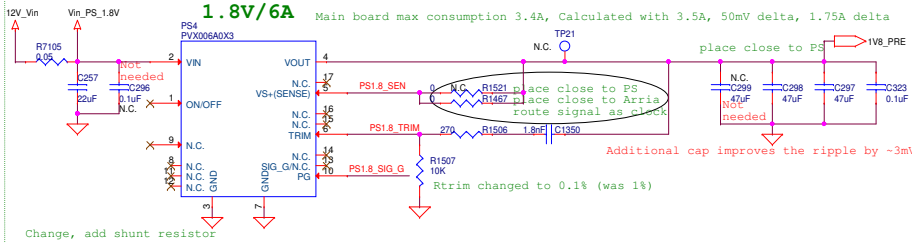
Main board max consumption 0.8A, Calculated with 1.2A, 50mV delta, 0.7A delta

2.5V/3A



1.8V/6A

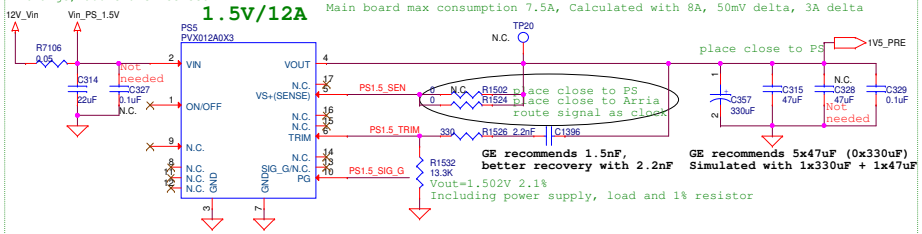
Main board max consumption 3.4A, Calculated with 3.5A, 50mV delta, 1.75A delta



Change, add shunt resistor

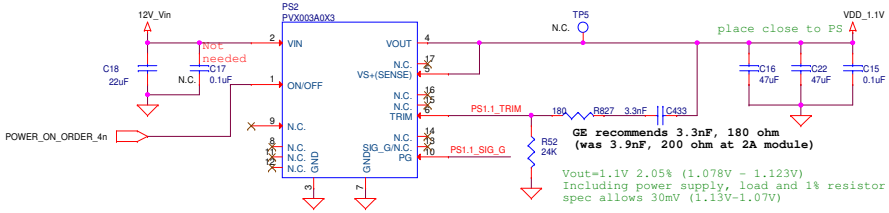
1.5V/12A

Main board max consumption 7.5A, Calculated with 8A, 50mV delta, 3A delta



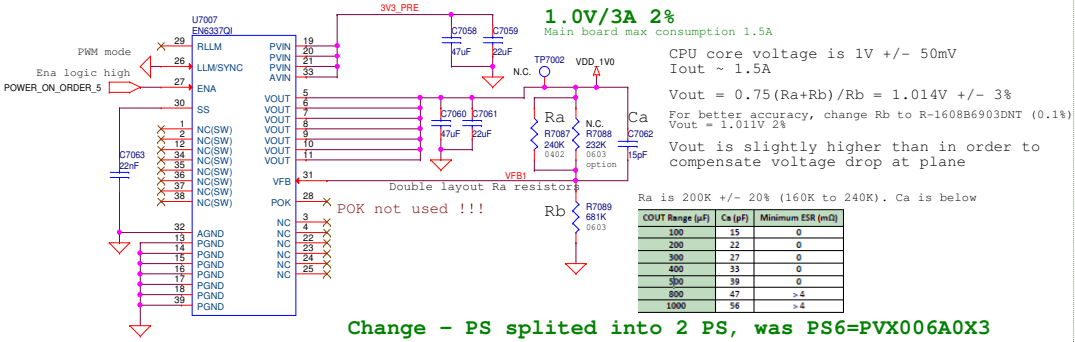
1.1V/3A

Main board max consumption ~2A, Calculated with 2.1A, 30mV delta, 1A delta



1.0V/3A 2%

Main board max consumption 1.5A

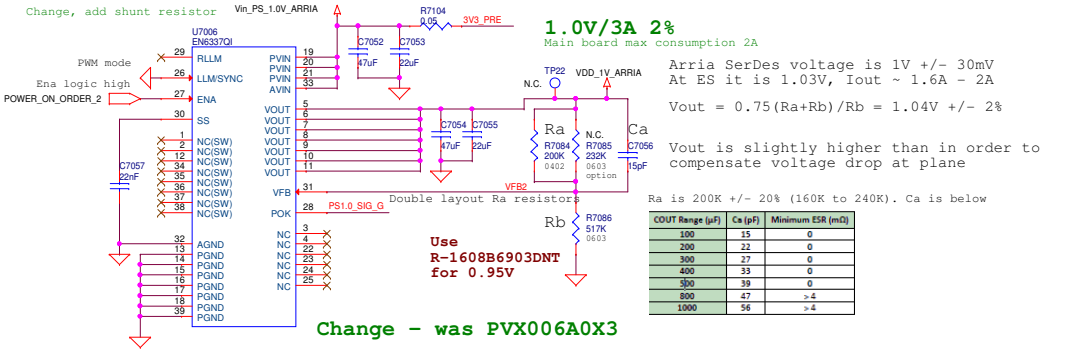


COUT Range (µF)	Ca (pF)	Minimum ESR (mΩ)
100	15	0
200	22	0
300	27	0
400	33	0
500	39	0
800	47	>4
1000	56	>4

Change - PS splited into 2 PS, was PS6=PVX006A0X3

1.0V/3A 2%

Main board max consumption 2A



COUT Range (µF)	Ca (pF)	Minimum ESR (mΩ)
100	15	0
200	22	0
300	27	0
400	33	0
500	39	0
800	47	>4
1000	56	>4

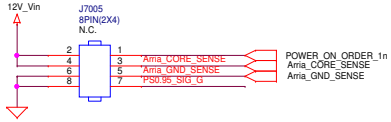
Change - was PVX006A0X3

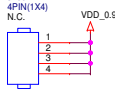
General change 47uF -
Move C-12101C476KATJ/X7R = 6.3V, 20%, X7R, ESR 2mohm @ 0.1MHz 0.2$
To C-12101X476KATJ = 10V, 10%, X5R, ESR 3mohm @ 0.1MHz 0.08$
GE example BOM is with worst Y5V capacitor

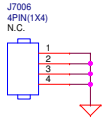
Optional change
C-TAJD337K010R/ESR 0.29$ 10V,10%,330MF,LOW ESR = 100 / 150 mohm @ 0.1MHz
C-TAJD337K006R 0.38$ 6V ,10%,330MF,LOW ESR = 50 mohm @ 0.1MHz
Due to better ESR stay with high price capacitor

0.95V/40A Piggy connection

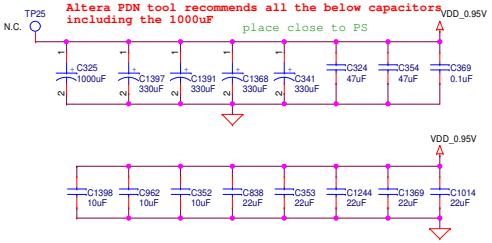
Rev 0.2 - Change - Removed PS7 and add piggy





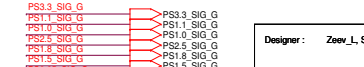


OLD - GE recommends 2x47uF + 4x330uF
OLD - Power integrity with all capacitors are 40MHz



Altera PDN tool recommends all the below capacitors including the 1000uF

Disperse GND TP on board both CS & PS



Designer :	Zeev_L, Shimon_A, Ran_Z
Title	VOLTAGE CONVERTERS
Size C	Design Name : ETX-2I-10G-LC.REV0.2I
Rev	0.0
Date:	Friday, June 17, 2016
Sheet	46 of 46

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