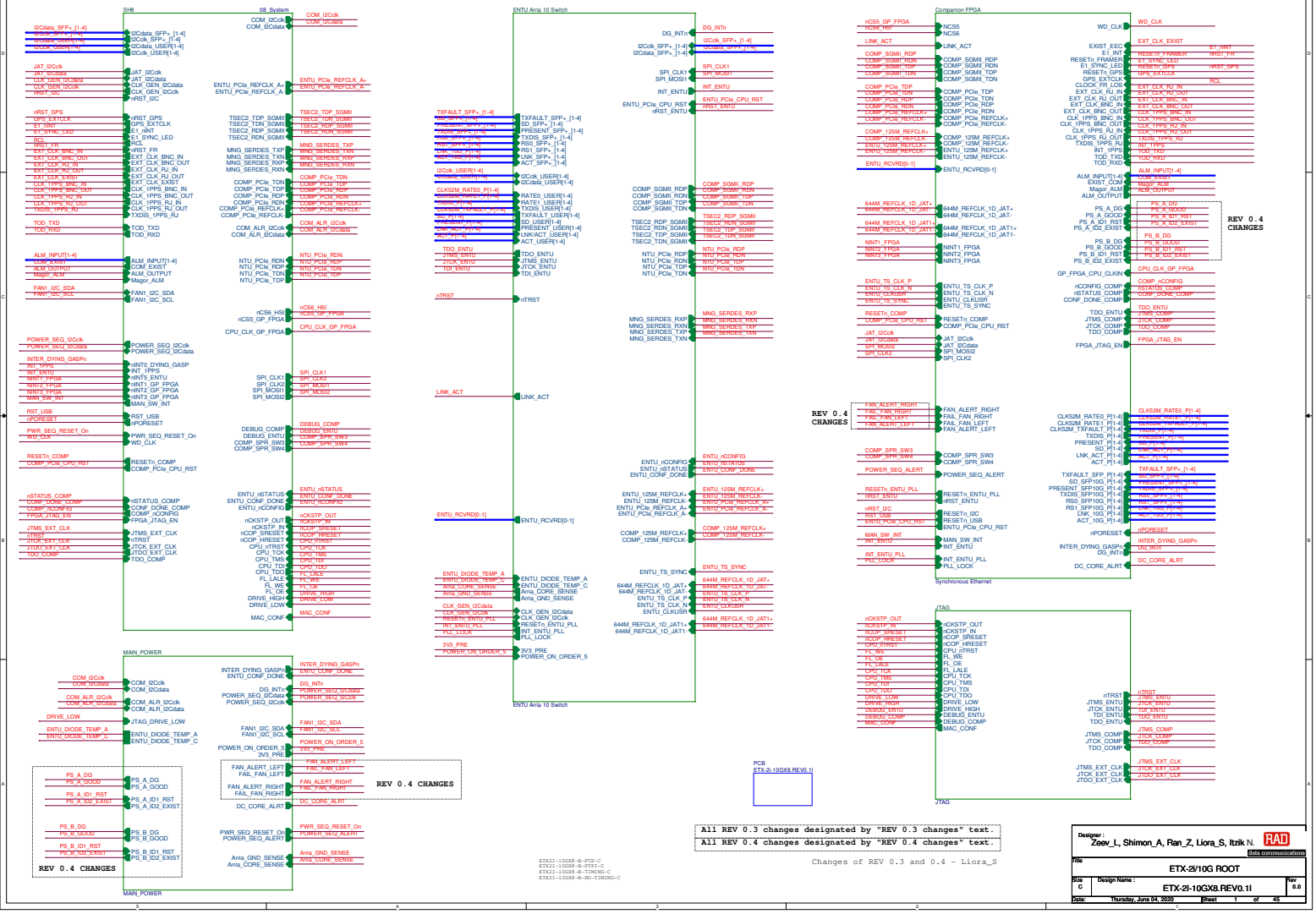
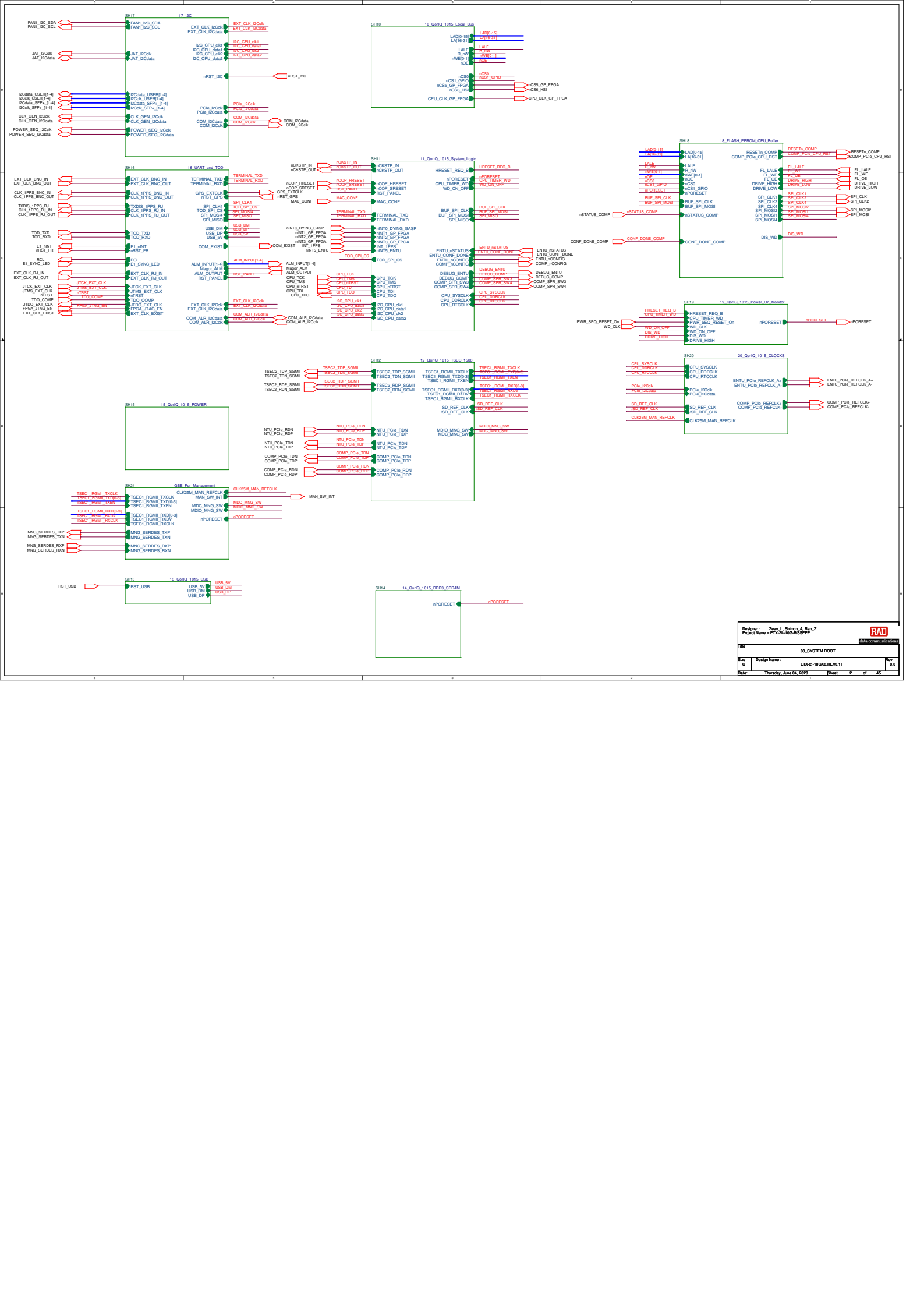
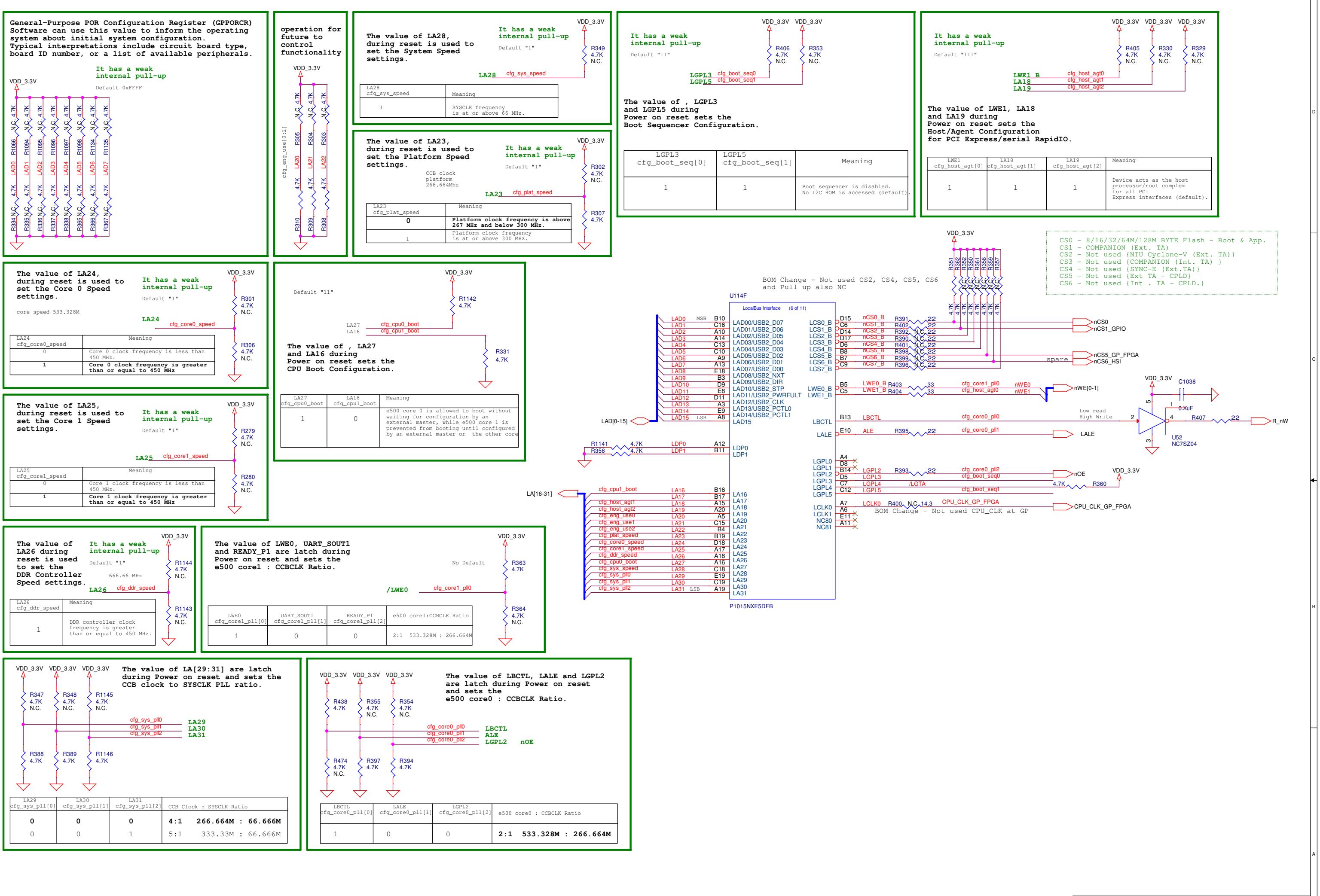
ETX-2i/10G 1/2 19" MAIN



DC_CORE_ALRT → DC_CORE_ALRT


SH17
17_I2C
FAN1_I2C_SDA
FAN1_I2C_SCL
JAT_I2Cclk
JAT_I2Cdata
I2Cdata_USER[1-4]
I2Cclk_USER[1-4]
I2Cdata_SFP+_[1-4]
I2Cclk_SFP+_[1-4]
CLK_GEN_I2Cclk
CLK_GEN_I2Cdata
POWER_SEQ_I2Cclk
POWER_SEQ_I2Cdata
EXT_CLK_I2Cclk
EXT_CLK_I2Cdata
I2C_CPU_clk1
I2C_CPU_data1
I2C_CPU_clk2
I2C_CPU_data2
nRST_I2C
PCIe_I2Cclk
PCIe_I2Cdata
COM_I2Cclk
COM_I2Cdata
SH10
10_QorIQ_1015_Local_Bus
LAD[0-15]
LA[16-31]
LALE
R_nW
nWE[0-1]
nOE
nCS0
nCS1_GPIO
nCS5_GP_FPGA
nCS6_HSI
CPU_CLK_GP_FPGA
nCS5
nCS6_HSI
CPU_CLK_GP_FPGA
SH16
16_UART_and_TOD
EXT_CLK_BNC_IN
EXT_CLK_BNC_OUT
CLK_1PPS_BNC_IN
CLK_1PPS_BNC_OUT
TXDIS_1PPS_RJ
CLK_1PPS_RJ_IN
CLK_1PPS_RJ_OUT
TOD_TXD
TOD_RXD
E1_nINT
nRST_FR
RCL
E1_SYNC_LED
EXT_CLK_RJ_IN
EXT_CLK_RJ_OUT
JTCK_EXT_CLK
JTMS_EXT_CLK
nTRST
TDO_COMP
JTDO_EXT_CLK
FPGA_JTAG_EN
EXT_CLK_EXIST
TERMINAL_TXD
TERMINAL_RXD
GPS_EXTCLK
nRST_GPS
SPI_CLK4
TOD_SPI_CS
SPI_MOSI4
SPI_MISO4
USB_DM
USB_DP
USB_5V
COM_EXIST
ALM_INPUT[1-4]
Major_ALM
ALM_OUTPUT
RST_PANEL
EXT_CLK_I2Cclk
EXT_CLK_I2Cdata
COM_ALR_I2Cdata
COM_ALR_I2Cclk
SH11
11_QorIQ_1015_System_Logic
nCKSTP_IN
nCKSTP_OUT
nCOP_HRESET
nCOP_SRESET
RST_PANEL
MAC_CONF
TERMINAL_TXD
TERMINAL_RXD
nINT0_DYING_GASP
nINT1_GP_FPGA
nINT2_GP_FPGA
nINT3_GP_FPGA
INT_1PPS
nINTS_ENTU
TOD_SPI_CS
CPU_TCK
CPU_TMS
CPU_nTRST
CPU_TDI
CPU_TDO
I2C_CPU_clk1
I2C_CPU_data1
I2C_CPU_clk2
I2C_CPU_data2
HRESET_REQ_B
nPORESET
CPU_TIMER_WD
WD_ON_OFF
BUF_SPI_CLK
BUF_SPI_MOSI
SPI_MISO
ENTU_nSTATUS
ENTU_CONF_DONE
ENTU_nCONFIG
COMP_nCONFIG
DEBUG_ENTU
DEBUG_COMP
COMP_SPR_SW3
COMP_SPR_SW4
CPU_SYSCLK
CPU_DDRCLK
CPU_RTCCLK
SH18
18_FLASH_EPROM_CPU_Buffer
LAD[0-15]
LA[16-31]
LALE
R_nW
nWE[0-1]
nOE
nCS0
nCS1_GPIO
nPORESET
BUF_SPI_CLK
BUF_SPI_MOSI
nSTATUS_COMP
CONF_DONE_COMP
RESETn_COMP
COMP_PCIe_CPU_RST
RESETn_COMP
COMP_PCIe_CPU_RST
FL_LALE
FL_WE
FL_OE
DRIVE_HIGH
DRIVE_LOW
SPI_CLK1
SPI_CLK2
SPI_CLK4
SPI_MOSI2
SPI_MOSI1
DIS_WD
SH19
19_QorIQ_1015_Power_On_Monitor
HRESET_REQ_B
CPU_TIMER_WD
PWR_SEQ_RESET_On
WD_CLK
WD_ON_OFF
DIS_WD
DRIVE_HIGH
nPORESET
SH20
20_QorIQ_1015_CLOCKS
CPU_SYSCLK
CPU_DDRCLK
CPU_RTCCLK
PCIe_I2Cclk
PCIe_I2Cdata
SD_REF_CLK
/SD_REF_CLK
CLK25M_MAN_REFCLK
ENTU_PCIe_REFCLK_A+
ENTU_PCIe_REFCLK_A-
COMP_PCIe_REFCLK+
COMP_PCIe_REFCLK-
SH12
12_QorIQ_1015_TSEC_1588
TSEC2_TDP_SGMII
TSEC2_TDN_SGMII
TSEC2_RDP_SGMII
TSEC2_RDN_SGMII
TSEC1_RGMII_TXCLK
TSEC1_RGMII_TXD[0-3]
TSEC1_RGMII_TXEN
TSEC1_RGMII_RXD[0-3]
TSEC1_RGMII_RXDV
TSEC1_RGMII_RXCLK
SD_REF_CLK
/SD_REF_CLK
MDIO_MNG_SW
MDC_MNG_SW
NTU_PCIe_RDN
NTU_PCIe_RDP
NTU_PCIe_TDN
NTU_PCIe_TDP
COMP_PCIe_TDN
COMP_PCIe_TDP
COMP_PCIe_RDN
COMP_PCIe_RDP
SH15
15_QorIQ_1015_POWER
SH24
GBE_For_Management
CLK25M_MAN_REFCLK
MAN_SW_INT
MDC_MNG_SW
MDIO_MNG_SW
nPORESET
MNG_SERDES_TXP
MNG_SERDES_TXN
MNG_SERDES_RXP
MNG_SERDES_RXN
SH13
13_QorIQ_1015_USB
RST_USB
USB_5V
USB_DM
USB_DP
SH14
14_QorIQ_1015_DDR3_SDRAM
nPORESET
Designer : Zeev_L, Shimon_A, Ran_Z
Project Name = ETX-2I-10G-B4SFPP
RAD
data communications
Title
08_SYSTEM ROOT
Size C
Design Name : ETX-2I-10GX8.REV0.11
Rev 0.0
Date: Thursday, June 04, 2020
Sheet 2 of 45



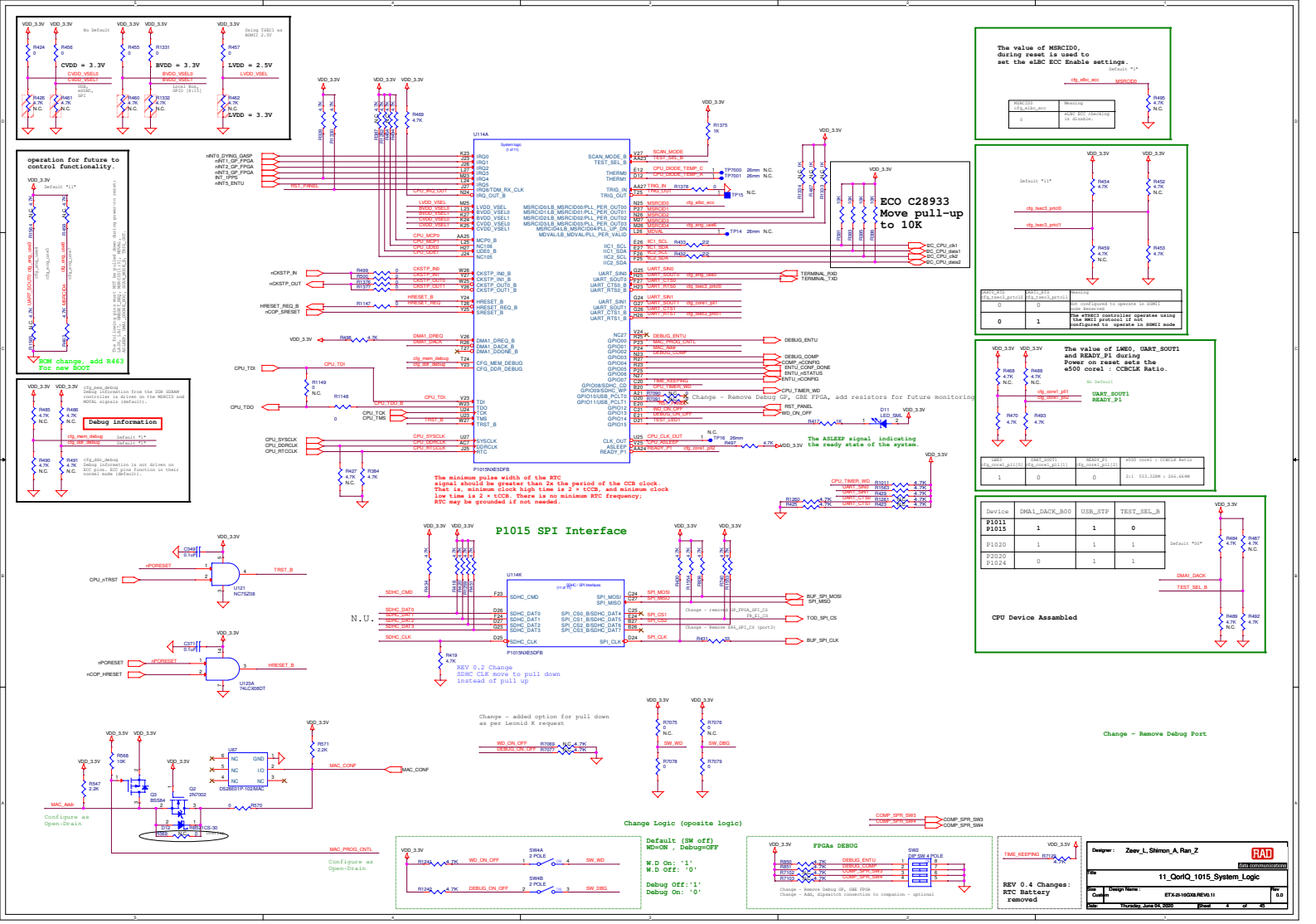
Designer : Zeev_L, Shimon_A, Ran_Z

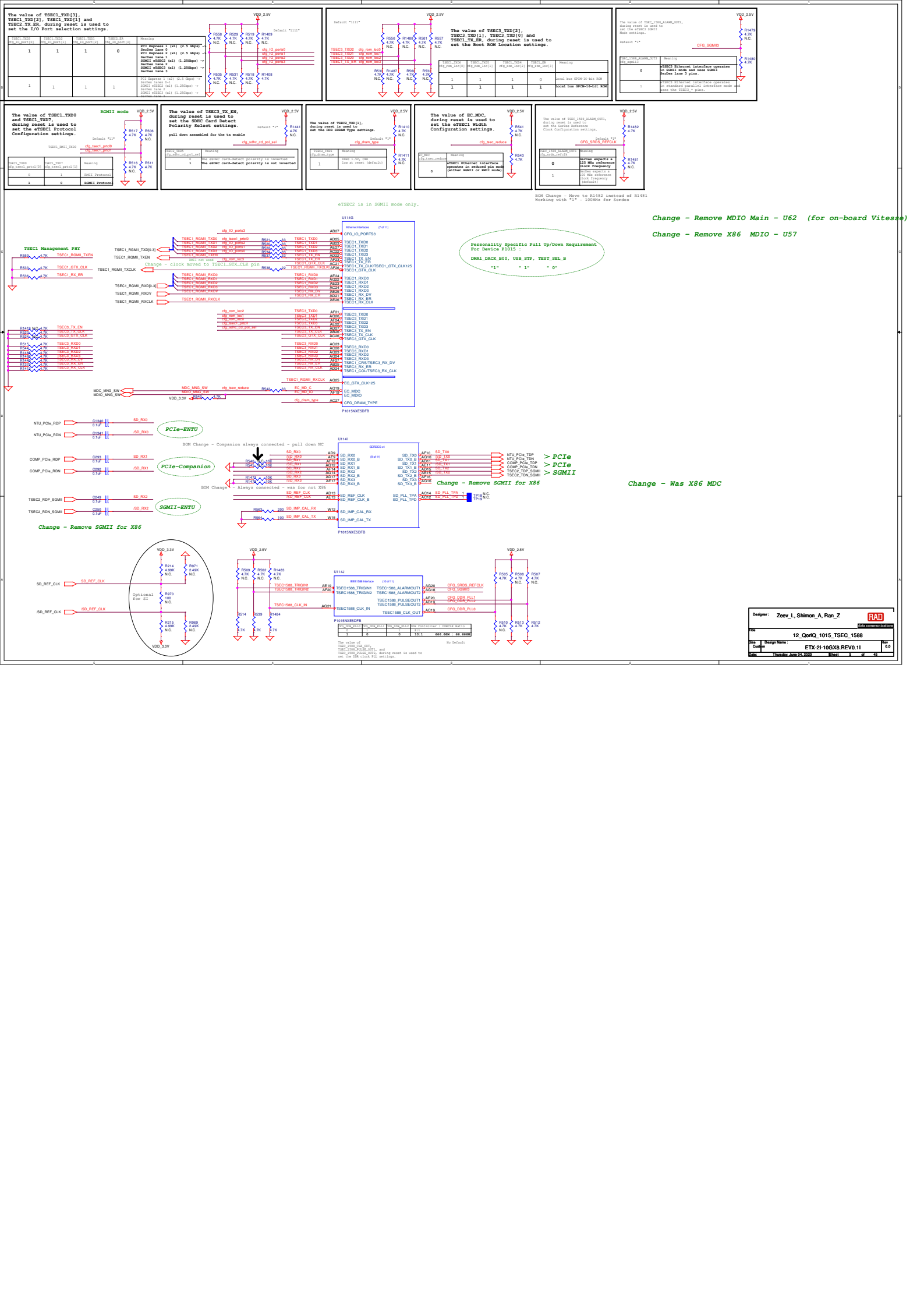
RAD data communications

Title: 10_QorIQ_1015_Local_Bus

Size	Design Name :	Rev
C	ETX-2I-10GX8.REV0.1I	0.0

Date: Thursday, June 04, 2020 | Sheet 3 of 45


CVDD = 3.3V
BVDD = 3.3V
LVDD = 2.5V
LVDD = 3.3V
operation for future to control functionality.
BOM change, add R463 For new BOOT
Debug information
P1015NXESDFB
The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is 2 * tCCB, and minimum clock low time is 2 x tCCB. There is no minimum RTC frequency; RTC may be grounded if not needed.
P1015 SPI Interface
N.U.
REV 0.2 Change
SDHC_CLK move to pull down instead of pull up
Change - added option for pull down as per Leonid K request
Configure as Open-Drain
Change Logic (oposite logic)
Default (SW off)
WD=ON , Debug=OFF
W.D On: '1'
W.D Off: '0'
Debug Off:'1'
Debug On: '0'
FPGAs DEBUG
Change - Remove Debug GP, GBE FPGA
Change - Add, dipswitch connection to companion - optional
ECO C28933
Move pull-up to 10K
Change - Remove Debug GP, GBE FPGA, add resistors for future monitoring
The value of MSRCID0, during reset is used to set the eLBC ECC Enable settings.
The value of LWE0, UART_SOUT1 and READY_P1 during Power on reset sets the e500 core1 : CCBCLK Ratio.
UART_SOUT1
READY_P1
The ASLEEP signal indicating the ready state of the system.
CPU Device Assambled
Change - Remove Debug Port
REV 0.4 Changes:
RTC Battery removed
Designer: Zeev_L, Shimon_A, Ran_Z
RAD data communications
11_QorIQ_1015_System_Logic
ETX-2S-10CO28.REV0.11
Thursday, June 04, 2020
Sheet 4 of 45


The value of TSEC1_TXD[3], TSEC1_TXD[2], TSEC1_TXD[1] and TSEC2_TX_ER, during reset is used to set the I/O Port selection settings.
The value of TSEC3_TXD[2], TSEC3_TXD[1], TSEC3_TXD[0] and TSEC1_TX_ER, during reset is used to set the Boot ROM Location settings.
The value of TSEC1_TXD0 and TSEC1_TXD7, during reset is used to set the eTSEC1 Protocol Configuration settings.
RGMII mode
The value of TSEC_TX_EN, during reset is used to set the SDHC Card Detect Polarity Select settings.
pull down assembled for the tx enable
The value of TSEC3_TXD[1], during reset is used to set the IEEE 1588 CLK settings.
The value of EC_MDC, during reset is used to set the eTSEC1 Width Configuration settings.
eTSEC2 is in SGMII mode only.
Change - Remove MDIO Main - U62 (for on-board Vitesse)
Change - Remove X86 MDIO - U57
TSEC1 Management PHY
Change - clock moved to TSEC1_GTX_CLK pin
Personality Specific Pull Up/Down Requirement For Device P1015 :
DMA1_DACK_B00, USB_STP, TEST_SEL_B
"1" " 1" " 0"
PCIe-ENTU
PCIe-Companion
SGMII-ENTU
BOM Change - Companion always connected - pull down NC
BOM Change - Always connected - was for not X86
Change - Remove SGMII for X86
Change - Remove SGMII for X86
Change - Was X86 MDC
BOM Change - Move to R1482 instead of R1481 Working with "1" - 100MHz for Serdes
Designer: Zeev_L, Shimon_A, Ran_Z
data communications
File: 12_QorIQ_1015_TSEC_1588
Size: Custom
Design Name: ETX-2I-10GX8.REV0.1I
Rev: 0.0
Date: Thursday, June 04, 2020
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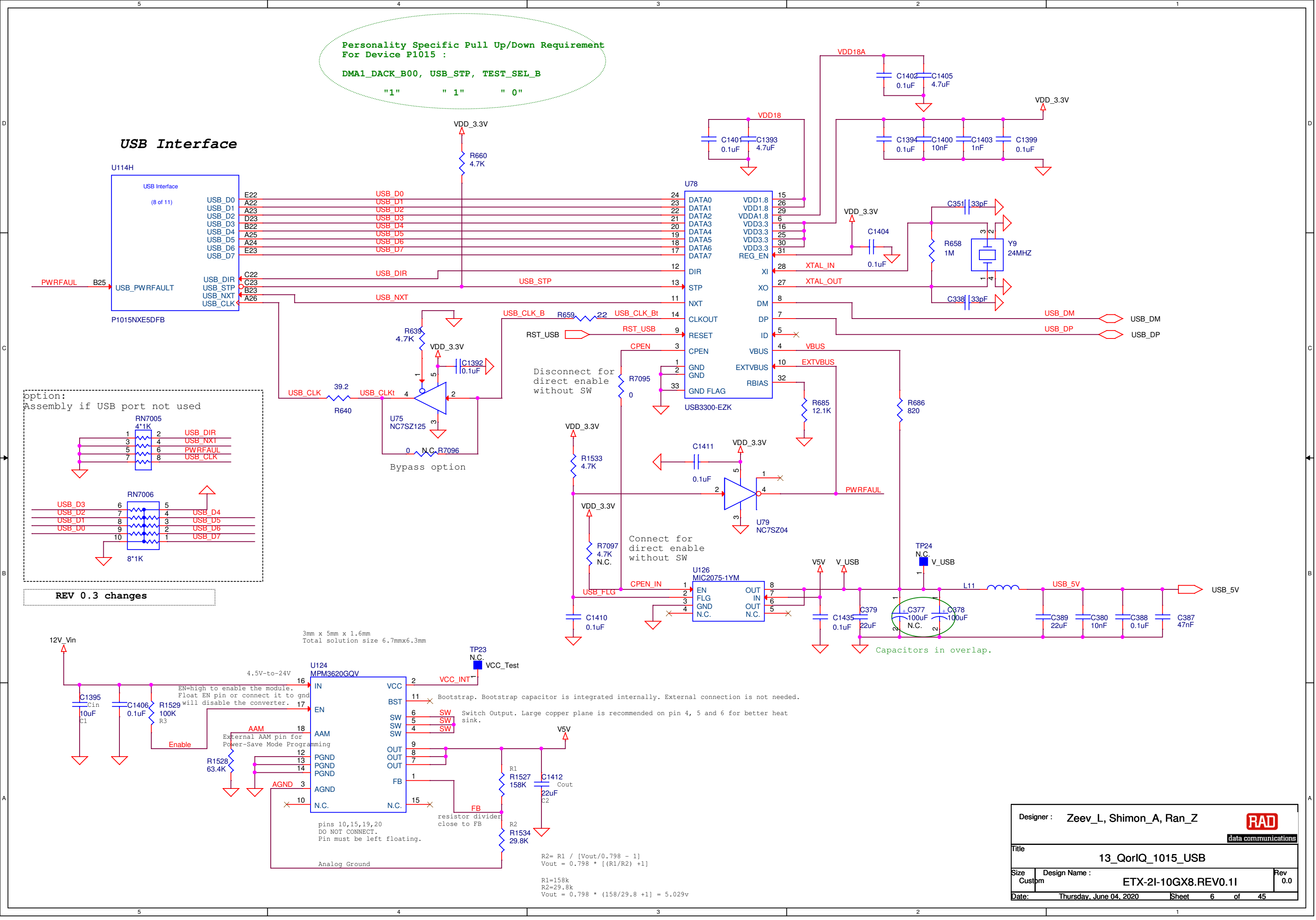


Personality Specific Pull Up/Down Requirement
For Device P1015 :
DMA1_DACK_B00, USB_STP, TEST_SEL_B
"1" " 1" " 0"
USB Interface
U114H
USB Interface
(8 of 11)
P1015NXE5DFB
USB_D0
USB_D1
USB_D2
USB_D3
USB_D4
USB_D5
USB_D6
USB_D7
USB_DIR
USB_STP
USB_NXT
USB_CLK
USB_PWRFAULT
PWRFAUL
VDD_3.3V
R660
4.7K
U78
USB3300-EZK
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
DIR
STP
NXT
CLKOUT
RESET
CPEN
GND
GND FLAG
VDD1.8
VDDA1.8
VDD3.3
REG_EN
XI
XO
DM
DP
ID
VBUS
EXTVBUS
RBIAS
VDD18A
VDD18
C1402
0.1uF
C1405
4.7uF
C1401
0.1uF
C1393
4.7uF
C1394
0.1uF
C1400
10nF
C1403
1nF
C1399
0.1uF
C1404
0.1uF
C351
33pF
C338
33pF
R658
1M
Y9
24MHZ
XTAL_IN
XTAL_OUT
USB_DM
USB_DP
RST_USB
USB_CLK_B
R659
22
USB_CLK_Bt
R639
4.7K
C1392
0.1uF
U75
NC7SZ125
R640
39.2
USB_CLKt
N.C.R7096
0
Bypass option
Disconnect for direct enable without SW
R7095
0
R685
12.1K
R686
820
option:
Assembly if USB port not used
RN7005
4*1K
RN7006
8*1K
REV 0.3 changes
R1533
4.7K
C1411
0.1uF
U79
NC7SZ04
PWRFAUL
R7097
4.7K
N.C.
Connect for direct enable without SW
CPEN_IN
USB_FLG
U126
MIC2075-1YM
EN
FLG
GND
N.C.
OUT
IN
C1410
0.1uF
V5V
V_USB
TP24
N.C.
C1435
0.1uF
C379
22uF
C377
100uF
N.C.
C378
100uF
L11
USB_5V
C389
22uF
C380
10nF
C388
0.1uF
C387
47nF
Capacitors in overlap.
12V_Vin
C1395
10uF
C1406
0.1uF
R1529
100K
Enable
3mm x 5mm x 1.6mm
Total solution size 6.7mmx6.3mm
4.5V-to-24V
U124
MPM3620GQV
EN=high to enable the module.
Float EN pin or connect it to gnd will disable the converter.
External AAM pin for Power-Save Mode Programming
R1528
63.4K
AAM
AGND
VCC
BST
SW
OUT
FB
PGND
N.C.
TP23
N.C.
VCC_Test
VCC_INT
Bootstrap. Bootstrap capacitor is integrated internally. External connection is not needed.
Switch Output. Large copper plane is recommended on pin 4, 5 and 6 for better heat sink.
R1527
158K
C1412
22uF
Cout
R1534
29.8K
resistor divider close to FB
pins 10,15,19,20
DO NOT CONNECT.
Pin must be left floating.
Analog Ground
R2= R1 / [Vout/0.798 - 1]
Vout = 0.798 * [(R1/R2) +1]
R1=158k
R2=29.8k
Vout = 0.798 * (158/29.8 +1) = 5.029v
Designer : Zeev_L, Shimon_A, Ran_Z
RAD
data communications
Title
13_QorIQ_1015_USB
Size Custom
Design Name :
ETX-2I-10GX8.REV0.1I
Rev 0.0
Date: Thursday, June 04, 2020
Sheet 6 of 45

The layout of:
single-ended signal traces should be 50 Ohms
differential signal traces should be 100 Ohms.

clock matching:
+/-10 mils for CK to CK#;
+/-25 mils clock pair to clock pair;

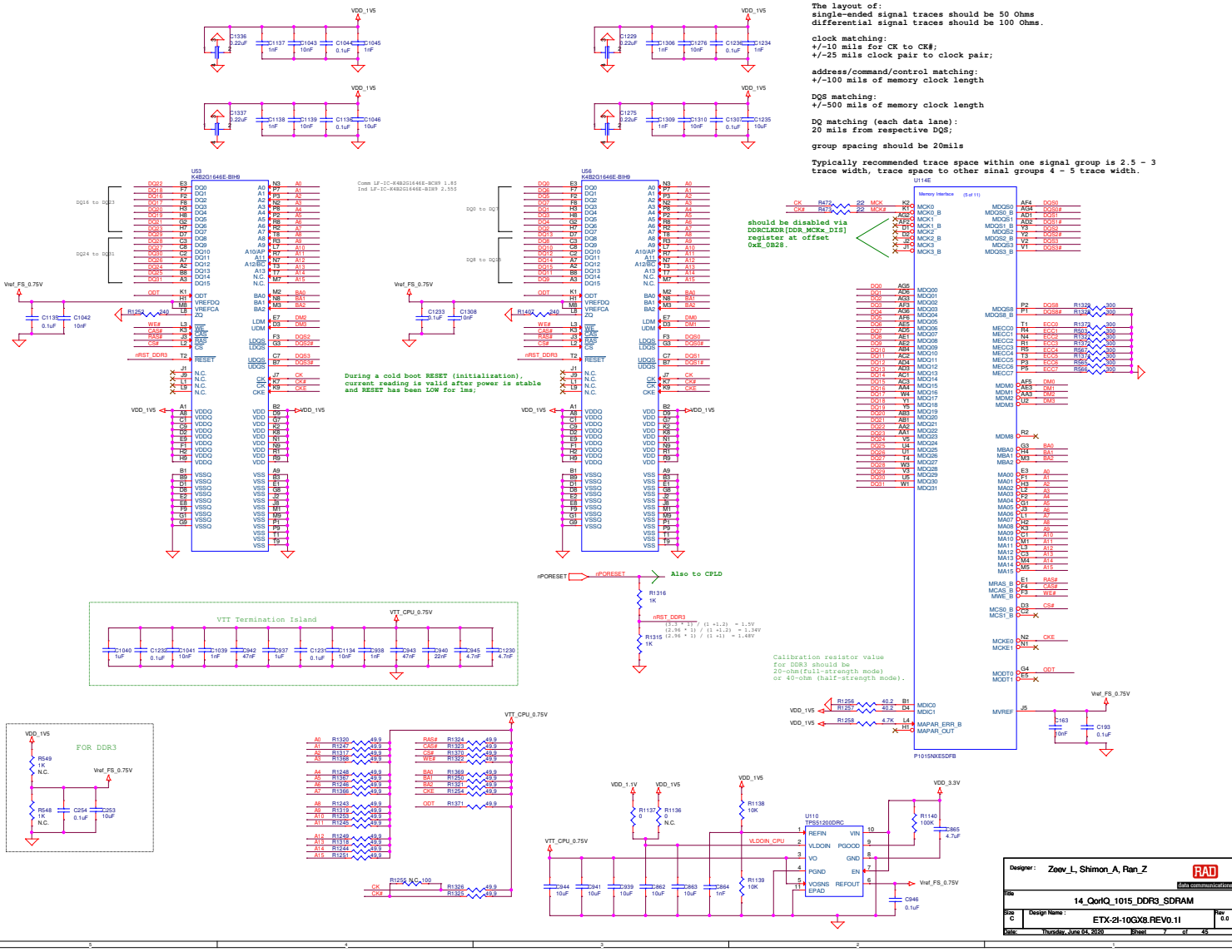
address/command/control matching:
+/-100 mils of memory clock length

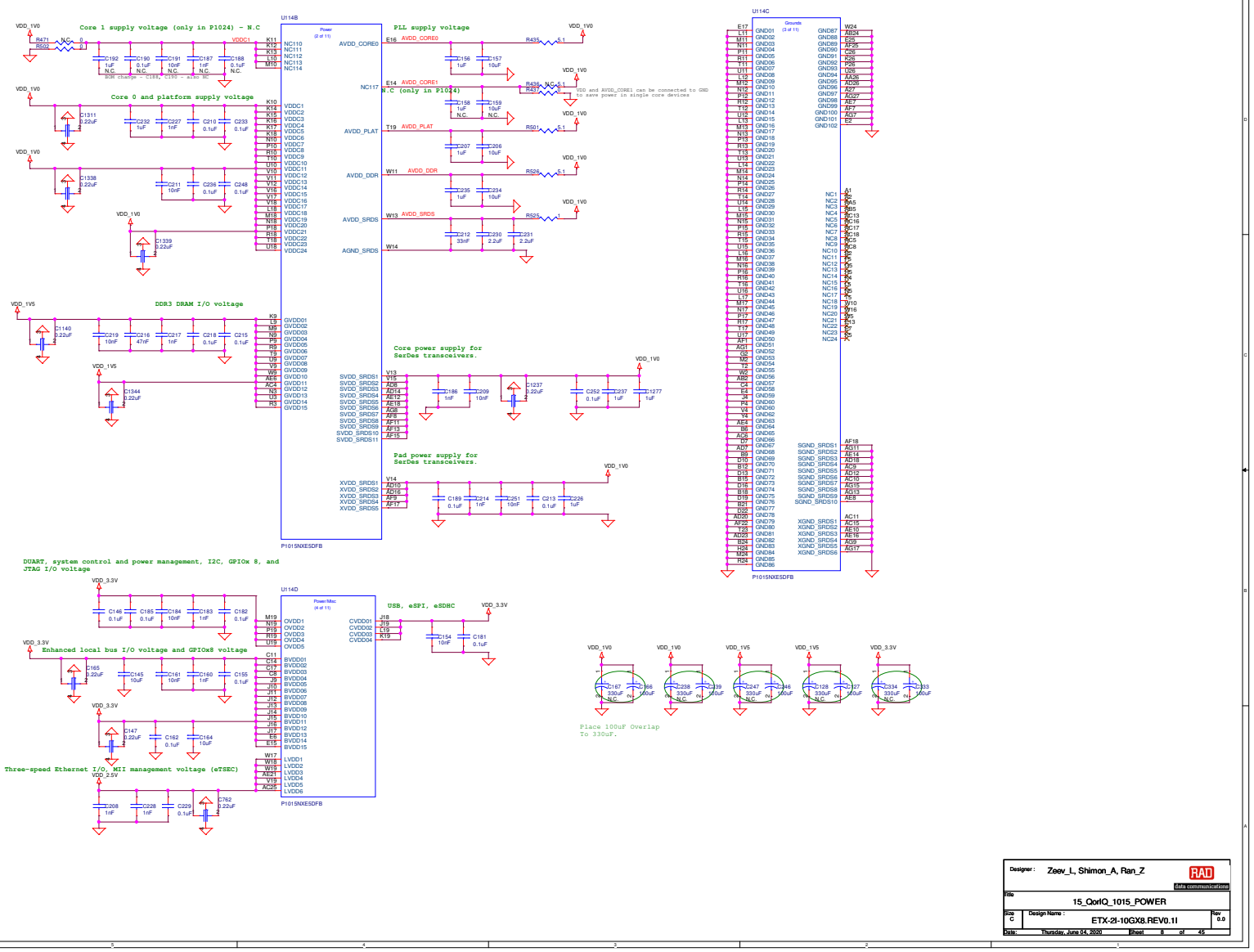
DQS matching:
+/-500 mils of memory clock length

DQ matching (each data lane):
20 mils from respective DQS;

group spacing should be 20mils

Typically recommended trace space within one signal group is 2.5 - 3 trace width, trace space to other sinal groups 4 - 5 trace width.




Core 1 supply voltage (only in P1024) - N.C
Core 0 and platform supply voltage
DDR3 DRAM I/O voltage
PLL supply voltage
Core power supply for SerDes transceivers.
Pad power supply for SerDes transceivers.
DUART, system control and power management, I2C, GPIOx 8, and JTAG I/O voltage
Enhanced local bus I/O voltage and GPIOx8 voltage
Three-speed Ethernet I/O, MII management voltage (eTSEC)
USB, eSPI, eSDHC
VDD and AVDD_CORE1 can be connected to GND to save power in single core devices
Place 100uF Overlap To 330uF.
P1015NXESDFB
Designer : Zeev_L, Shimon_A, Ran_Z
15_QorIQ_1015_POWER
ETX-2I-10GX8.REV0.1I
Thursday, June 04, 2020

Connector for COMMUNICATION

BOM - Always connected
No special BOM for comm/alra, piggy

Place close to
Communication/ALM Piggy

Place close to
Panel (RS232 connector)

I2C nets names changed

REV 0.3 changes

BOM Change - Remove RST_Panel pull up (another pull up at CPU scheme)

Change - Added, check

RS232 Control Port

Enable/Disable transmit
when receiver level not
valid.
0 function not operate

Discharging
resistor

Change - Added, check

Factory default
Low active

POWER# :
0 - USB device in Configured state
1 - USB device in Unconfigured state
or during USB suspend mode

Change - Option for automatically chain bypass when no Timing piggy ('1')

SLEEP# :
0 - indicates USB suspend

Place close to EEC/Timing Piggy

Connector for EEC

Designer :	Zeev_I, Shimon_A, Ran_Z
Title	16_UART_and_TOD
Size	C
Design Name :	ETX-2I-10GX8.REV0.1I
Rev	0.0
Date:	Thursday, June 04, 2020
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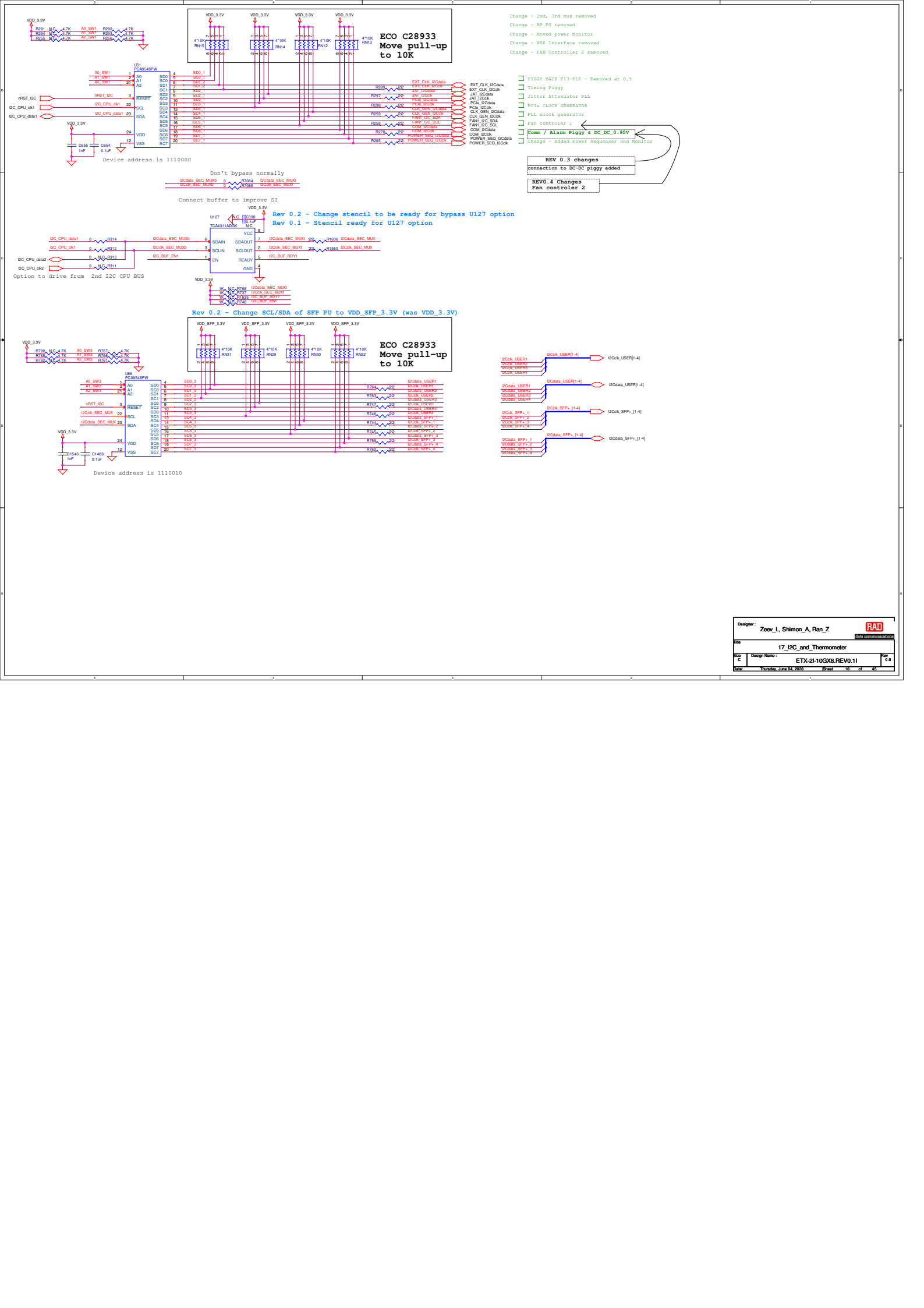
ECO C28933
Move pull-up
to 10K
Change - 2md, 3rd mux removed
Change - BP PS removed
Change - Moved power Monitor
Change - X86 Interface removed
Change - FAN Controller 2 removed
PIGGY BACK P13-P16 - Removed at 0.5
Timing Piggy
Jitter Attenuator PLL
PCIe CLOCK GENERATOR
PLL clock generator
Fan controler 1
Comm / Alarm Piggy & DC_DC_0.95V
Change - Added Power Sequencer and Monitor
REV 0.3 changes
connection to DC-DC piggy added
REV0.4 Changes
Fan controler 2
Device address is 1110000
Don't bypass normally
Connect buffer to improve SI
Rev 0.2 - Change stencil to be ready for bypass U127 option
Rev 0.1 - Stencil ready for U127 option
Option to drive from 2nd I2C CPU BUS
Rev 0.2 - Change SCL/SDA of SFP PU to VDD_SFP_3.3V (was VDD_3.3V)
ECO C28933
Move pull-up
to 10K
Device address is 1110010
Designer :
Zeev_L, Shimon_A, Ran_Z
Title
17_I2C_and_Thermometer
Size
C
Design Name :
ETX-2I-10GX8.REV0.1I
Rev
0.0
Date:
Thursday, June 04, 2020
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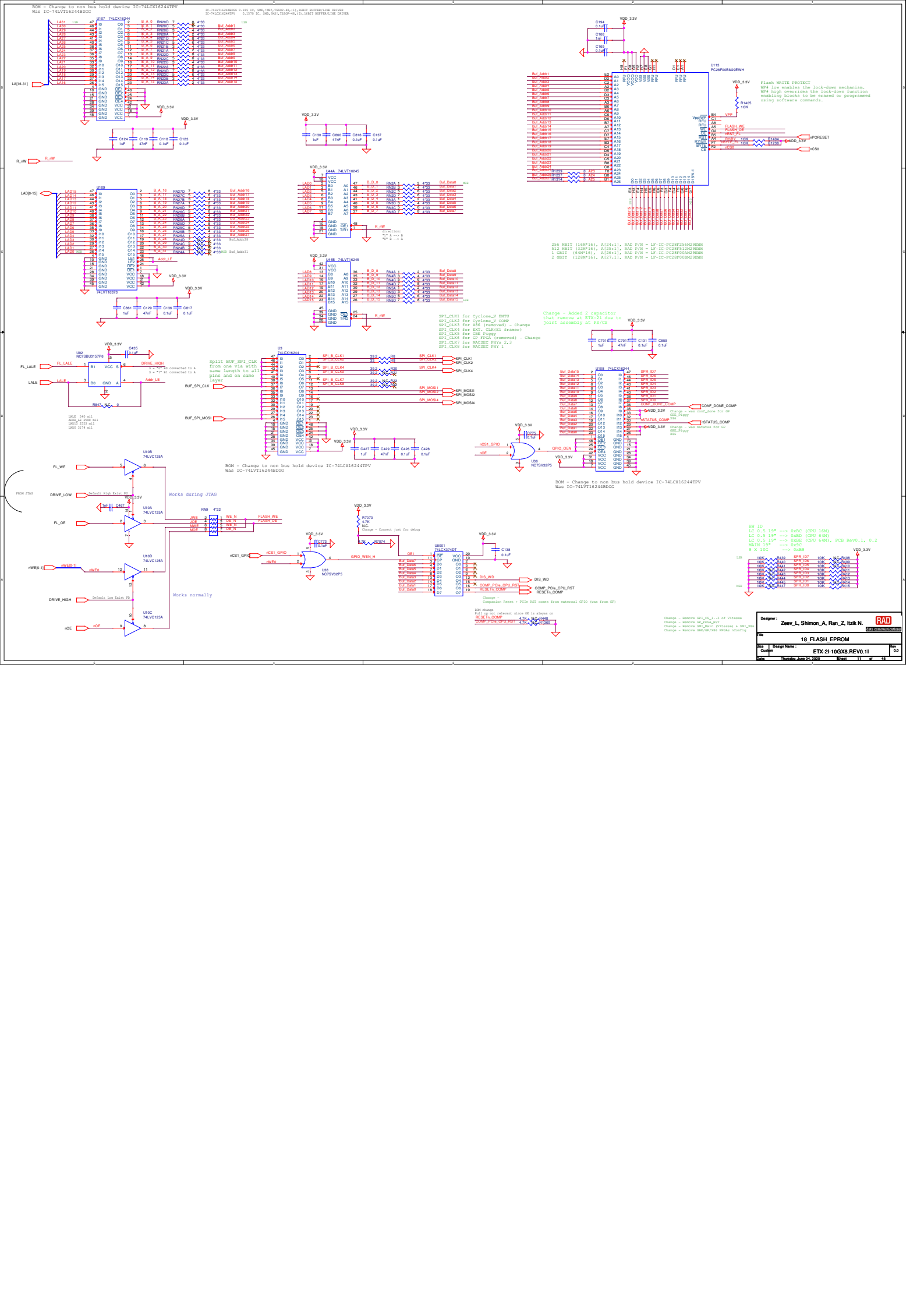
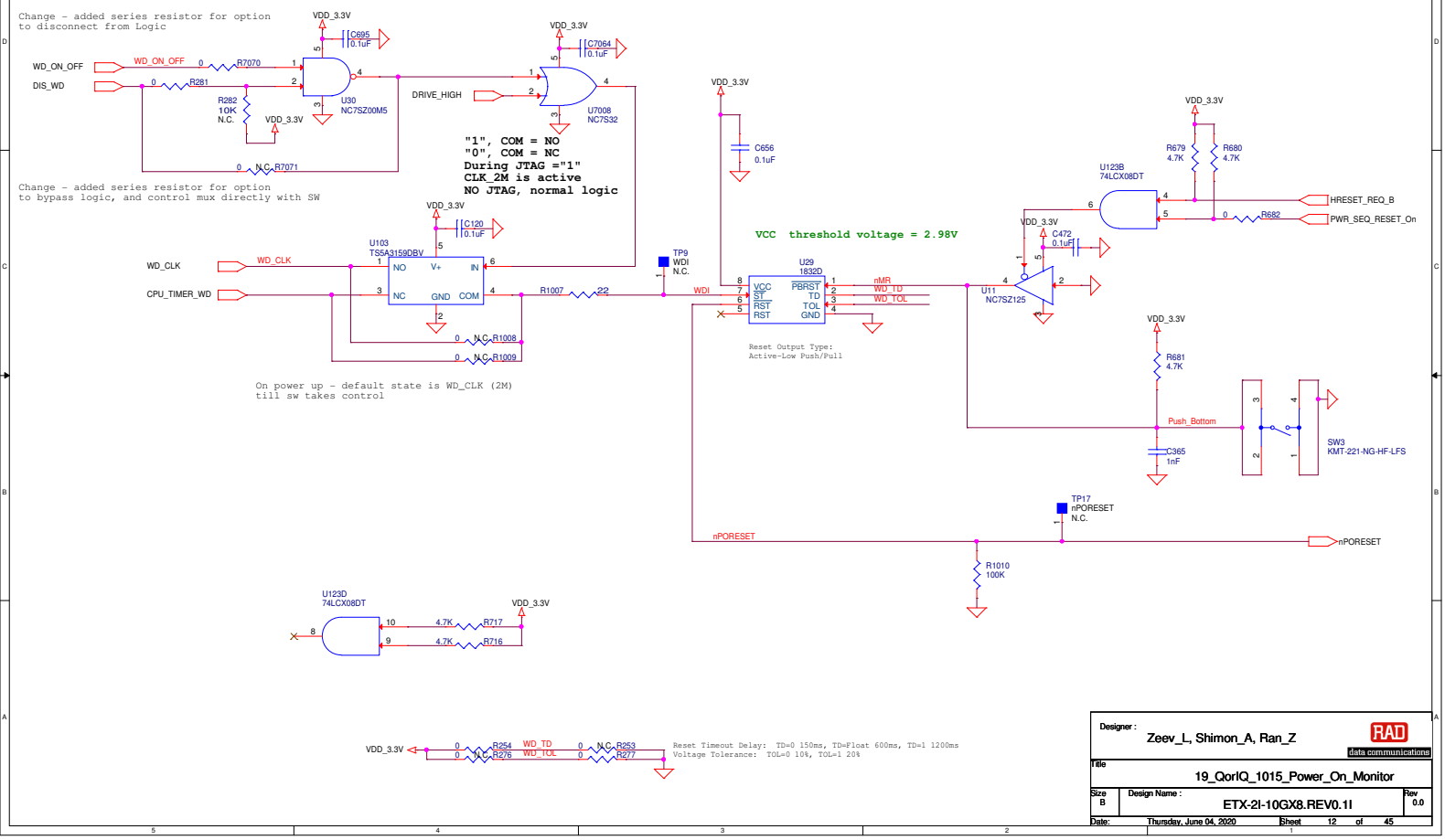
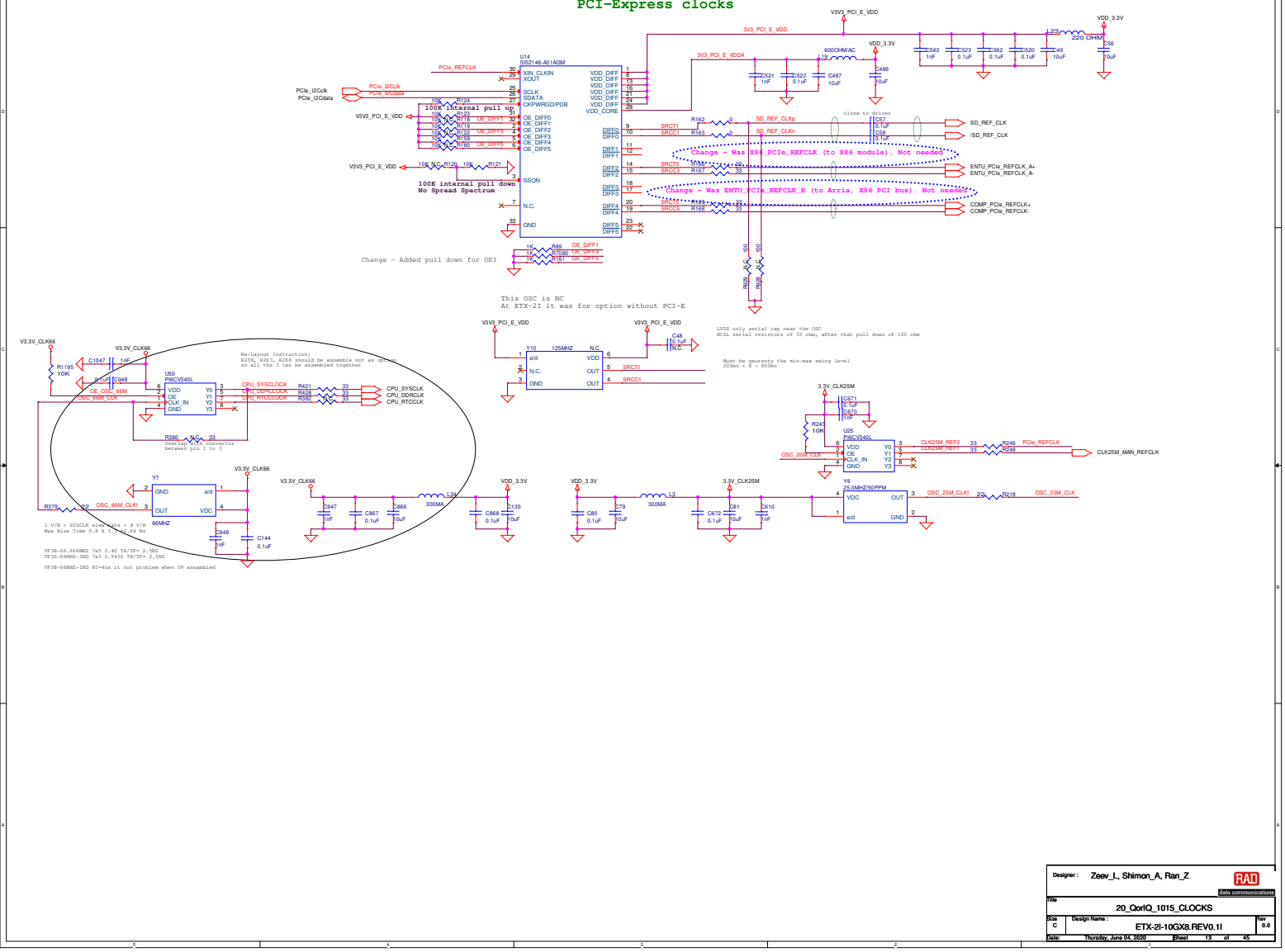

BOM - Change to non bus hold device IC-74LCX16244TPV
Was IC-74LVT16244BDGG
U107 74LCX16244
LA[16-31]
Buf_Addr1
Buf_Addr2
Buf_Addr3
Buf_Addr4
Buf_Addr5
Buf_Addr6
Buf_Addr7
Buf_Addr8
Buf_Addr9
Buf_Addr10
Buf_Addr11
Buf_Addr12
Buf_Addr13
Buf_Addr14
Buf_Addr15
VDD_3.3V
R_nW
LAD[0-15]
U109
74LVT16373
Addr_LE
Buf_Addr16
Buf_Addr17
Buf_Addr18
Buf_Addr19
Buf_Addr20
Buf_Addr21
Buf_Addr22
Buf_Addr23
Buf_Addr24
Buf_Addr25
Buf_Addr26
Buf_Addr27
Buf_Addr28
Buf_Addr31
U44 74LVT16245
U48 74LVT16245
Buf_Data0
Buf_Data1
Buf_Data2
Buf_Data3
Buf_Data4
Buf_Data5
Buf_Data6
Buf_Data7
Buf_Data8
Buf_Data9
Buf_Data10
Buf_Data11
Buf_Data12
Buf_Data13
Buf_Data14
Buf_Data15
U113
PC28F00BM29EWH
Flash WRITE PROTECT
WP# low enables the lock-down mechanism.
WP# high overrides the lock-down function
enabling blocks to be erased or programmed
using software commands.
nPORESET
nCS0
256 MBIT (16M*16), A[24:1], RAD P/N = LF-IC-PC28F256M29EWH
512 MBIT (32M*16), A[25:1], RAD P/N = LF-IC-PC28F512M29EWH
1 GBIT (64M*16), A[26:1], RAD P/N = LF-IC-PC28F00AM29EWH
2 GBIT (128M*16), A[27:1], RAD P/N = LF-IC-PC28F00BM29EWH
Change - Added 2 capacitor
that remove at ETX-2i due to
joint assembly at P5/C5
SPI_CLK1 for Cyclone_V ENTU
SPI_CLK2 for Cyclone_V COMP
SPI_CLK3 for X86 (removed) - Change
SPI_CLK4 for EXT. CLK(E1 framer)
SPI_CLK5 for GBE Piggy
SPI_CLK6 for GP FPGA (removed) - Change
SPI_CLK7 for MACSEC PHYs 2,3
SPI_CLK8 for MACSEC PHY 1
U80
NC7SBU157P6
FL_LALE
LALE
DRIVE_HIGH
Addr_LE
Split BUF_SPI_CLK
from one via with
same length to all
pins and on same
layer
BUF_SPI_CLK
BUF_SPI_MOSI
SPI_CLK1
SPI_CLK2
SPI_CLK4
SPI_MOSI1
SPI_MOSI2
SPI_MOSI4
U3
74LCX16244
U108
74LCX16244
SPR_ID7
SPR_ID6
SPR_ID5
SPR_ID4
SPR_ID3
SPR_ID2
SPR_ID1
SPR_ID0
CONF_DONE_COMP
nSTATUS_COMP
Change - was conf_done for GP GBE_Piggy
Change - was nStatus for GP GBE_Piggy
X86
BOM - Change to non bus hold device IC-74LCX16244TPV
Was IC-74LVT16244BDGG
U10B
74LVC125A
U10A
74LVC125A
U10D
74LVC125A
U10C
74LVC125A
FL_WE
DRIVE_LOW
FL_OE
nWE[0-1]
DRIVE_HIGH
nOE
Works during JTAG
Works normally
Default High Exist PD
Default Low Exist PD
FROM JTAG
RN9 4*22
FLASH_WE
FLASH_OE
nCS1_GPIO
nWE0
GPIO_WEN_H
U8001
74LCX374DT
U8
NC7SV32P5
DIS_WD
COMP_PCIe_CPU_RST
RESETn_COMP
Change - Connect just for debug
Change - Comparison Reset + PCIe RST comes from external GPIO (was from GP)
BOM change
Pull up not relevant since OE is always on
Change - Remove SPI_CS_1..3 of Vitesse
Change - Remove GP_FPGA_RST
Change - Remove SMI_Main (Vitesse) & SMI_X86
Change - Remove GBE/GP/X86 FPGAs nConfig
HW ID
LC 0.5 19" --> 0xBC (CPU 16M)
LC 0.5 19" --> 0xBD (CPU 64M)
LC 0.5 19" --> 0xBE (CPU 64M), PCB Rev0.1, 0.2
KAIA 19" --> 0xBC
8 X 10G --> 0xB8
Designer : Zeev_L, Shimon_A, Ran_Z, Itzik N.
RAD data communications
Title
18_FLASH_EPROM
Size
Custom
Design Name :
ETX-2I-10GX8_REV0.1I
Rev
0.0
Date: Thursday, June 04, 2020
Sheet 11 of 45

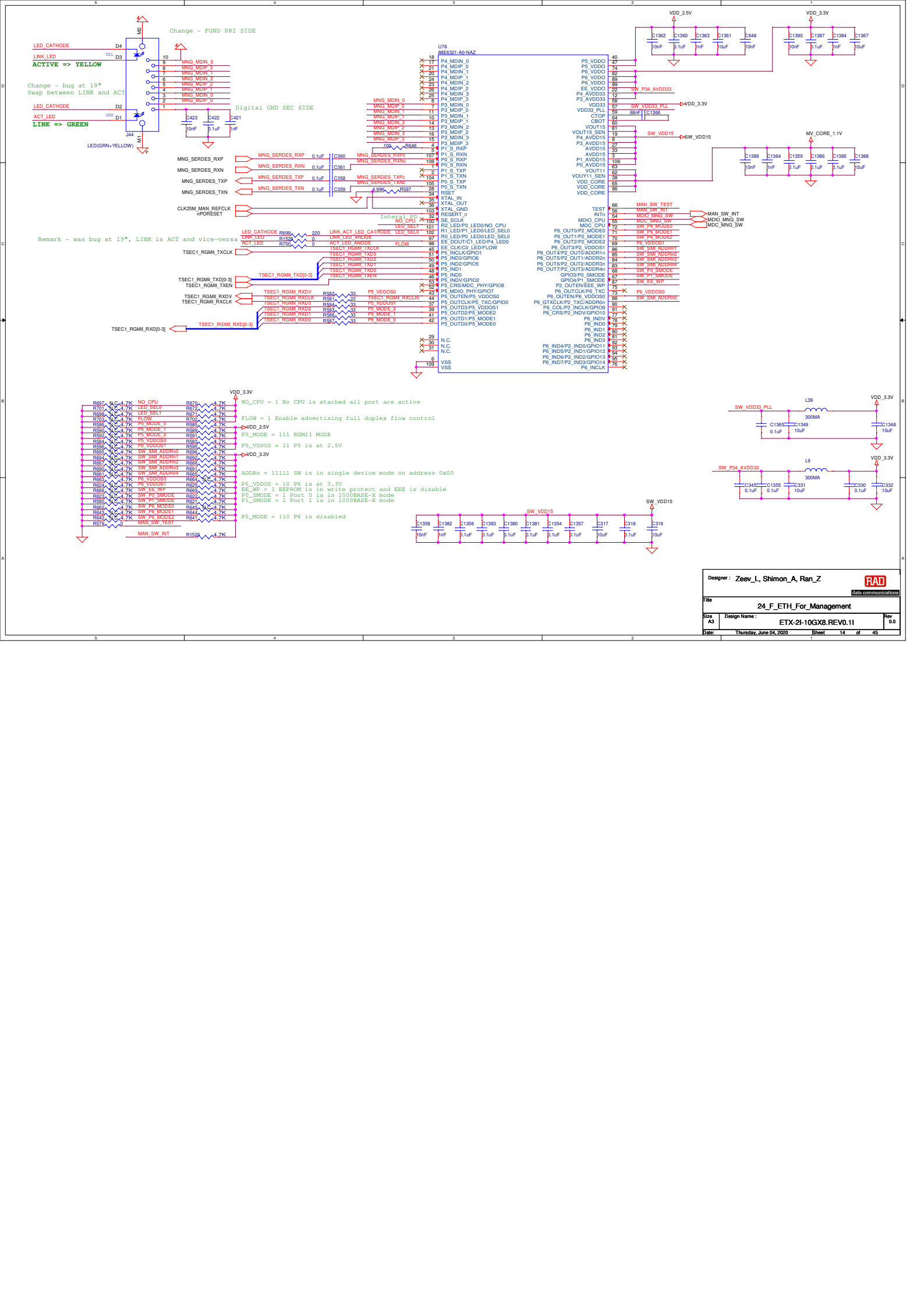


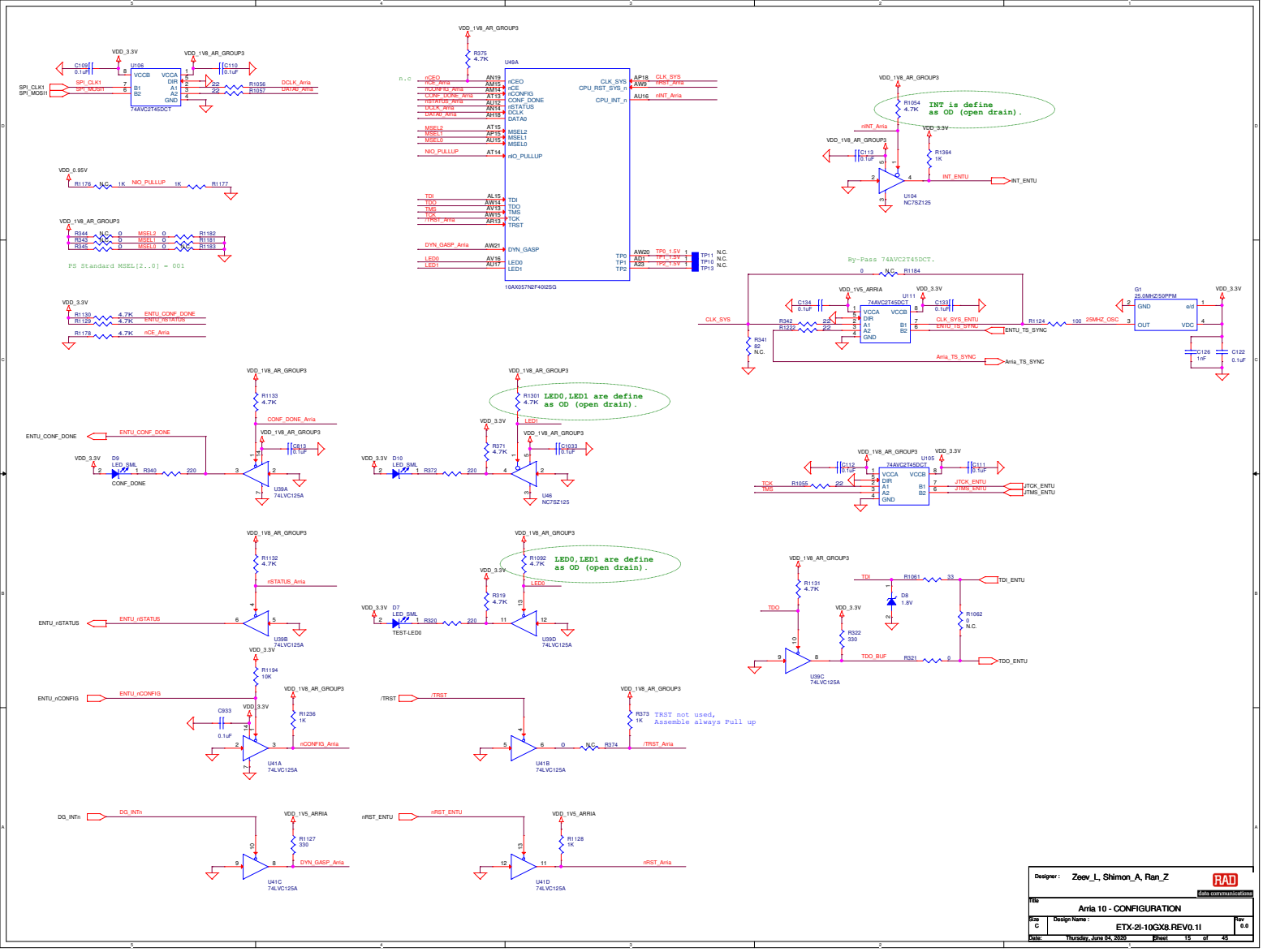
Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications
Title	19_QorIQ_1015_Power_On_Monitor	
Size B	Design Name : ETX-2I-10GX8.REV0.1I	Rev 0.0
Date: Thursday, June 04, 2020	Sheet 12 of 45	

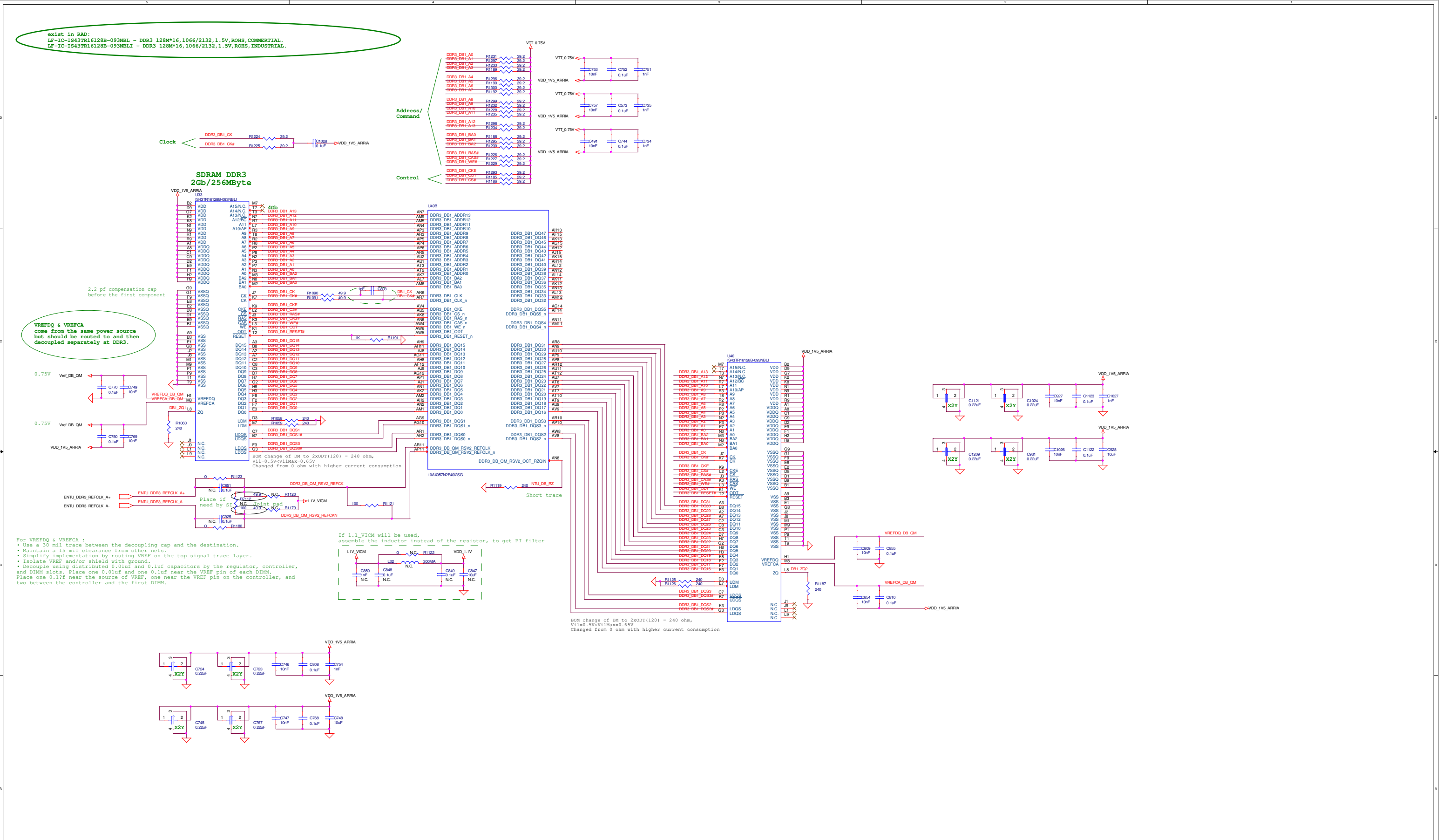
PCI-Express clocks



Designer :	Zeev_I, Shimon_A, Ran_Z	RAD data communications	
Title	20_QorIQ_1015_CLOCKS		
Size C	Design Name : ETX-2I-10GX8.REV0.1I		Rev 0.0
Date: Thursday, June 04, 2020		Sheet 13 of 45	

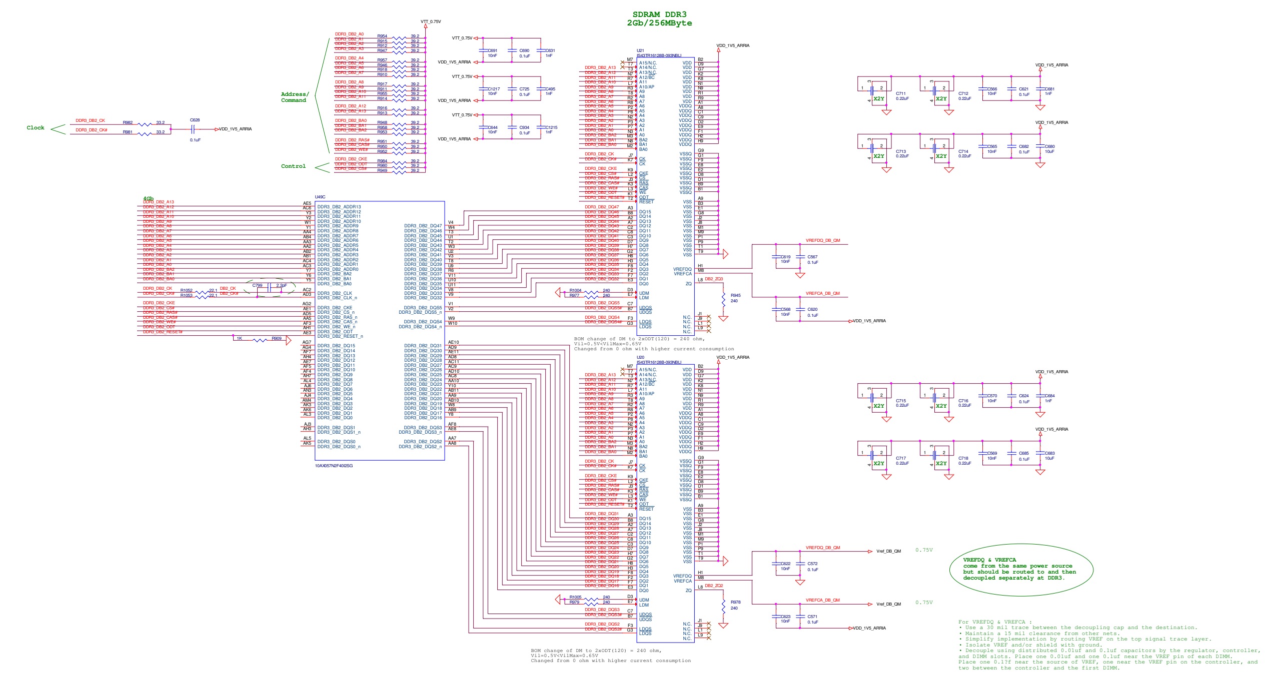

Change - FGND PRI SIDE
LED_CATHODE
LINK_LED
ACTIVE => YELLOW
Change - bug at 19"
Swap between LINK and ACT
LED_CATHODE
ACT_LED
LINK => GREEN
LED(GRN+YELLOW)
Digital GND SEC SIDE
Remark - was bug at 19", LINK is ACT and vice-versa
U76
88E6321-A0-NAZ
Interal PD
NO_CPU = 1 No CPU is atached all port are active
FLOW = 1 Enable advertising full duplex flow control
P5_MODE = 111 RGMII MODE
P5_VDDOS = 11 P5 is at 2.5V
ADDRn = 11111 SW is in single device mode on address 0x00
P6_VDDOS = 10 P6 is at 3.3V
EE_WP = 1 EEPROM is in write protect and EEE is disable
P0_SMODE = 1 Port 0 is in 1000BASE-X mode
P1_SMODE = 1 Port 1 is in 1000BASE-X mode
P6_MODE = 110 P6 is disabled
Designer : Zeev_L, Shimon_A, Ran_Z
data communications
Title
24_F_ETH_For_Management
Size A3
Design Name :
ETX-2I-10GX8.REV0.1I
Rev 0.0
Date: Thursday, June 04, 2020
Sheet 14 of 45


INT is define as OD (open drain).
LED0,LED1 are define as OD (open drain).
LED0,LED1 are define as OD (open drain).
By-Pass 74AVC2T45DCT.
TRST not used, Assemble always Pull up
PS Standard MSEL[2..0] = 001
10AX057N2F40I2SG
Designer : Zeev_L, Shimon_A, Ran_Z
Title
Arria 10 - CONFIGURATION
Size C
Design Name : ETX-2I-10GX8.REV0.1I
Rev 0.0
Date: Thursday, June 04, 2020
Sheet 15 of 45



exist in RAD:
LF-IC-IS43TR16128B-093NBL - DDR3 128M*16,1066/2132,1.5V,ROHS,COMMERTIAL.
LF-IC-IS43TR16128B-093NBLI - DDR3 128M*16,1066/2132,1.5V,ROHS,INDUSTRIAL.
Clock
Address/ Command
Control
SDRAM DDR3
2Gb/256MByte
U33
IS43TR16128B-093NBLI
4Gb
2.2 pf compensation cap before the first component
VREFDQ & VREFCA come from the same power source but should be routed to and then decoupled separately at DDR3.
0.75V
Vref_DB_QM
VDD_1V5_ARRIA
VTT_0.75V
10AX057N2F40I2SG
BOM change of DM to 2xODT(120) = 240 ohm, Vil=0.5V<VilMax=0.65V Changed from 0 ohm with higher current consumption
Place if need by SI
Joint pad
Short trace
ENTU_DDR3_REFCLK_A+
ENTU_DDR3_REFCLK_A-
DDR3_DB_QM_RSV2_REFCK
DDR3_DB_QM_RSV2_REFCKN
1.1V_VICM
For VREFDQ & VREFCA :
• Use a 30 mil trace between the decoupling cap and the destination.
• Maintain a 15 mil clearance from other nets.
• Simplify implementation by routing VREF on the top signal trace layer.
• Isolate VREF and/or shield with ground.
• Decouple using distributed 0.01uf and 0.1uf capacitors by the regulator, controller, and DIMM slots. Place one 0.01uf and one 0.1uf near the VREF pin of each DIMM. Place one 0.1?f near the source of VREF, one near the VREF pin on the controller, and two between the controller and the first DIMM.
If 1.1_VICM will be used, assemble the inductor instead of the resistor, to get PI filter
VDD_1.1V
VREFDQ_DB_QM
VREFCA_DB_QM

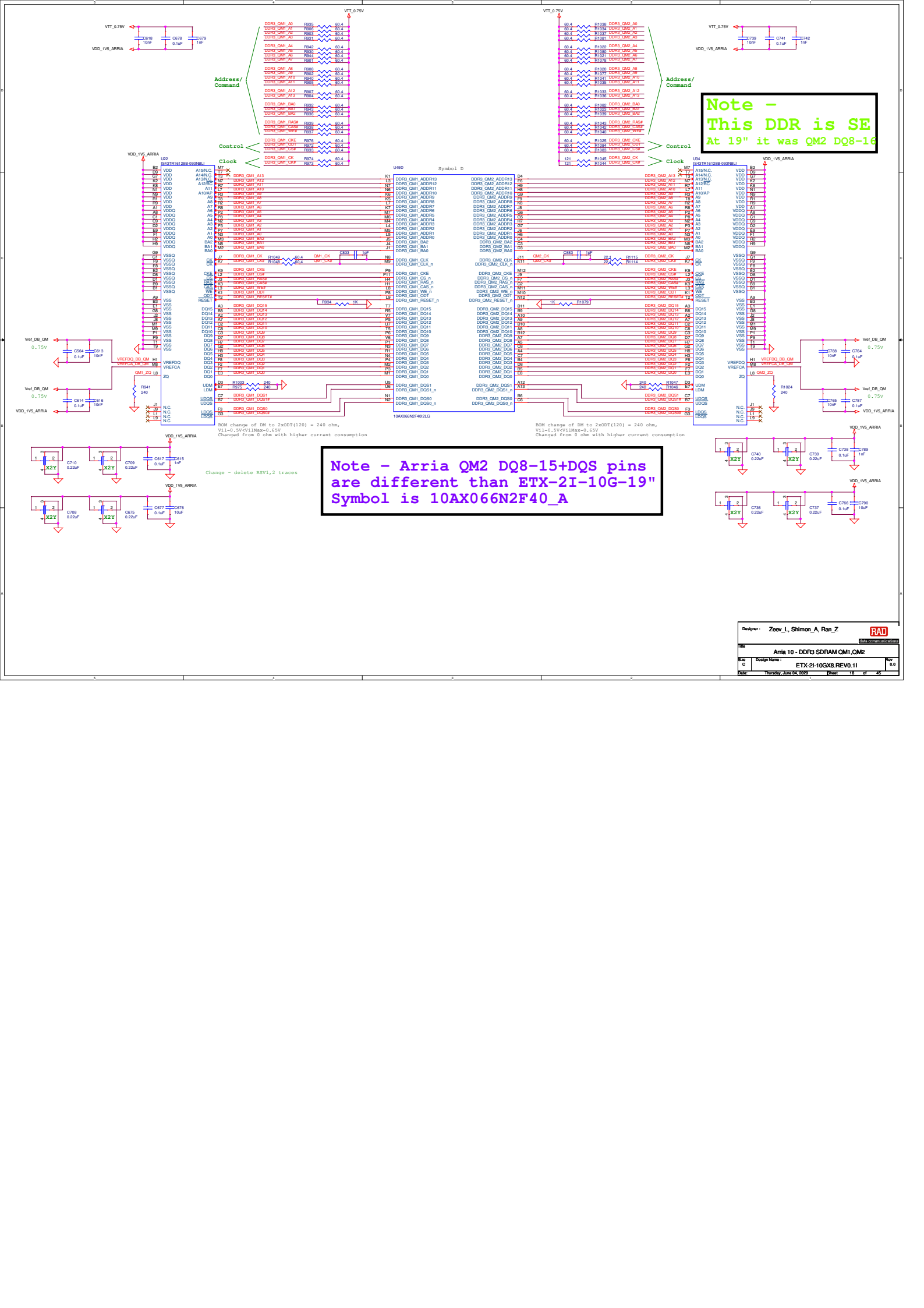
Designer : Zeev_L, Shimon_A, Ran_Z		RAD data communications
Title: Arria 10 - DDR3 SDRAM DB1		
Size: D	Design Name : ETX-2I-10GX8.REV0.1I	Rev: 0.0
Date: Thursday, June 04, 2020	Sheet 16 of 45	

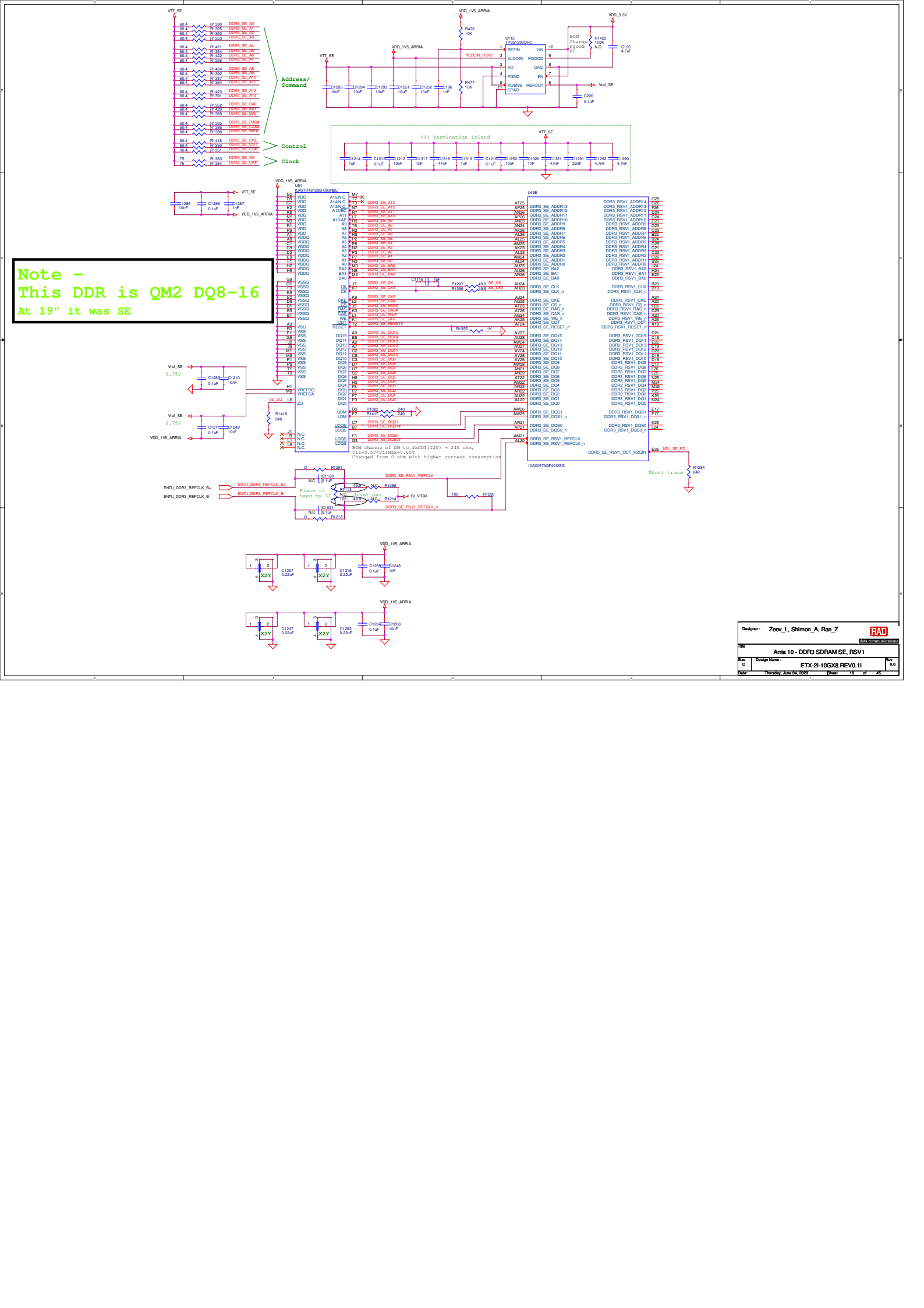


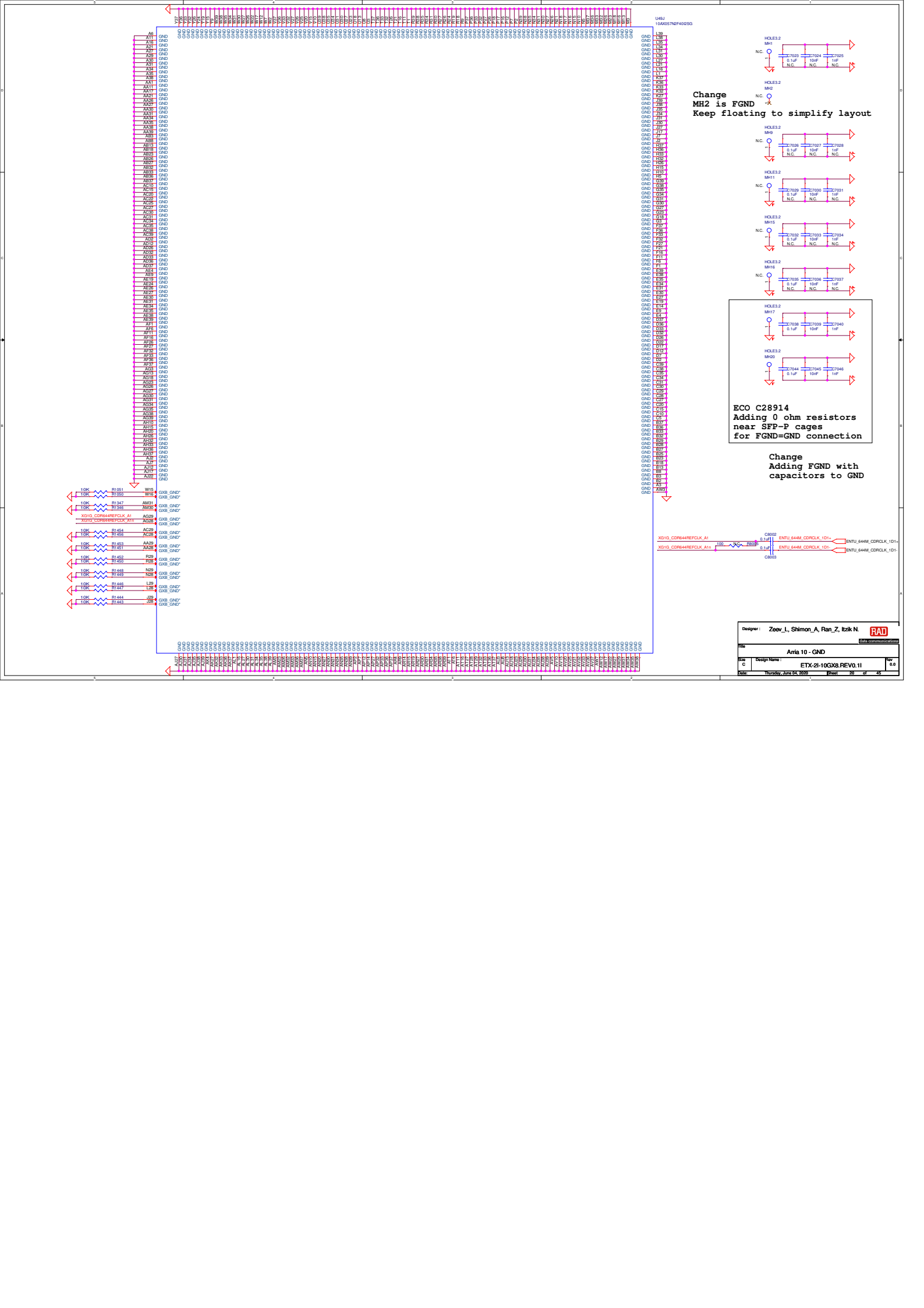
SDRAM DDR3
2Gb/256MByte
Clock
Address/
Command
Control
BOM change of DM to 2xODT(120) = 240 ohm,
Vil<0.5V<VilMax=0.65V
Changed from 0 ohm with higher current consumption
VREFDQ & VREFCA
come from the same power source
but should be routed to and then
decoupled separately at DDR3.
0.75V
For VREFDQ & VREFCA :
• Use a 30 mil trace between the decoupling cap and the destination.
• Maintain a 15 mil clearance from other nets.
• Simplify implementation by routing VREF on the top signal trace layer.
• Isolate VREF and/or shield with ground.
• Decouple using distributed 0.01uf and 0.1uf capacitors by the regulator, controller, and DIMM slots. Place one 0.01uf and one 0.1uf near the VREF pin of each DIMM.
Place one 0.1?f near the source of VREF, one near the VREF pin on the controller, and two between the controller and the first DIMM.

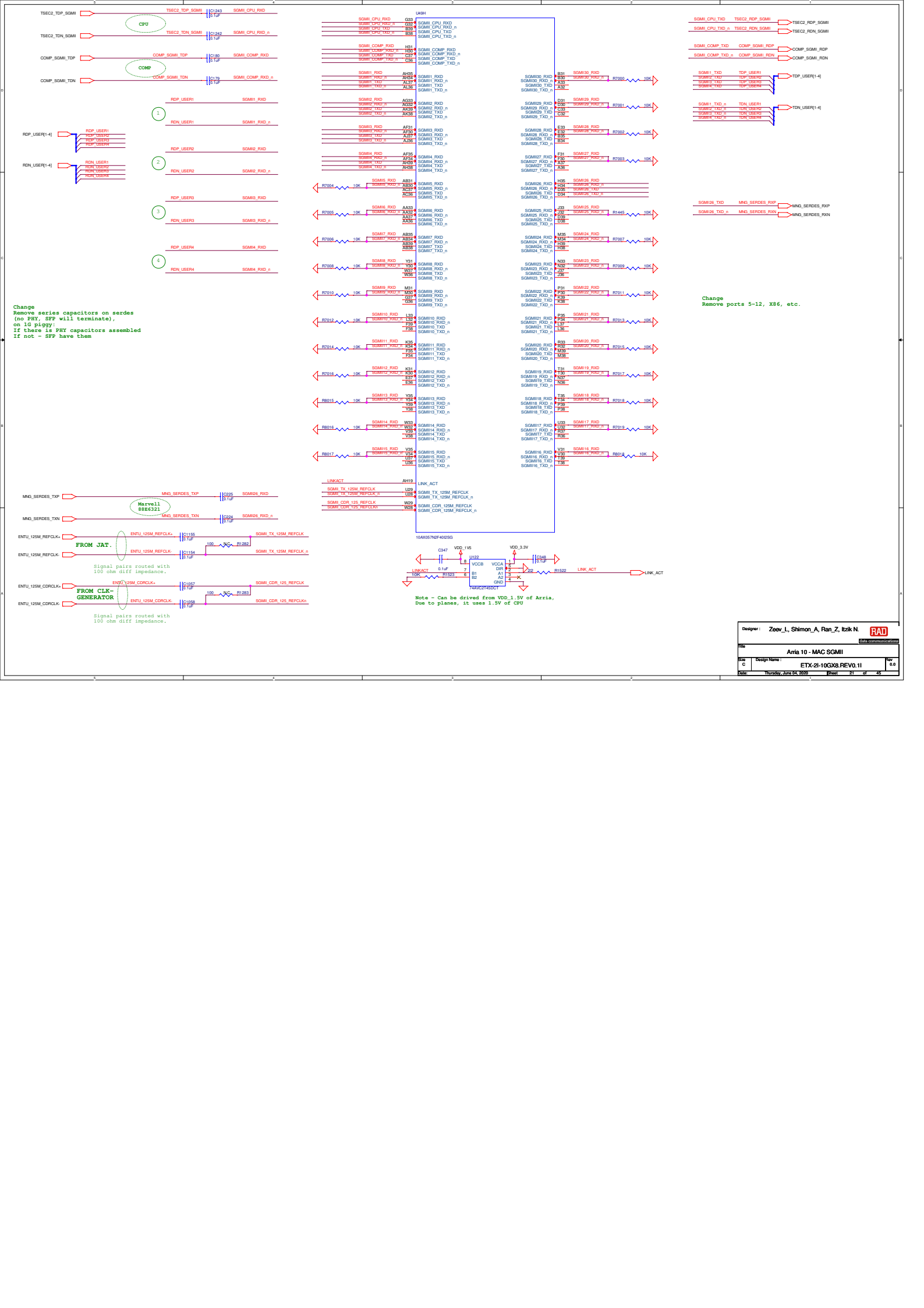
Designer :	Zeev_L, Shimon_A, Ran_Z
Title	Arria 10 - DDR3 SDRAM DB2
Size D	Design Name : ETX-2I-10GX8.REV0.1I
Rev	0.0
Date:	Thursday, June 04, 2020
Sheet	17 of 45

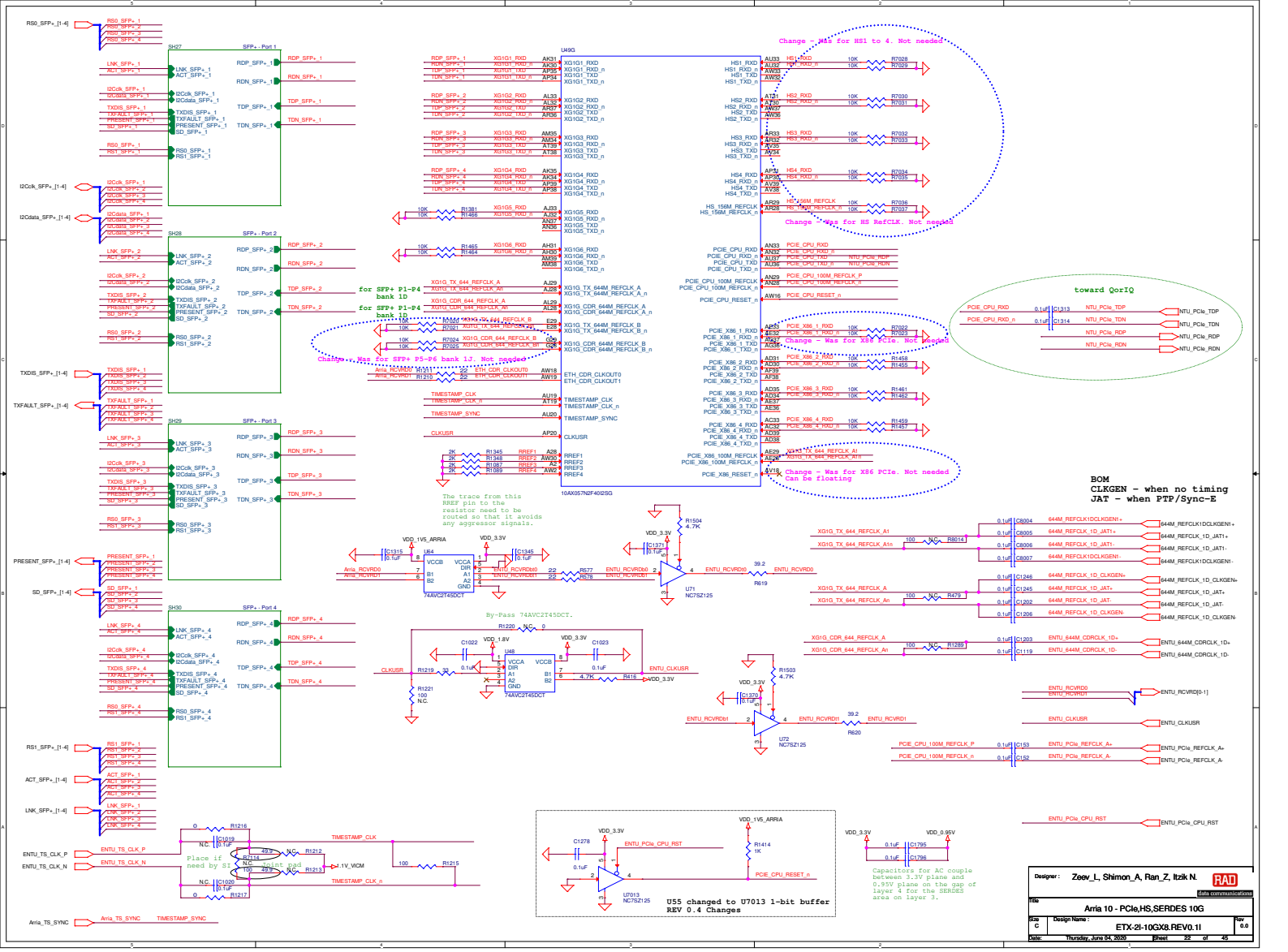
RAD data communications

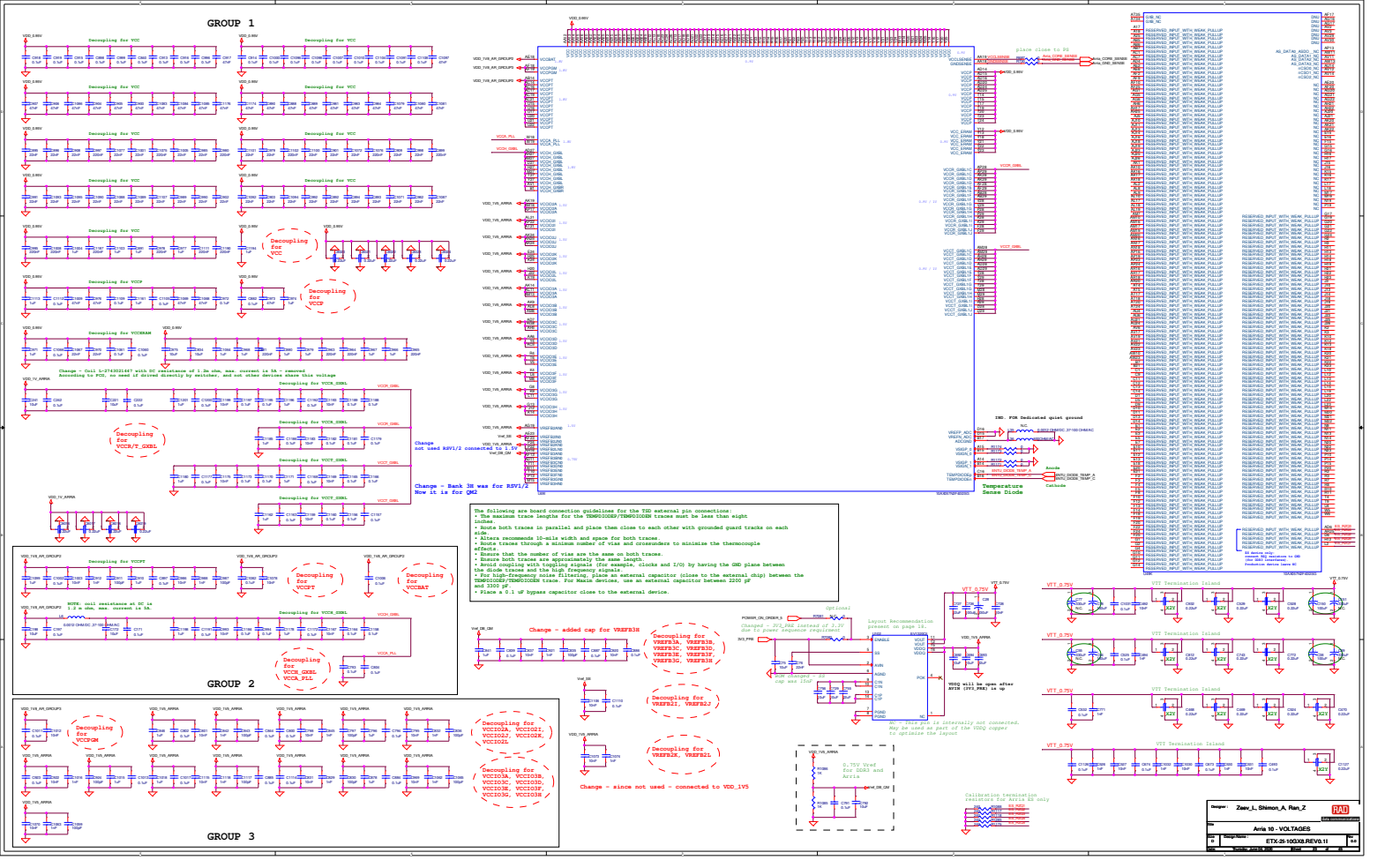

Note -
This DDR is SE
At 19" it was QM2 DQ8-16
Note - Arria QM2 DQ8-15+DQS pins are different than ETX-2I-10G-19" Symbol is 10AX066N2F40_A
Change - delete RSV1,2 traces
BOM change of DM to 2xODT(120) = 240 ohm, Vil=0.5VVilMax=0.65V Changed from 0 ohm with higher current consumption
Address/ Command
Control
Clock
Designer : Zeev_L, Shimon_A, Ran_Z
Title
Arria 10 - DDR3 SDRAM QM1,QM2
Size C
Design Name : ETX-2I-10GX8.REV0.1I
Rev 0.0
Date: Thursday, June 04, 2020
Sheet 18 of 45

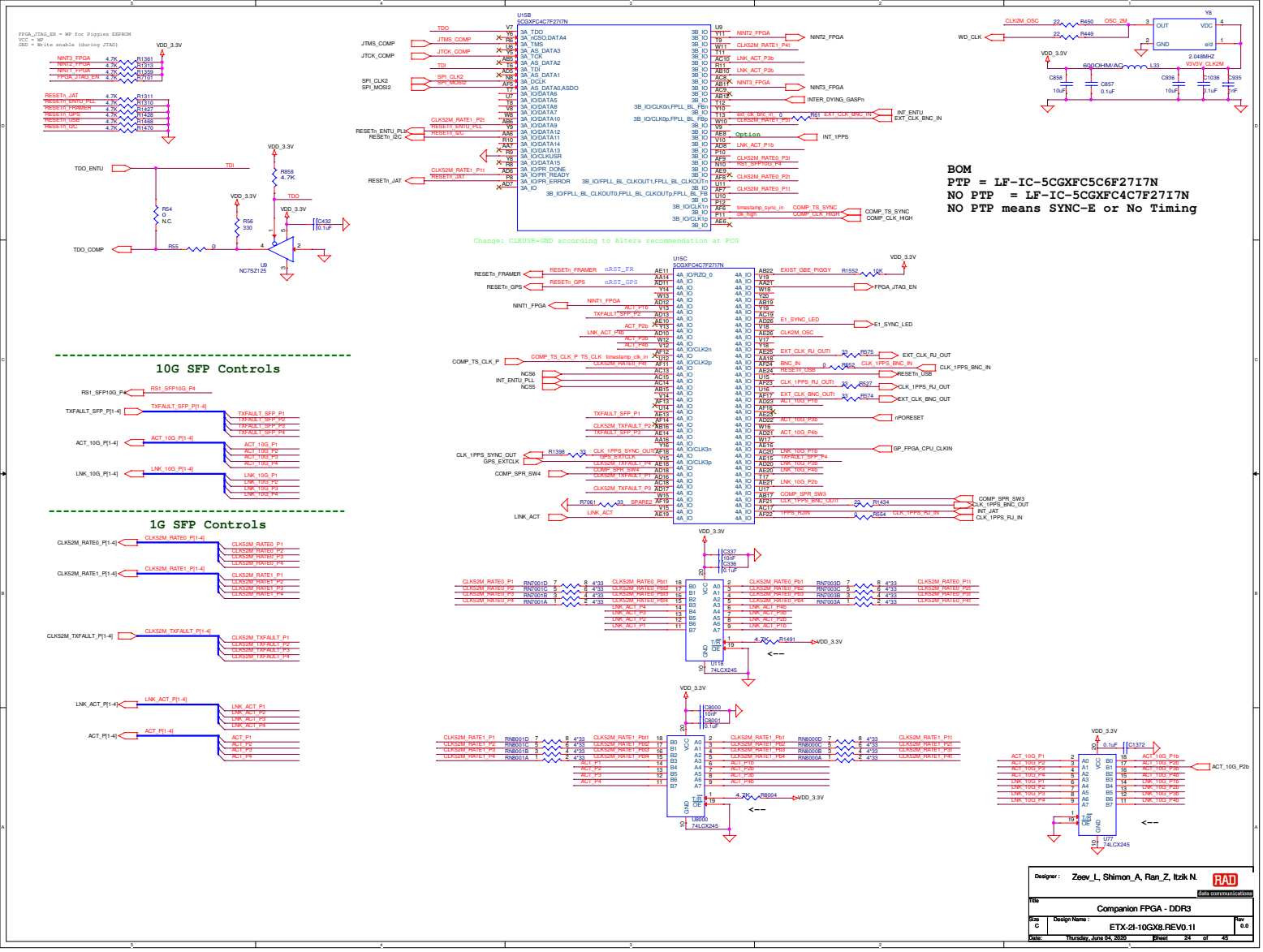

Note -
This DDR is QM2 DQ8-16
At 19" it was SE
Address/
Command
Control
Clock
VTT Termination Island
Short trace
Place if
need by SI
Test pad
BOM change of DM to 2xODT(120) = 240 ohm,
Vil=0.5*Vil1Max=0.65V
Changed from 0 ohm with higher current consumption
Designer : Zeev_L, Shimon_A, Ran_Z
Title
Arria 10 - DDR3 SDRAM SE, RSV1
Design Name :
ETX-2I-10GX8.REV0.1I
Size C
Rev 0.0
Date: Thursday, June 04, 2020
Sheet 19 of 45


U49J
10AX057N2F40I2SG
Change
MH2 is FGND
Keep floating to simplify layout
ECO C28914
Adding 0 ohm resistors
near SFP-P cages
for FGND=GND connection
Change
Adding FGND with
capacitors to GND
Designer : Zeev_I, Shimon_A, Ran_Z, Itzik N.
Title
Arria 10 - GND
Size C
Design Name : ETX-2I-10GX8.REV0.1I
Rev 0.0
Date: Thursday, June 04, 2020
Sheet 20 of 45


TSEC2_TDP_SGMII
CPU
TSEC2_TDN_SGMII
SGMII_CPU_RXD
SGMII_CPU_RXD_n
C1243 0.1uF
C1242 0.1uF
COMP_SGMII_TDP
COMP_SGMII_TDN
COMP
SGMII_COMP_RXD
SGMII_COMP_RXD_n
C180 0.1uF
C179 0.1uF
RDP_USER1
RDN_USER1
RDP_USER2
RDN_USER2
RDP_USER3
RDN_USER3
RDP_USER4
RDN_USER4
SGMII1_RXD
SGMII1_RXD_n
SGMII2_RXD
SGMII2_RXD_n
SGMII3_RXD
SGMII3_RXD_n
SGMII4_RXD
SGMII4_RXD_n
U49H
SGMII_CPU_TXD
SGMII_CPU_TXD_n
SGMII_COMP_TXD
SGMII_COMP_TXD_n
TSEC2_RDP_SGMII
TSEC2_RDN_SGMII
COMP_SGMII_RDP
COMP_SGMII_RDN
TDP_USER[1-4]
TDN_USER[1-4]
SGMII1_TXD
SGMII1_TXD_n
SGMII2_TXD
SGMII2_TXD_n
SGMII3_TXD
SGMII3_TXD_n
SGMII4_TXD
SGMII4_TXD_n
SGMII5_RXD
SGMII5_RXD_n
SGMII6_RXD
SGMII6_RXD_n
SGMII7_RXD
SGMII7_RXD_n
SGMII8_RXD
SGMII8_RXD_n
SGMII9_RXD
SGMII9_RXD_n
SGMII10_RXD
SGMII10_RXD_n
SGMII11_RXD
SGMII11_RXD_n
SGMII12_RXD
SGMII12_RXD_n
SGMII13_RXD
SGMII13_RXD_n
SGMII14_RXD
SGMII14_RXD_n
SGMII15_RXD
SGMII15_RXD_n
SGMII16_RXD
SGMII16_RXD_n
SGMII17_RXD
SGMII17_RXD_n
SGMII18_RXD
SGMII18_RXD_n
SGMII19_RXD
SGMII19_RXD_n
SGMII20_RXD
SGMII20_RXD_n
SGMII21_RXD
SGMII21_RXD_n
SGMII22_RXD
SGMII22_RXD_n
SGMII23_RXD
SGMII23_RXD_n
SGMII24_RXD
SGMII24_RXD_n
SGMII25_RXD
SGMII25_RXD_n
SGMII26_RXD
SGMII26_RXD_n
SGMII27_RXD
SGMII27_RXD_n
SGMII28_RXD
SGMII28_RXD_n
SGMII29_RXD
SGMII29_RXD_n
SGMII30_RXD
SGMII30_RXD_n
R7000 10K
R7001 10K
R7002 10K
R7003 10K
R1445 10K
R7007 10K
R7009 10K
R7011 10K
R7013 10K
R7015 10K
R7017 10K
R7018 10K
R7019 10K
R8018 10K
R7004 10K
R7005 10K
R7006 10K
R7008 10K
R7010 10K
R7012 10K
R7014 10K
R7016 10K
R8015 10K
R8016 10K
R8017 10K
LINKACT
LINK_ACT
SGMII_TX_125M_REFCLK
SGMII_TX_125M_REFCLK_n
SGMII_CDR_125_REFCLK
SGMII_CDR_125M_REFCLK_n
10AX057N2F40I2SG
C347 0.1uF
VDD_1V5
VDD_3.3V
U122
VCCB
VCCA
DIR
A1
A2
GND
B1
B2
74AVC2T245DCT
C348 0.1uF
R1523 10K
R1522 22
LINK_ACT
MNG_SERDES_RXP
MNG_SERDES_RXN
MNG_SERDES_TXP
MNG_SERDES_TXN
Marvell 88E6321
C225 0.1uF
C224 0.1uF
SGMII26_RXD
SGMII26_RXD_n
ENTU_125M_REFCLK+
ENTU_125M_REFCLK-
FROM JAT.
C1155 0.1uF
C1154 0.1uF
100 NC
R1282
SGMII_TX_125M_REFCLK
SGMII_TX_125M_REFCLK_n
Signal pairs routed with 100 ohm diff impedance.
ENTU_125M_CDRCLK+
ENTU_125M_CDRCLK-
FROM CLK-GENERATOR
C1057 0.1uF
C1058 0.1uF
R1283
SGMII_CDR_125_REFCLK
SGMII_CDR_125_REFCLKn
Change
Remove series capacitors on serdes
(no PHY, SFP will terminate),
on IG piggy:
If there is PHY capacitors assembled
If not - SFP have them
Change
Remove ports 5-12, X86, etc.
Note - Can be drived from VDD_1.5V of Arria,
Due to planes, it uses 1.5V of CPU
Designer : Zeev_I, Shimon_A, Ran_Z, Itzik N.
RAD
data communications
Title
Arria 10 - MAC SGMII
Size C
Design Name : ETX-2I-10GX8.REV0.1I
Rev 0.0
Date: Thursday, June 04, 2020
Sheet 21 of 45


Change - Was for HS1 to 4. Not needed
Change - Was for HS RefCLK. Not needed
toward QorIQ
Change - Was for SFP+ P5-P6 bank 1J. Not needed
Change - Was for X86 PCIe. Not needed
Change - Was for X86 PCIe. Not needed Can be floating
for SFP+ P1-P4 bank 1D
for SFP+ P1-P4 bank 1C
The trace from this RREF pin to the resistor need to be routed so that it avoids any aggressor signals.
By-Pass 74AVC2T45DCT.
Place if need by SI
U55 changed to U7013 1-bit buffer REV 0.4 Changes
Capacitors for AC couple between 3.3V plane and 0.95V plane on the gap of layer 4 for the SERDES area on layer 3.
BOM
CLKGEN - when no timing JAT - when PTP/Sync-E
Designer : Zeev_I, Shimon_A, Ran_Z, Itzik N.
Title
Arria 10 - PCIe,HS,SERDES 10G
Size C
Design Name : ETX-2I-10GX8.REV0.1I
Rev 0.0
Date: Thursday, June 04, 2020
Sheet 22 of 45


GROUP 1
Decoupling for VCC
Decoupling for VCCP
Decoupling for VCCBRAM
Decoupling for VCCR_GXBL
Change = added cap for VREFB3H
Change = since not used - connected to VDD_1V5
GROUP 2
GROUP 3
Decoupling for VCCIO2A, VCCIO2J, VCCIO2K, VCCIO2L
Decoupling for VCCIO3A, VCCIO3B, VCCIO3C, VCCIO3D, VCCIO3E, VCCIO3F, VCCIO3G, VCCIO3H
Decoupling for VREFB3A, VREFB3B, VREFB3C, VREFB3D, VREFB3E, VREFB3F, VREFB3G, VREFB3H
Decoupling for VREFB2L, VREFB2J
Decoupling for VREFB2K, VREFB2L
Temperature Sense Diode
Calibration termination resistors for Arria 10 only
0.75V Vref for DDR3 and Arria
VTT Termination Island
Designer: Zeev_L, Shimon_A, Ran_Z
Arria 10 - VOLTAGES
ETX-20-10GX8.REV0.11



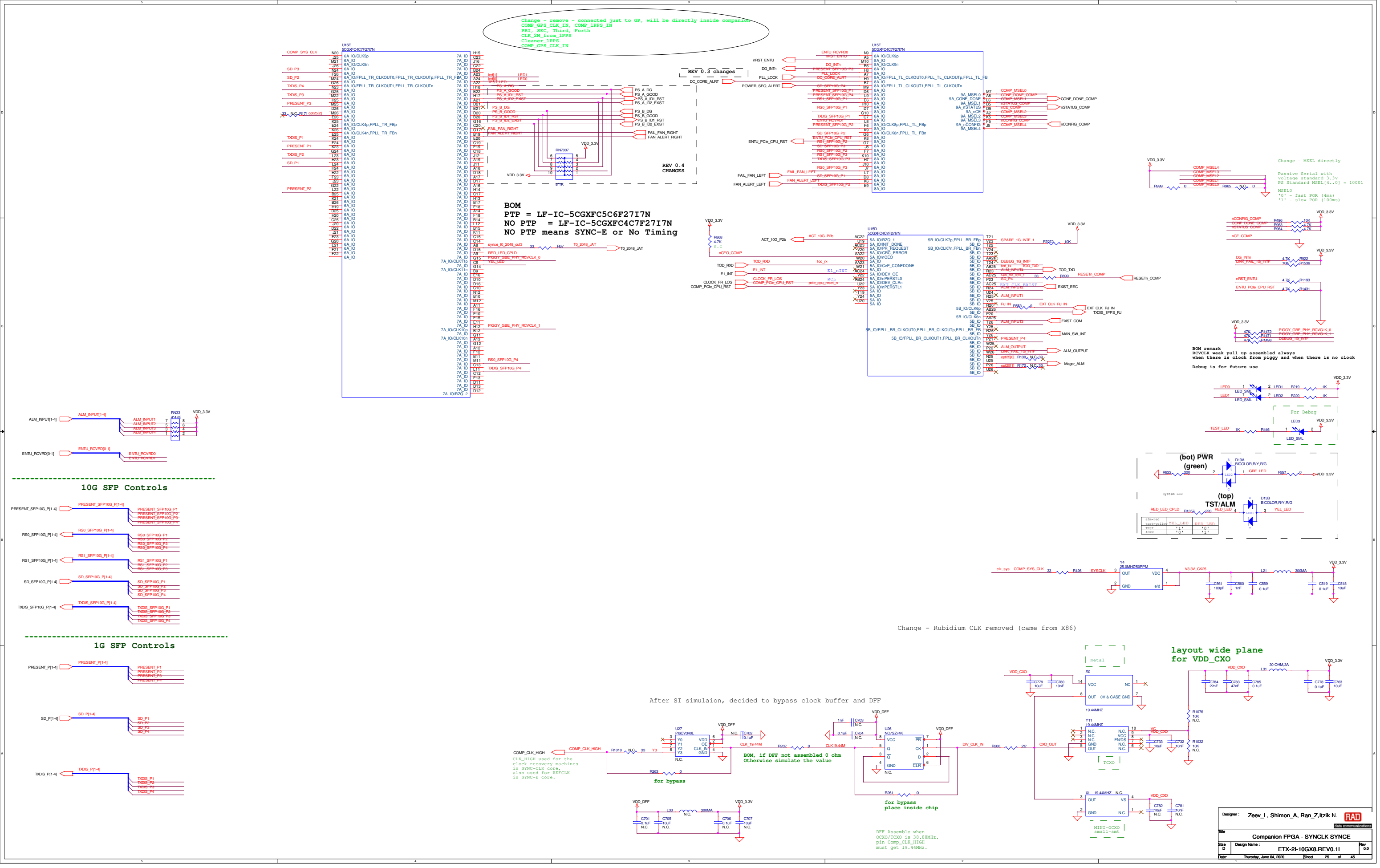
BOM
PTP = LF-IC-5CGXFC5C6F27I7N
NO PTP = LF-IC-5CGXFC4C7F27I7N
NO PTP means SYNC-E or No Timing

Change: CLKUSR=GND according to Altera recommendation at PCG

10G SFP Controls

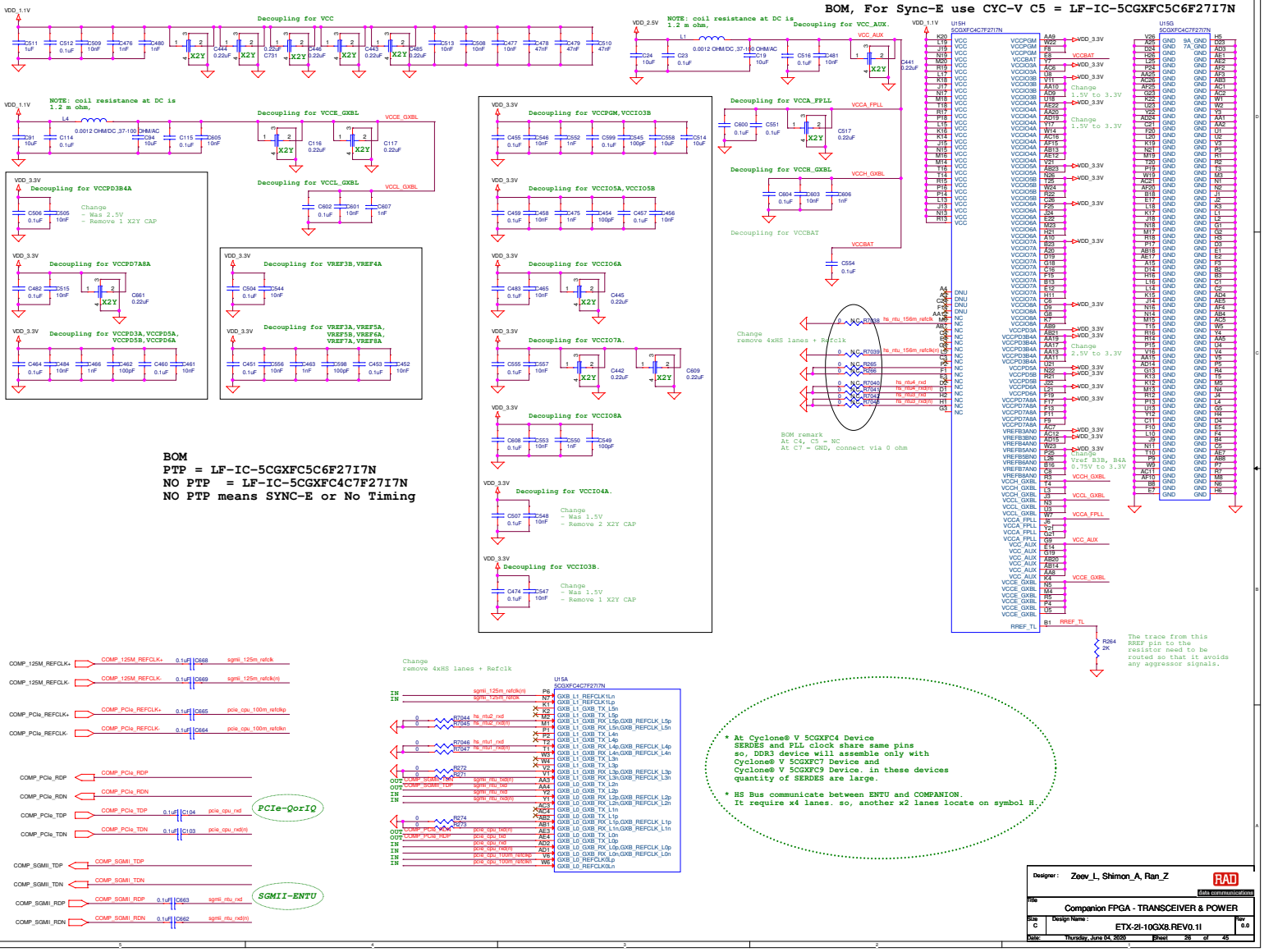
1G SFP Controls

Designer :	Zeev_I, Shimon_A, Ran_Z, Itzik N.	RAD data communications	
Title	Companion FPGA - DDR3		
Size C	Design Name : ETX-2I-10GX8.REV0.1I		Rev 0.0
Date: Thursday, June 04, 2020	Sheet 24 of 45		



Change - remove - connected just to GP, will be directly inside companion
COMP_GPS_CLK_IN, COMP_1PPS_IN
PRS, SEC, Third, Forth
CLK_IN from 1PPS
Cleaner_1PPS
COMP_GPS_CLK_IN
REV 0.3 changes
REV 0.4 CHANGES
BOM
PTP = LF-IC-5CGXFC5C6F27I7N
NO PTP = LF-IC-5CGXFC4C7F27I7N
NO PTP means SYNC-E or No Timing
10G SFP Controls
1G SFP Controls
Change - MSEL directly
BOM remark
RCVCLK weak pull up assembled always
when there is clock from piggy and when there is no clock
Debug is for future use
For Debug
(bot) PWR (green)
(top) TST/ALM
Change - Rubidium CLK removed (came from X86)
layout wide plane for VDD_CXO
After SI simulaion, decided to bypass clock buffer and DFF
CLK_8
for bypass
BOM, if DFF not assembled 0 ohm
Otherwise simulate the value
for bypass place inside chip
Zeev_L, Shimon_A, Ran_Z,Itzik N.
Companion FPGA - SYNCLK SYNCE
ETX-2I-10GX8.REV0.1I
Thursday, June 04, 2020

BOM, For Sync-E use CYC-V C5 = LF-IC-5CGXFC5C6F27I7N

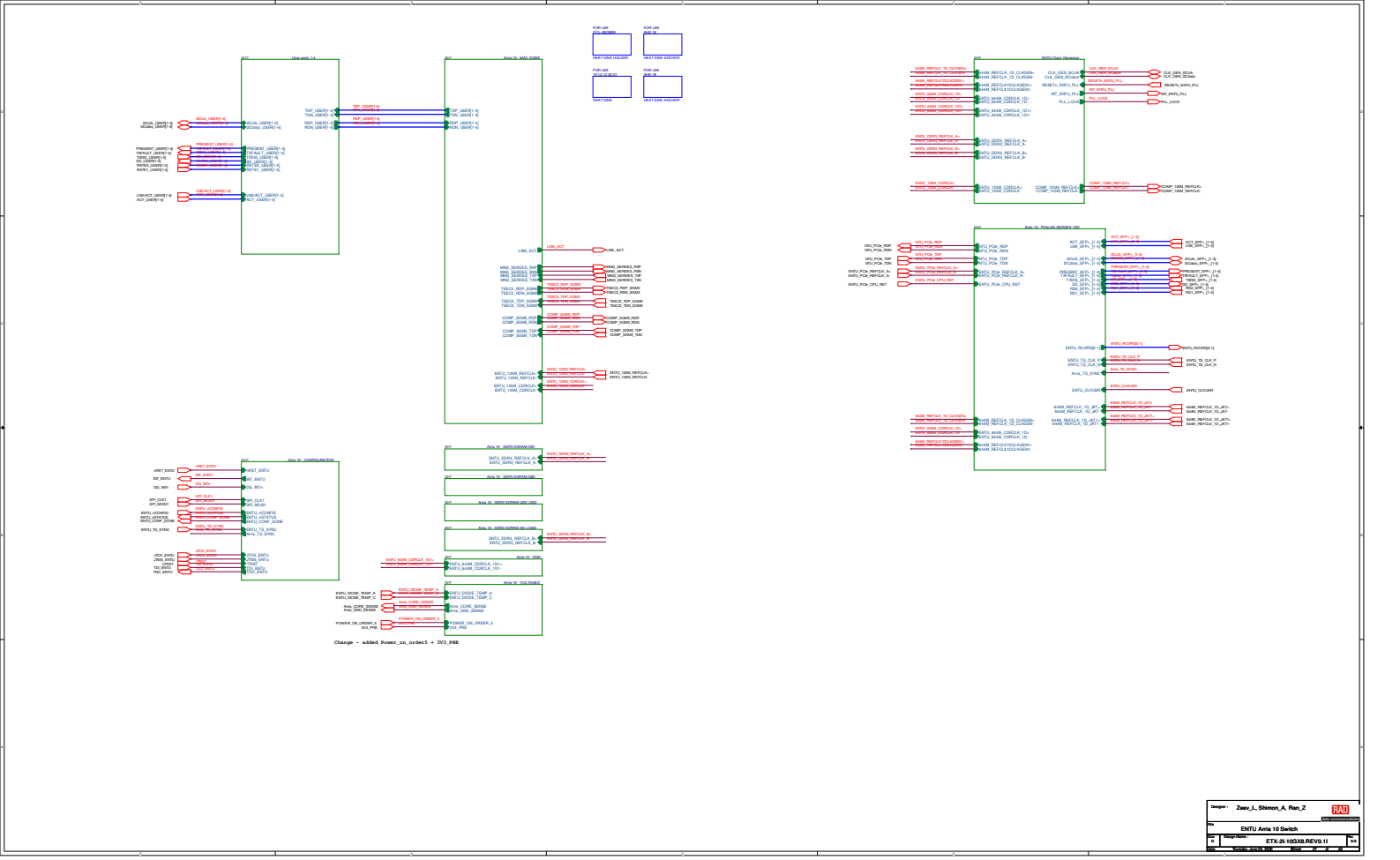


BOM
PTP = LF-IC-5CGXFC5C6F27I7N
NO PTP = LF-IC-5CGXFC4C7F27I7N
NO PTP means SYNC-E or No Timing

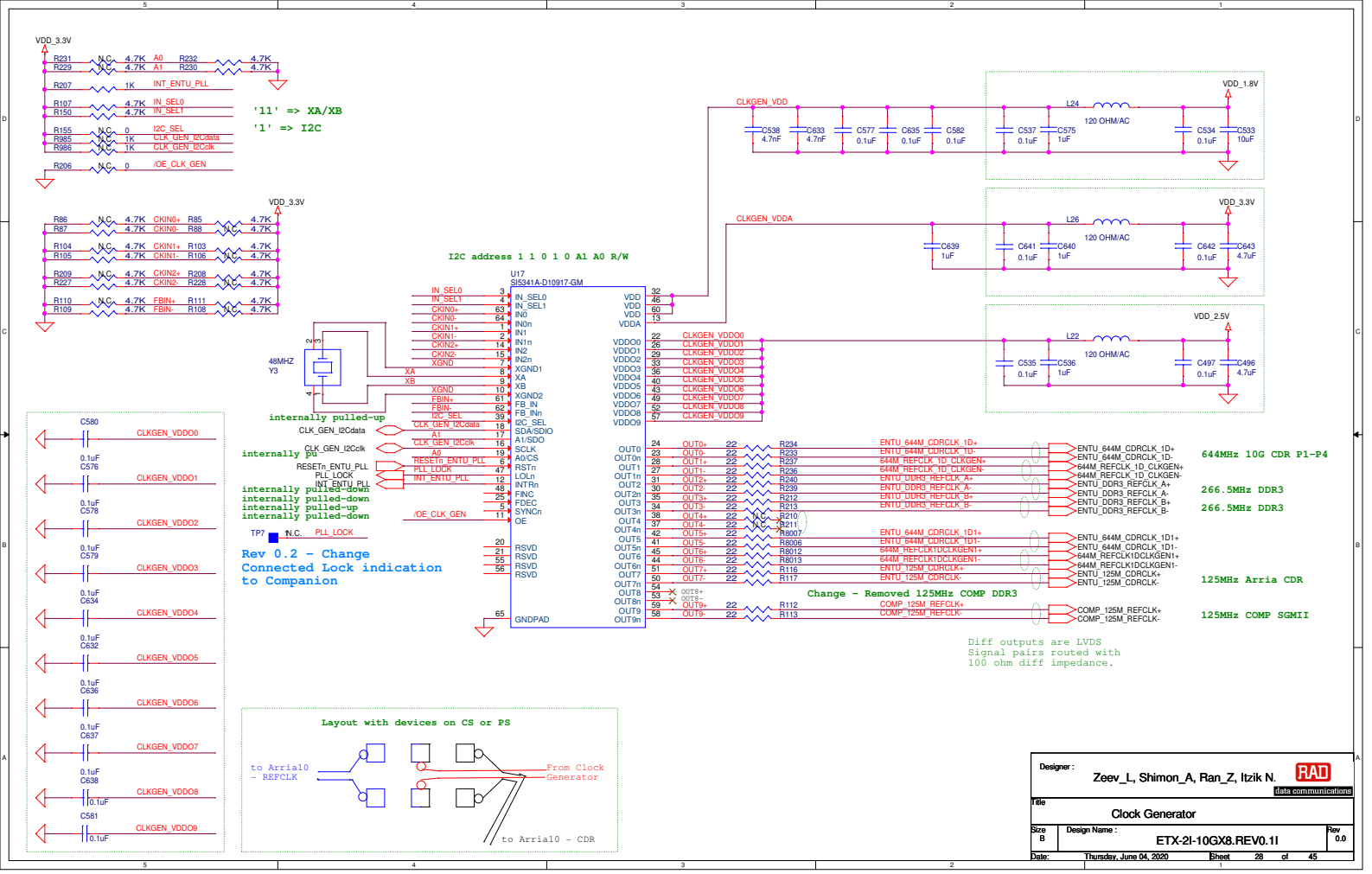
* At Cyclone® V 5CGXFC4 Device SERDES and PLL clock share same pins so, DDR3 device will assemble only with Cyclone® V 5CGXFC7 Device and Cyclone® V 5CGXFC9 Device. in these devices quantity of SERDES are large.

* HS Bus communicate between ENTU and COMPANION. It require x4 lanes. so, another x2 lanes locate on symbol H.

Designer :	Zeev_I, Shimon_A, Ran_Z
Title	Companion FPGA - TRANSCEIVER & POWER
Size C	Design Name : ETX-2I-10GX8.REV0.1I
Rev 0.0	
Date: Thursday, June 04, 2020	Sheet 26 of 45

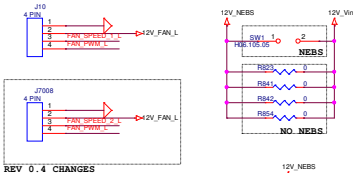


Designer:	Zaev_L, Shimon_A, Ran_Z
Title	ENTU Ania 10 Switch
Size: D	Design Name: ETX-26-10GX8.REV0.1I
Rev: 0.0	
Date: Tuesday, April 19, 2022	Sheet 1 of 25



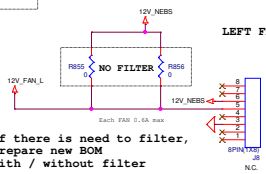
Designer :	Zeev_L, Shimon_A, Ran_Z, Itzik N.
Title	Clock Generator
Size	B
Design Name :	ETX-2I-10GX8.REV0.1I
Rev	0.0
Date:	Thursday, June 04, 2020
Sheet	28 of 45

LEFT SIDE FANS



REV 0.4 CHANGES

LEFT FAN FILTER CONNECTOR

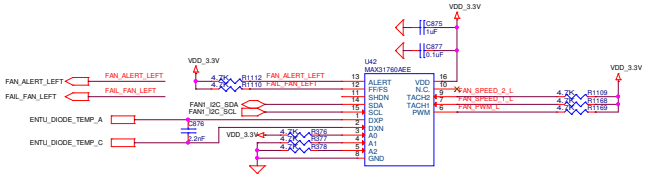


If filter is needed Assemble special filter 12V-FAN-SIP

If there is need to filter,
prepare new BOM
with / without filter

For now no filter resistor
always assemble

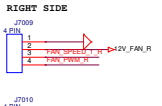
LEFT Fan Controlers

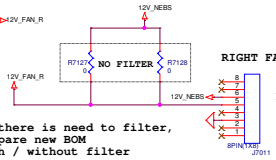


Device address is 1010 001 R/W
A2 A1 A0 = 0 0 1

REV 0.4 CHANGES

RIGHT SIDE





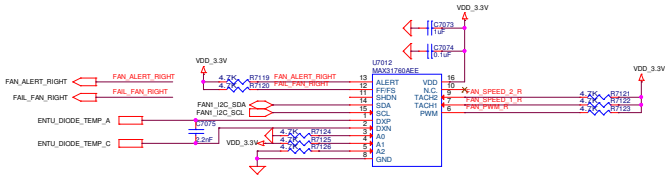
RIGHT FAN FILTER CONNECTOR

If filter is needed Assemble special filter 12V-FAN-SIP

If there is need to filter,
prepare new BOM
with / without filter

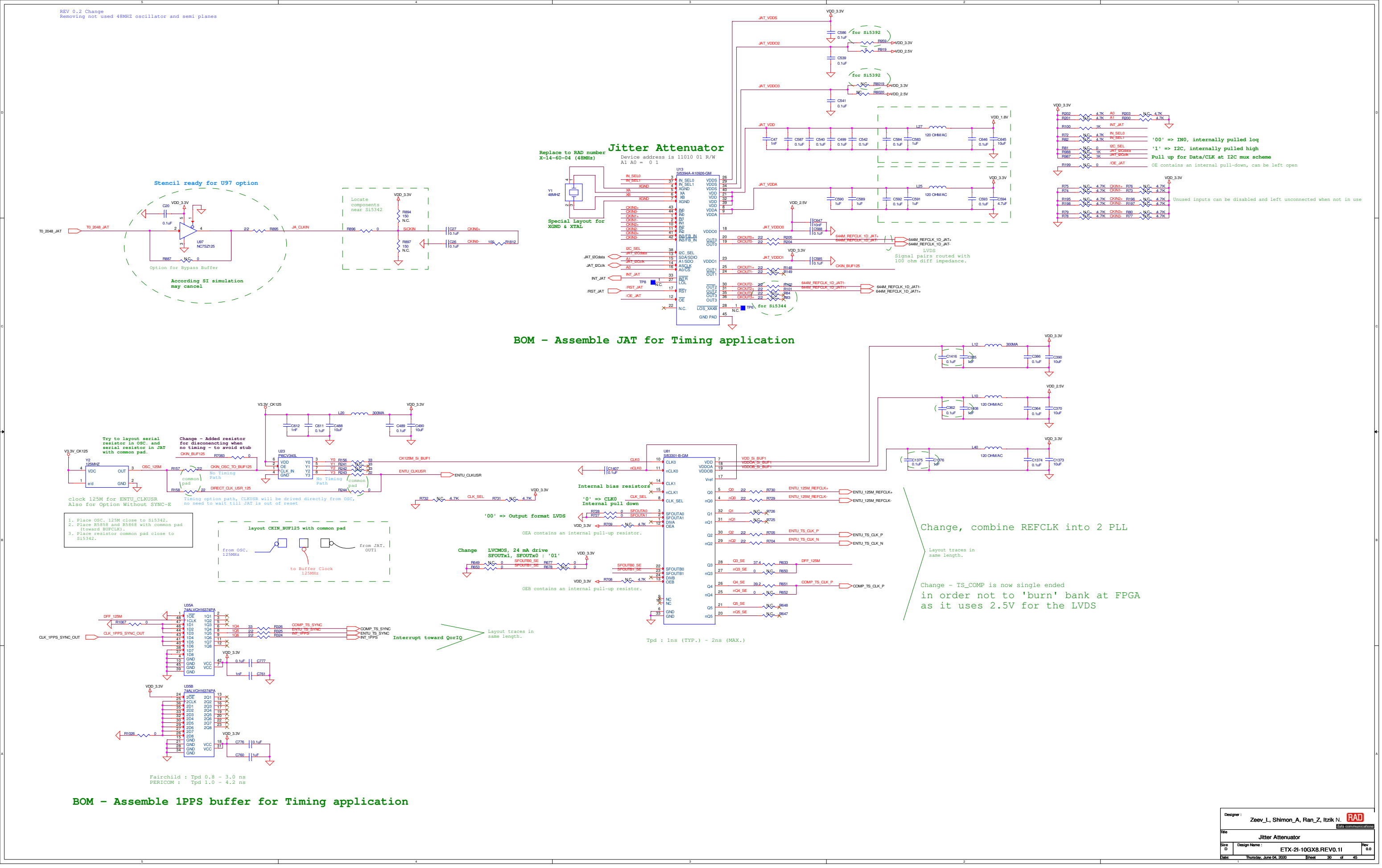
For now no filter resistor
always assemble

RIGHT Fan Controlers

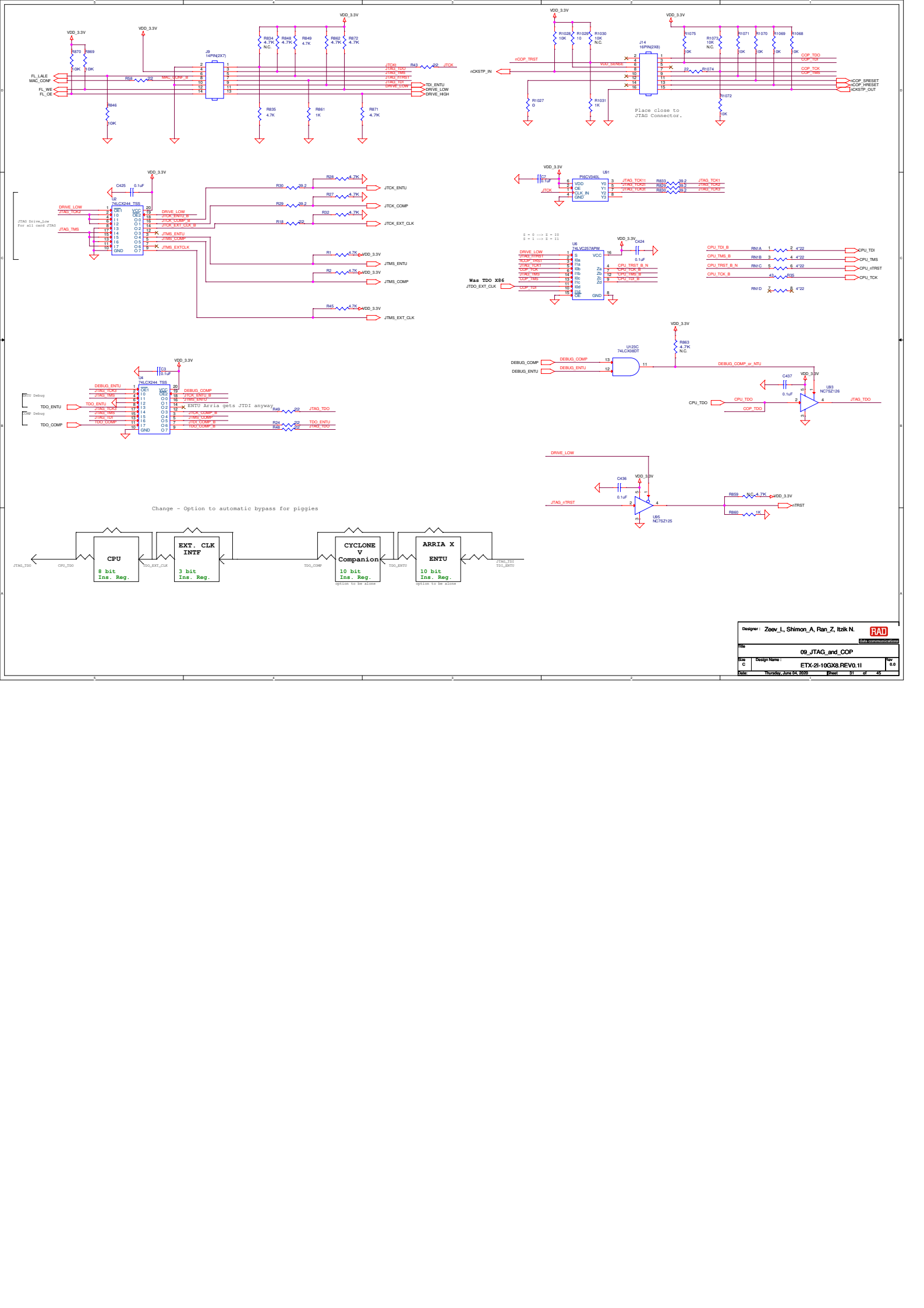


Device address is 1010 010 R/W
A2 A1 A0 = 0 1 0

Designer : Zeev_L, Shimon_A, Ran_Z			RAD data communications
Title: Fan Controlers			
Size: C	Design Name : ETX-2I-10GX8.REV0.11		Rev: 0.0
Date: Thursday, June 04, 2020	Sheet 29 of 45		



REV 0.2 Change
Removing not used 48MHZ oscillator and semi planes
Jitter Attenuator
Device address is 11010 01 R/W
A1 A0 = 0 1
Replace to RAD number X-14-60-04 (48MHz)
Special Layout for XGND & XTAL
Stencil ready for U97 option
Option for Bypass Buffer
According SI simulation may cancel
Locate components near Si5342
for Si5392
for Si5344
'00' => I2C, internally pulled low
'1' => I2C, internally pulled high
Pull up for Data/CLK at I2C bus scheme
OE contains an internal pull-down, can be left open
Unused inputs can be disabled and left unconnected when not in use
LVDS
Signal pairs routed with 100 ohm diff impedance.
BOM - Assemble JAT for Timing application
Try to layout serial resistor in OSC and serial resistor in JAT with common pad.
Change - Added resistor for disconnecting when no timing - to avoid stub
No Timing Path
common pad
Timing option path, CLKOUT will be driven directly from OSC, no need to wait till JAT is out of reset
clock 125M for ENTU_CLKUSR
Also for Option Without SYNC-E
1. Place OSC 125M close to Si5342.
2. Place R5856 and R5868 with common pad toward BUF125.
3. Place resistor common pad close to Si5342.
layout CKIN_BUF125 with common pad
from OSC 125MHz
to Buffer Clock 125MHz
from JAT OUT1
Internal bias resistors
'0' => CLK0
Internal pull down
'00' => Output format LVDS
OEA contains an internal pull-up resistor.
Change
LVCMOS, 24 mA drive
SFOUTx1, SFOUTx0 : '01'
OEB contains an internal pull-up resistor.
Tpd : 1ns (TYP.) - 2ns (MAX.)
Change, combine REFCLK into 2 PLL
Layout traces in same length.
Change - TS_COMP is now single ended
in order not to 'burn' bank at FPGA
as it uses 2.5V for the LVDS
Interrupt toward QorIQ
Layout traces in same length.
Fairchild : Tpd 0.8 - 3.0 ns
PERICOM : Tpd 1.0 - 4.2 ns
BOM - Assemble 1PPS buffer for Timing application
Designer : Zeev_L, Shimon_A, Ran_Z, Itzik N.
RAD
Title: Jitter Attenuator
Size D
Design Name : ETX-2I-10GX8.REV0.1I
Rev 0.3
Date: Thursday, June 04, 2020
Sheet 30 of 45


VDD_3.3V
FL_LALE
MAC_CONF
FL_WE
FL_OE
R870
R869
10K
R58
22
MAC_CONF_B
J9
14PIN(2X7)
R834
4.7K
N.C.
R848
4.7K
R849
4.7K
R862
4.7K
R872
4.7K
JTCK
JTAG_TDO
JTAG_TMS
JTAG_nTRST
JTAG_TDI
DRIVE_LOW
R43
TDI_ENTU
DRIVE_LOW
DRIVE_HIGH
R846
R835
4.7K
R861
1K
R871
4.7K
nCKSTP_IN
nCOP_TRST
VDD_SENSE
J14
16PIN(2X8)
R1028
10K
R1029
10
R1030
10K
N.C.
R1075
10K
R1073
10K
N.C.
R1071
10K
R1070
10K
R1069
10K
R1068
10K
COP_TDO
COP_TDI
COP_TCK
COP_TMS
R1074
22
nCOP_SRESET
nCOP_HRESET
nCKSTP_OUT
R1027
0
R1031
1K
R1072
10K
Place close to
JTAG Connector.
U2
74LCX244_TSS
C425
0.1uF
DRIVE_LOW
JTAG_TCRZ
JTAG_TMS
JTAG Drive_Low
For all card JTAG
JTCK_ENTU_B
JTCK_COMP_B
JTCK_EXT_CLK_B
JTMS_ENTU
JTMS_COMP
JTMS_EXTCLK
R30
39.2
R27
39.2
R29
39.2
R18
22
R28
4.7K
R32
4.7K
JTCK_ENTU
JTCK_COMP
JTCK_EXT_CLK
R1
4.7K
R2
4.7K
R45
4.7K
JTMS_ENTU
JTMS_COMP
JTMS_EXT_CLK
U91
P16CV340L
C7
0.1uF
JTCK
JTAG_TCK11
JTAG_TCK21
JTAG_TCK31
R833
R829
R830
39.2
JTAG_TCK1
JTAG_TCK2
JTAG_TCK3
U8
74LVC257APW
C424
0.1uF
S = 0 ---> Z = I0
S = 1 ---> Z = I1
DRIVE_LOW
JTAG_nTRST
COP_TRST
JTAG_TCK1
COP_TCK
JTAG_TMS
COP_TMS
COP_TDI
CPU_TRST_B_N
CPU_TCK_B
CPU_TMS_B
CPU_TDI_B
Was TDO X86
JTDO_EXT_CLK
CPU_TDI_B
CPU_TMS_B
CPU_TRST_B_N
CPU_TCK_B
RN1A
RN1B
RN1C
RN1D
4*22
R35
CPU_TDI
CPU_TMS
CPU_nTRST
CPU_TCK
U4
74LCX244_TSS
C3
0.1uF
DEBUG_ENTU
DEBUG_COMP
TDO_ENTU
TDO_COMP
ENTU Debug
COMP Debug
JTCK_ENTU_B
JTMS_ENTU
JTMS_COMP
JTDI_COMP_B
TDO_COMP_B
ENTU Arria gets JTDI anyway
R49
22
R24
22
R48
22
JTAG_TDO
TDO_ENTU
U1:23C
74LCX08DT
DEBUG_COMP
DEBUG_ENTU
R863
4.7K
N.C.
DEBUG_COMP_or_NTU
C437
0.1uF
U93
NC7SZ126
CPU_TDO
COP_TDO
JTAG_TDO
DRIVE_LOW
C436
0.1uF
JTAG_nTRST
U95
NC7SZ125
R859
NC_4.7K
R860
1K
nTRST
Change - Option to automatic bypass for piggies
JTAG_TDO
CPU_TDO
CPU
8 bit
Ins. Reg.
TDO_EXT_CLK
EXT. CLK
INTF
3 bit
Ins. Reg.
TDO_COMP
CYCLONE
V
Companion
10 bit
Ins. Reg.
option to be alone
TDO_ENTU
ARRIA X
ENTU
10 bit
Ins. Reg.
option to be alone
JTAG_TDI
TDI_ENTU
Designer : Zeev_L, Shimon_A, Ran_Z, Itzik N.
RAD
data communications
Title
09_JTAG_and_COP
Size
C
Design Name :
ETX-2I-10GX8.REV0.1I
Rev
0.0
Date:
Thursday, June 04, 2020
Sheet
31
of
45

POWER CONNECTOR

J7001
4B STRAIGHT PIN
1 2 3 4
12V_PS
12V_PS

FLAT CABLE connector for Backplane signals

SIGNAL CONNECTOR

CN1
16PIN(2X8)

PS_B_ID2_EXIST	2	1	PS_B_ID1_RST
PS_B_GOOD	4	3	PS_B_DG
12V_PS	6	5	PS_A_ID2_EXIST
	8	7	PS_A_ID1_RST
PS_A_GOOD	10	9	PS_A_DG
	12	11	POWER_SEQ_I2Cclk
	14	13	POWER_SEQ_I2Cdata
	16	15	

FANS_ACTIVE2
FANS_HD_LMI_FAIL
FANS_HD_FAIL
FANS_ON_SPEED_CNT
disconnected signals

PS A = LEFT PS signals

PS_A_DG → PS_A_DG
PS_A_GOOD → PS_A_GOOD
PS_A_ID1_RST → PS_A_ID1_RST
PS_A_ID2_EXIST → PS_A_ID2_EXIST

PS B = RIGHT PS signals

PS_B_DG → PS_B_DG
PS_B_GOOD → PS_B_GOOD
PS_B_ID1_RST → PS_B_ID1_RST
PS_B_ID2_EXIST → PS_B_ID2_EXIST

REV 0.4 CHANGES

For PS ID reading

I2C address for PS:
1 0 1 0 A2 A1 A0 R/W
A2, A1 = 0, A0:
Right PS- ADD0 = 0;
Left PS - ADD0 = 1;

FAN_CONTROL

REV 0.4 CHANGES

FAIL_FAN_LEFT → FAIL_FAN_LEFT
FAN_ALERT_LEFT → FAN_ALERT_LEFT
FAIL_FAN_RIGHT → FAIL_FAN_RIGHT
FAN_ALERT_RIGHT → FAN_ALERT_RIGHT
FAN1_I2C_SDA → FAN1_I2C_SDA
FAN1_I2C_SCL → FAN1_I2C_SCL
ENTU_DIODE_TEMP_C → ENTU_DIODE_TEMP_C
ENTU_DIODE_TEMP_A → ENTU_DIODE_TEMP_A

FAN_CONTROL

12V_Vin
C53 330uF
C45 330uF

Change - added for filtering input ripple of DC/DC

Change - Added for Arria DDR VTT termination

3V3_PRE → 3V3_PRE

VOLTAGE_CONVERTERS

Arria_GND_SENSE
Arria_CORE_SENSE
COM_I2Cclk
COM_I2Cdata
COM_ALR_I2Cclk
COM_ALR_I2Cdata
DC_CORE_ALRT
3V3_PRE
1V5_PRE
1V8_PRE
PS3.3_SIG_G
PS2.5_SIG_G
PS1.0_SIG_G
PS1.1_SIG_G
PS0.95_SIG_G
PS1.5_SIG_G
PS1.8_SIG_G
POWER_ON_ORDER_5n
POWER_ON_ORDER_1n
POWER_ON_ORDER_4n
POWER_ON_ORDER_2n
POWER_ON_ORDER_5

VOLTAGE_CONVERTERS

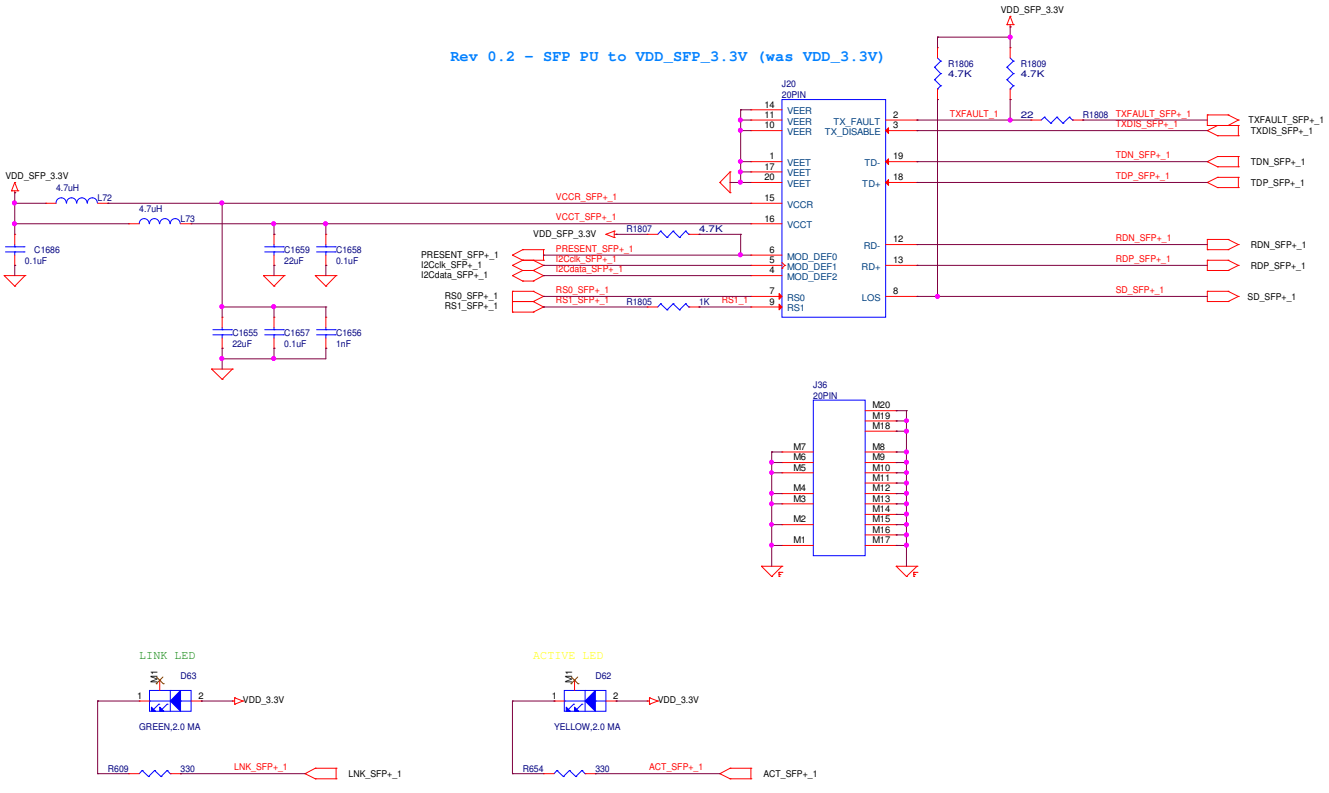
VOLTAGE_ CONTROL

3V3_PRE
1V5_PRE
1V8_PRE
PS3.3_SIG_G
PS2.5_SIG_G
PS1.0_SIG_G
PS1.1_SIG_G
PS0.95_SIG_G
PS1.5_SIG_G
PS1.8_SIG_G
POWER_ON_ORDER_5n
POWER_ON_ORDER_1n
POWER_ON_ORDER_4n
POWER_ON_ORDER_2n
INTER_DYING_GASPn
DG_INTn
POWER_SEQ_I2Cclk
POWER_SEQ_I2Cdata
POWER_SEQ_ALERT
PWR_SEQ_RESET_On
ENTU_CONF_DONE
JTAG_DRIVE_LOW
POWER_ON_ORDER_5

VOLTAGE_ CONTROL

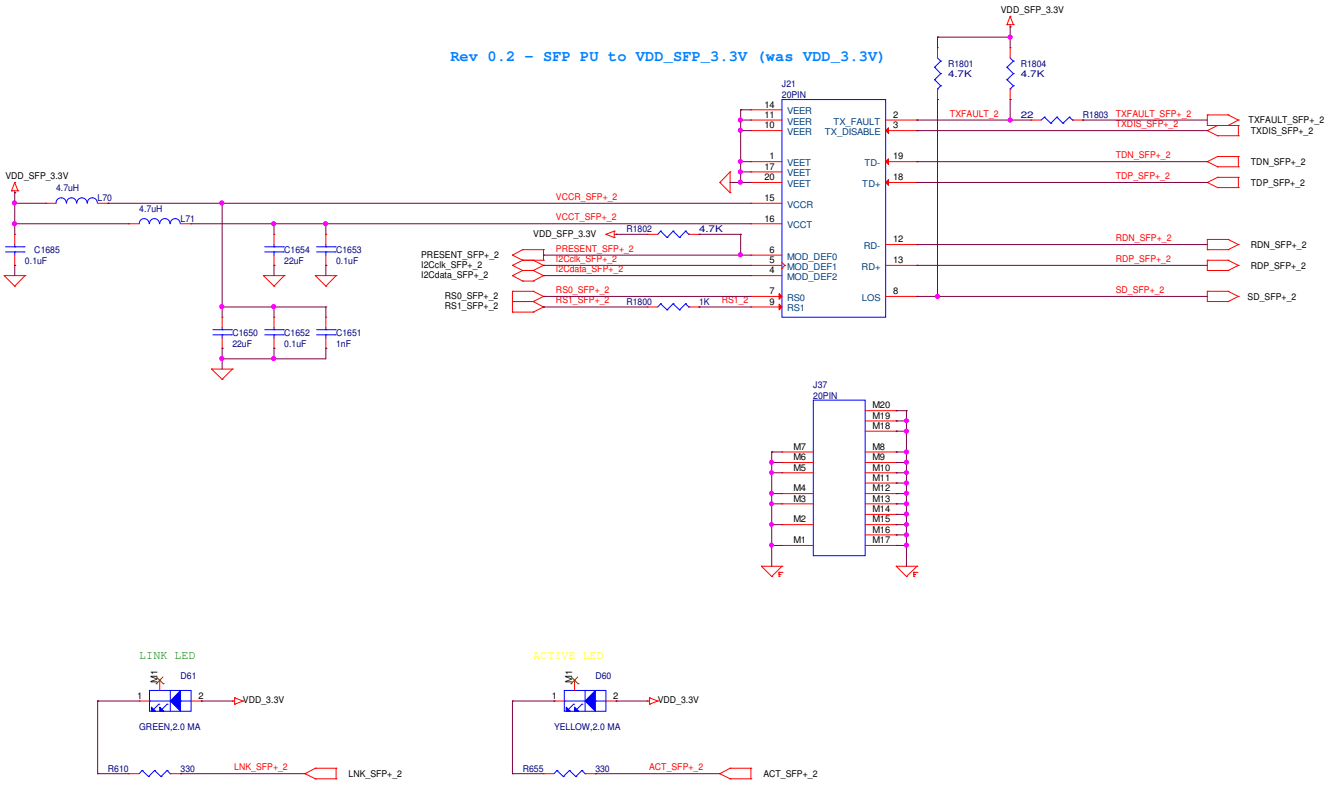
COM_ALR_I2Cclk
COM_ALR_I2Cdata

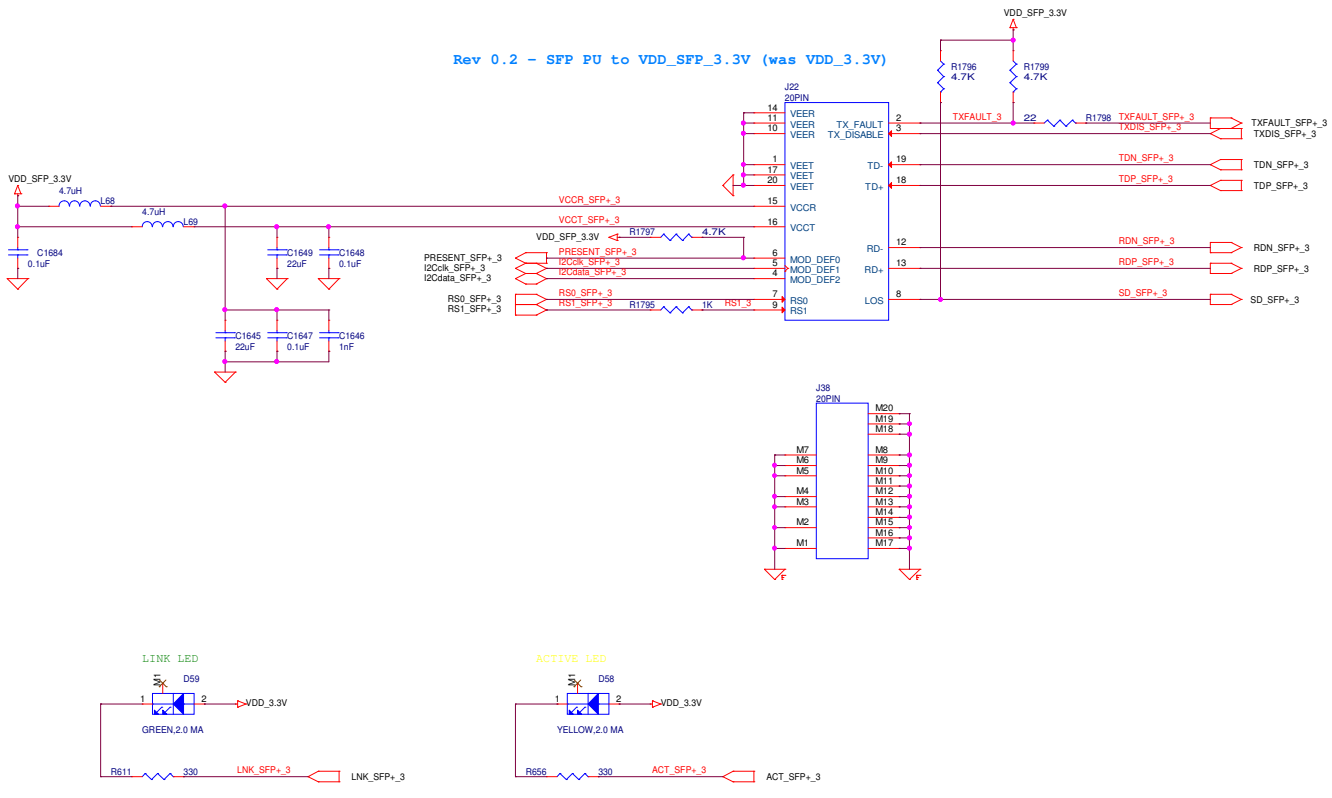
Designer :	Zeev_L, Shimon_A, Ran_Z, Itzik N.	RAD data communications	
Title	MAIN POWER		
Size B	Design Name : ETX-2I-10GX8.REV0.1I		Rev 0.0
Date: Thursday, June 04, 2020	Sheet 32 of 45		



LNK and ACT derived From Arria 10

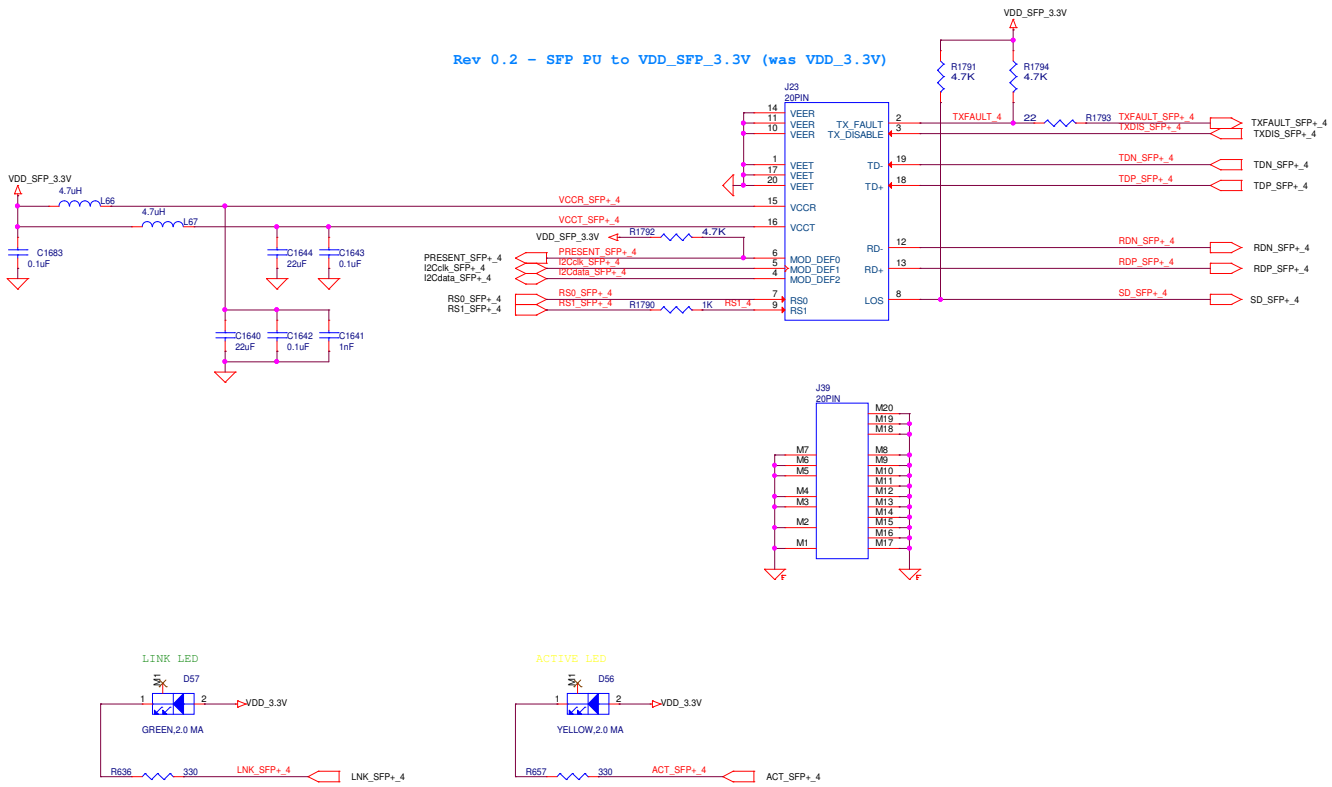
Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications	
Title	SFP+ - Port 1		
Size B	Design Name : ETX-2I-10GX8.REV0.1I		Rev 0.0
Date: Thursday, June 04, 2020	Sheet 33 of 45		


Rev 0.2 - SFP PU to VDD_SFP_3.3V (was VDD_3.3V)
VDD_SFP_3.3V
R1801 4.7K
R1804 4.7K
J21
20PIN
VEER
TX_FAULT
TX_DISABLE
VEET
TD-
TD+
VCCR
VCCT
RD-
RD+
LOS
MOD_DEF0
MOD_DEF1
MOD_DEF2
RS0
RS1
TXFAULT_2
R1803
TXFAULT_SFP+_2
TXDIS_SFP+_2
TXFAULT_SFP+_2
TXDIS_SFP+_2
TDN_SFP+_2
TDP_SFP+_2
RDN_SFP+_2
RDP_SFP+_2
SD_SFP+_2
4.7uH
L70
L71
C1685 0.1uF
C1654 22uF
C1653 0.1uF
C1650 22uF
C1652 0.1uF
C1651 1nF
VCCR_SFP+_2
VCCT_SFP+_2
R1802 4.7K
PRESENT_SFP+_2
I2Cclk_SFP+_2
I2Cdata_SFP+_2
RS0_SFP+_2
RS1_SFP+_2
R1800 1K
J37
20PIN
LINK LED
D61
GREEN,2.0 MA
R610 330
LNK_SFP+_2
ACTIVE LED
D60
YELLOW,2.0 MA
R655 330
ACT_SFP+_2
LNK and ACT derived From Arria 10
Designer : Zeev_L, Shimon_A, Ran_Z
RAD
data communications
Title
SFP+ - Port 2
Size B
Design Name : ETX-2I-10GX8.REV0.1I
Rev 0.0
Date: Thursday, June 04, 2020
Sheet 34 of 45



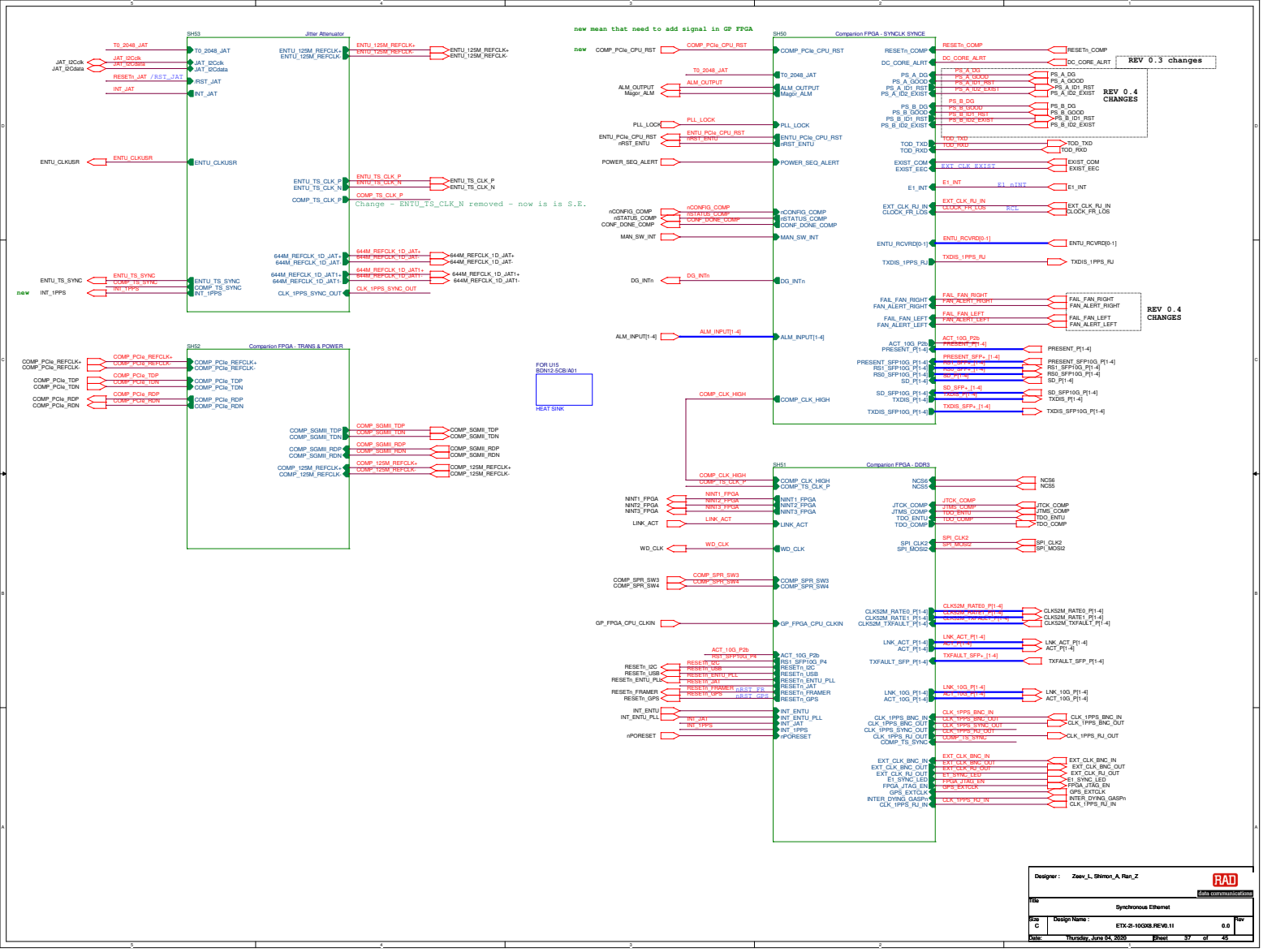
LNK and ACT derived From Arria 10

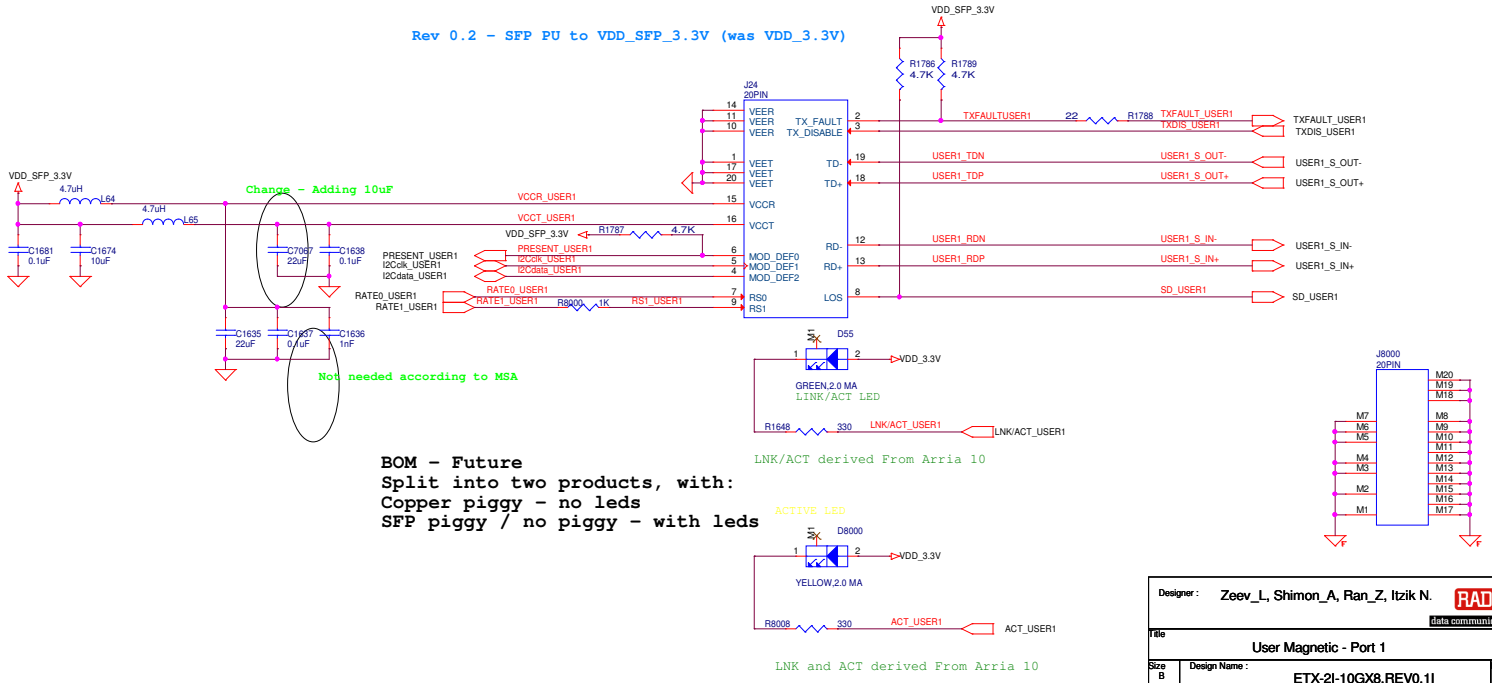
Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications	
Title	SFP+ - Port 3		
Size B	Design Name : ETX-2I-10GX8.REV0.1I		Rev 0.0
Date: Thursday, June 04, 2020	Sheet 35 of 45		



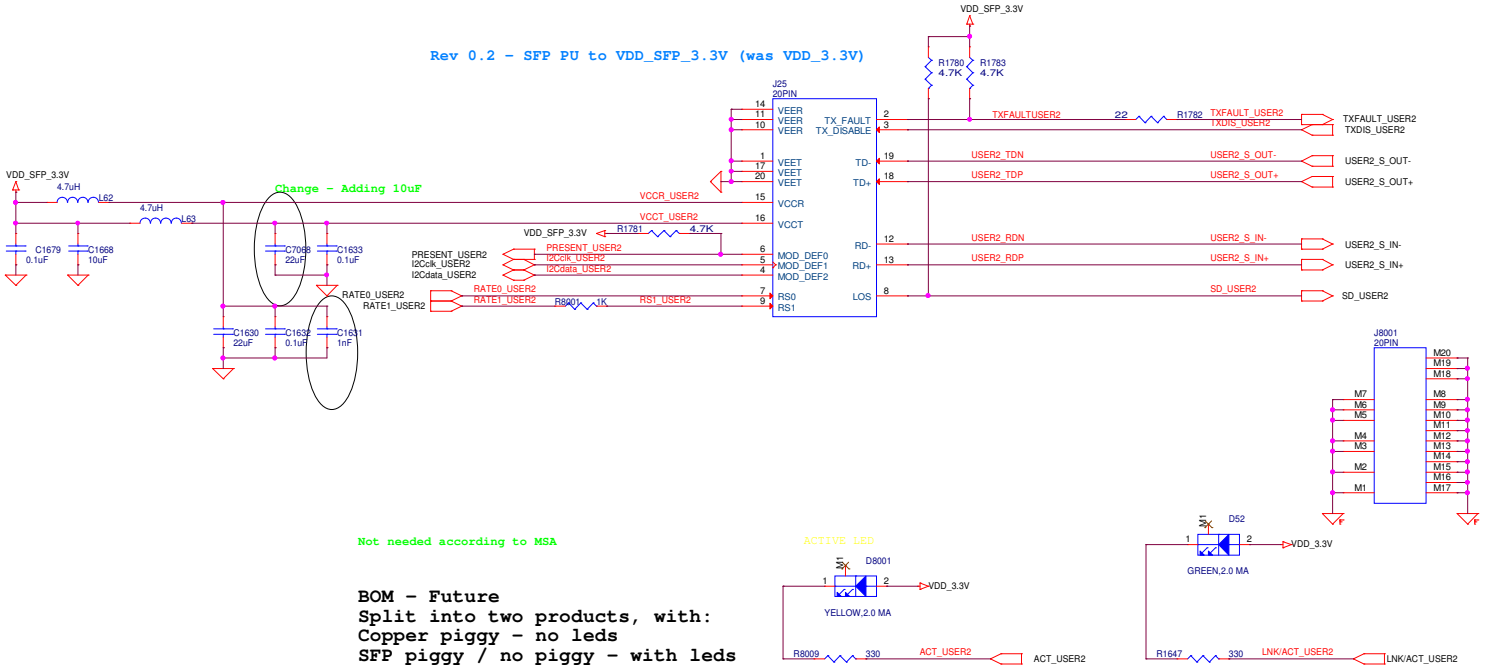
LNK and ACT derived From Arria 10

Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications	
Title	SFP+ - Port 4		
Size B	Design Name : ETX-2I-10GX8.REV0.1I		Rev 0.0
Date: Thursday, June 04, 2020	Sheet 36 of 45		


new mean that need to add signal in GP FPGA
SH53
Jitter Attenuator
SH52
Comparion FPGA - TRANS & POWER
SH50
Comparion FPGA - SYNCLK SYNCE
SH51
Comparion FPGA - DDR3
Change - ENTU_TS_CLK_N removed - now is S.E.
REV 0.3 changes
REV 0.4 CHANGES
REV 0.4 CHANGES
FOR U15
BDN12-5CB/A01
HEAT SINK
Designer : Zeev_L, Shimon_A, Ran_Z
rad data communications
Title
Synchronous Ethernet
Size C
Design Name : ETX-2I-10GX8.REV0.11
Rev 0.0
Date: Thursday, June 04, 2020
Sheet 37 of 45



Designer :	Zeev_L, Shimon_A, Ran_Z, Itzik N.		
Title	User Magnetic - Port 1		
Size B	Design Name : ETX-2I-10GX8.REV0.1I		Rev 0.0
Date: Thursday, June 04, 2020	Sheet 38 of 45		

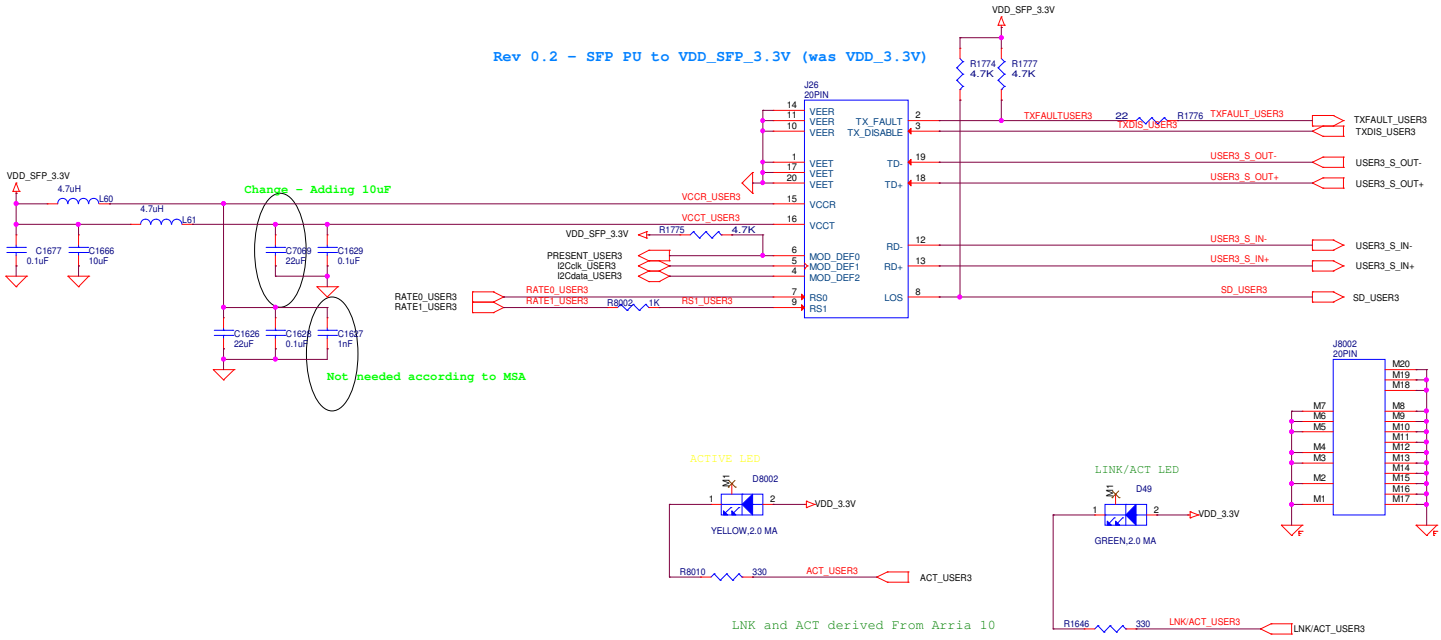


Not needed according to MSA

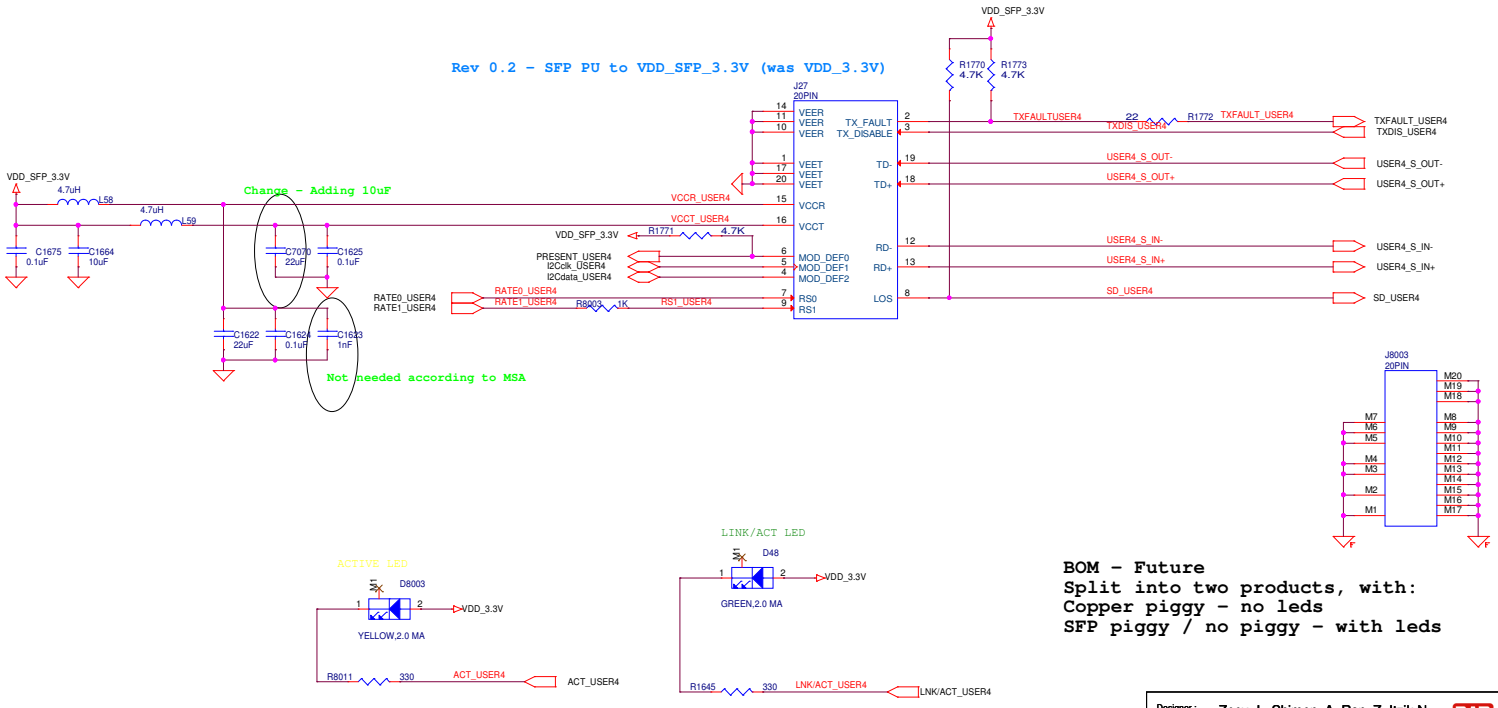
BOM – Future
Split into two products, with:
Copper piggy – no leds
SFP piggy / no piggy – with leds

LNK and ACT derived From Arria 10

Designer :	Zeev_L, Shimon_A, Ran_Z, Itzik N.	RAD data communications
Title	User Magnetic - Port 2	
Size B	Design Name : ETX-2I-10GX8.REV0.1I	Rev 0.0
Date: Thursday, June 04, 2020	Sheet 39 of 45	



Designer :	Zeev_L, Shimon_A, Ran_Z,Itzik N.	RAD data communications
Title	User Magnetic - Port 3	
Size B	Design Name : ETX-2I-10GX8.REV0.1I	Rev 0.0
Date: Thursday, June 04, 2020	Sheet 40 of 45	

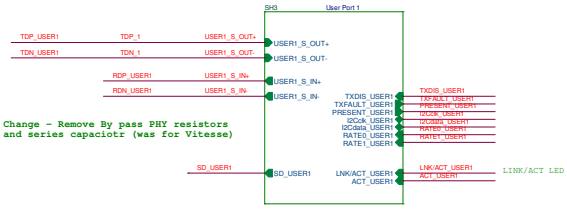


BOM - Future
Split into two products, with:
Copper piggy - no leds
SFP piggy / no piggy - with leds

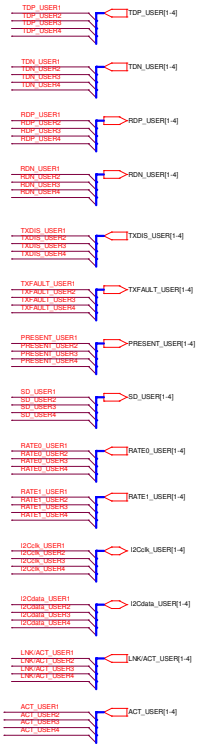
LNK and ACT derived From Arria 10

Designer :	Zeev_L, Shimon_A, Ran_Z, Itzik N.	RAD data communications	
Title	User Magnetic - Port 4		
Size B	Design Name : ETX-2I-10GX8.REV0.1I		Rev 0.0
Date:	Thursday, June 04, 2020	Sheet 41 of 45	

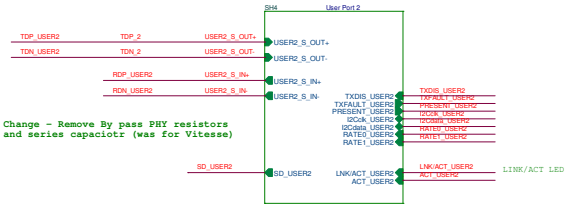
PORT 1 in the panel



Change - Remove By pass PHY resistors and series capaciotr (was for Vitesse)

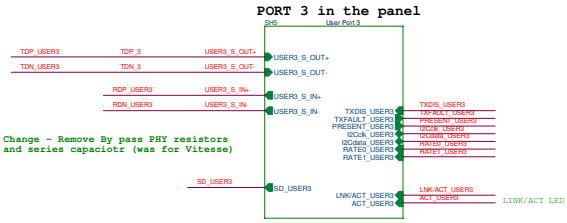


PORT 2 in the panel



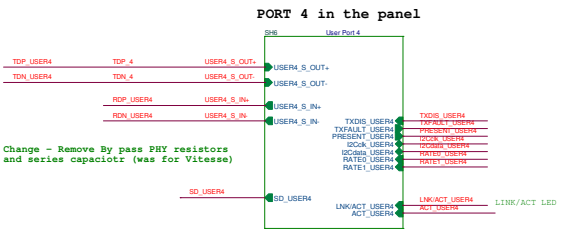
Change - Remove By pass PHY resistors and series capaciotr (was for Vitesse)

PORT 3 in the panel



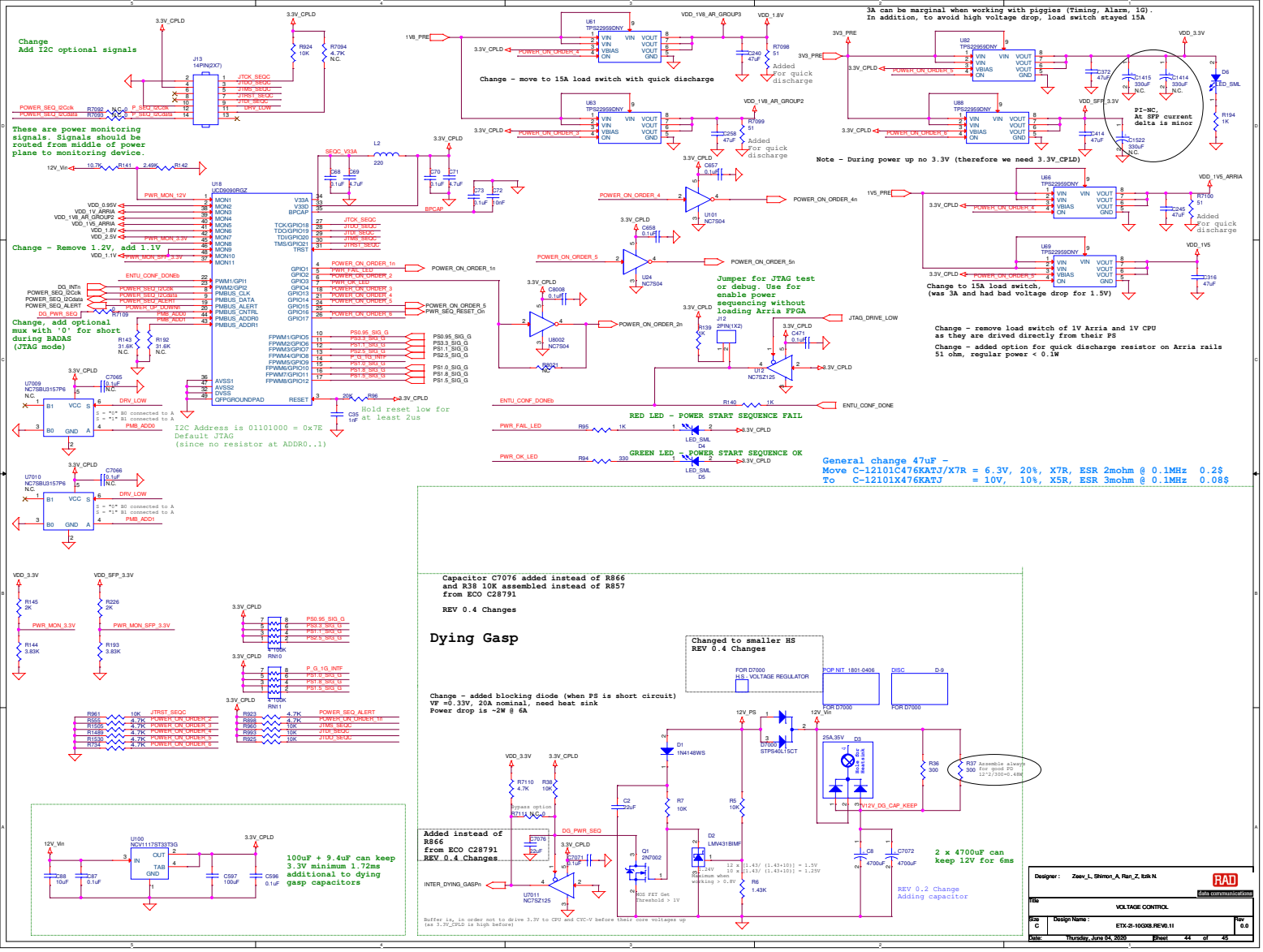
Change - Remove By pass PHY resistors and series capaciotr (was for Vitesse)

PORT 4 in the panel



Change - Remove By pass PHY resistors and series capaciotr (was for Vitesse)

Designer :	Zeev_L, Shimon_A, Ran_Z	RAD data communications	
Title	VSC8574 - User ports 1-4		
Size C	Design Name : ETX-2I-10GX8.REV0.1I		Rev 0.0
Date: Thursday, June 04, 2020	Sheet 45 of 45		

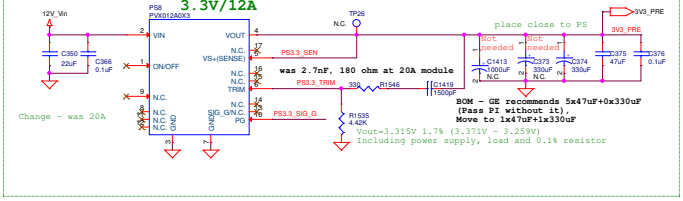


Designer :	Zeev_L, Shimon_A, Ran_Z, Itzik N.
Title	VOLTAGE CONTROL
Size	C
Design Name :	ETX-2I-10GX8.REV0.11
Rev	0.0
Date:	Thursday, June 04, 2020
Sheet	44 of 45

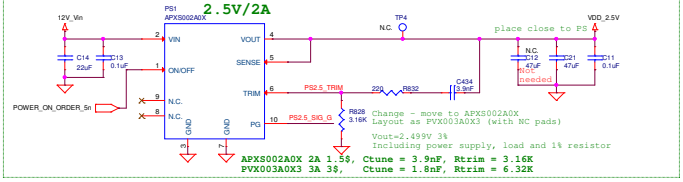
Main board max consumption ~6A
1G Piggy up to 1.8A (in case of 4x1.5W MiRIC)
Timing piggy 0.75A (up to 1.35A during OCXO warm up)
Alarm piggy 0.2A

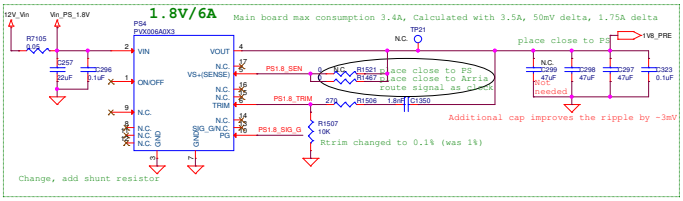
Main board max consumption 9A, Calculated with 9.5A, 50mV delta, 3A delta

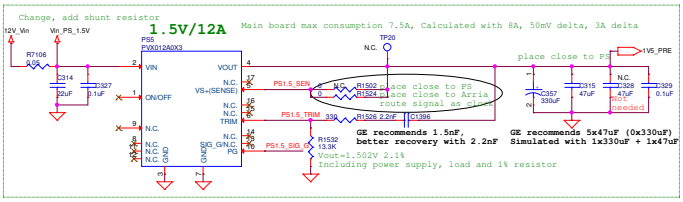
No Piggy - Simulation, Max 6A, 50mV delta, 2A delta
With Piggy - Simulation, Max 9A, 50mV delta, 3A delta



Main board max consumption 0.8A, Calculated with 1.2A, 50mV delta, 0.7A delta



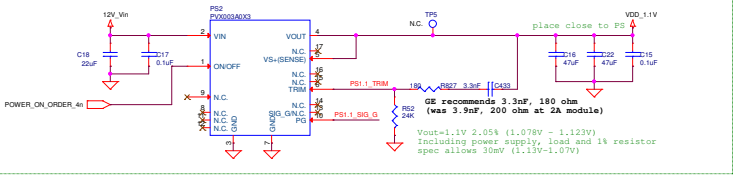




Change - Remove 1.2V (was for GP FPGA)

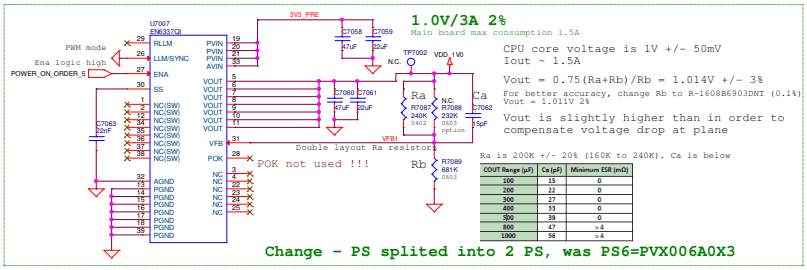
1.1V/3A

Main board max consumption ~2A, Calculated with 2.1A, 30mV delta, 1A delta



1.0V/3A 2%

Main board max consumption 1.5A

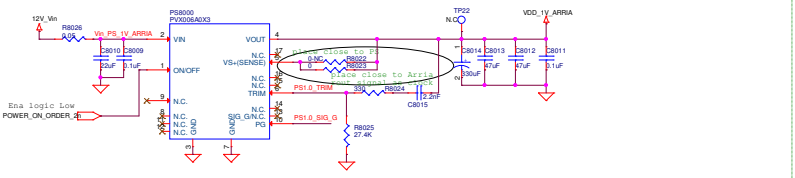


COUT Range (µF)	Ca (pF)	Minimum ESR (mΩ)
100	15	0
200	22	0
300	27	0
400	33	0
500	39	0
800	47	>4
1000	56	>4

Change - PS splited into 2 PS, was PS6=PVX006A0X3

1.0V/6A 2%

Main board (Arria) max consumption 3.9A

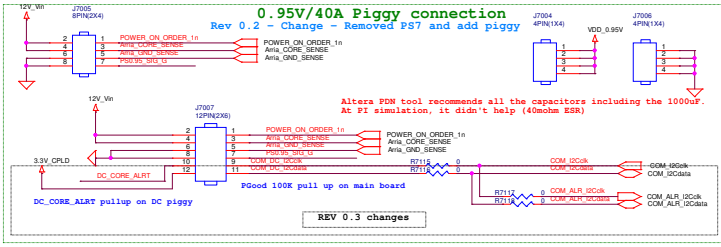


General change 47uF -
Move C-12101C476KATJ/X7R = 6.3V, 20%, X7R, ESR 2mohm @ 0.1MHz 0.2$
To C-12101X476KATJ = 10V, 10%, X5R, ESR 3mohm @ 0.1MHz 0.08$
GE example BOM is with worst Y5V capacitor

Optional change
C-TAJD337K010R/ESR 0.29$ 10V,10%,330MF,LOW ESR = 100 / 150 mohm @ 0.1MHz
C-TAJD337K006R 0.38$ 6V ,10%,330MF,LOW ESR = 50 mohm @ 0.1MHz
Due to better ESR stay with high price capacitor

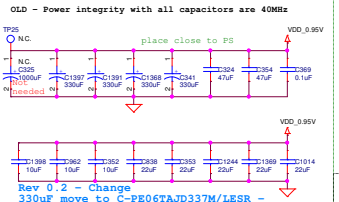
0.95V/40A Piggy connection

Rev 0.2 - Change - Removed PS7 and add piggy



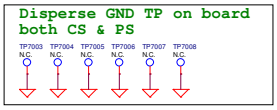
OLD - GE recommends 2x47uF + 4x330uF

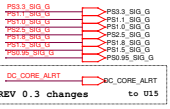
OLD - Power integrity with all capacitors are 40MHz



Rev 0.2 - Change
330uF move to C-PE06TAJD337M/LESR -
better ESR 15mohm, but 20%

Disperse GND TP on board both CS & PS





Designer : Zeev_L, Shimon_A, Ran_Z, Liora_S(rev0.3), Itzik N.

RAD data communications

Title: VOLTAGE CONVERTERS

Size: C | Design Name : ETX-2I-10GX8.REV0.1I | Rev: 0.0

Date: Thursday, June 04, 2020 | Sheet 45 of 45