P, I, D 계수는 제어비트에 따라 결정되며, 상세사항은 아래의 표와 같다.

Table 3.3.3.6 PCV-21 밸브 제어를 위한 PID 제어계수

	발생 조건	계수값	
1	1. CONFIGURATION=1, 2, 3, 4, 10 2. ENGINE TEST SET-UP BIT=1 3. TC1_SETUP_MEM_AETF2_EGD BIT=1	P	10
		I	3
		D	0
2	1. CONFIGURATION=5 2. ENGINE TEST SET-UP BIT=1 3. TC1_SETUP_MEM_AETF2_EGD BIT=1	P	10
		I	3
		D	0
3	1. CONFIGURATION=6, 7, 8, 9, 11, 12 2. ENGINE TEST SET-UP BIT=1 3. TC1_SETUP_MEM_AETF2_EGD BIT=1	P	15
		I	5
		D	0
4	1. FCV21 FAST GAIN DIFF PRESSURE MEMORY BIT=0 2. FCV21 INTERMEDIATE GAIN DIFF PRESSURE MEM BIT=1 FCV21 INTERRUPT PB BIT=0	P	14
		I	14
		D	6
5	1. FCV21 FAST GAIN DIFF PRESSURE MEMORY BIT=1 2. FCV21 INTERMEDIATE GAIN DIFF PRESSURE MEM BIT=1 FCV21 INTERRUPT PB BIT=0	P	20
		I	14
		D	6
6	1. FCV21 FAST GAIN DIFF PRESSURE MEMORY BIT=0 2. FCV21 INTERMEDIATE GAIN DIFF PRESSURE MEM BIT=0 FCV21 INTERRUPT PB BIT=0	P	0.7
		I	8
		D	0
7	1. CONFIGURATION=1, 2, 3, 4, 10 2. ENGINE TEST SET-UP BIT=1 3. TC2_SETUP_MEM_AETF2_EGD BIT=1 4. FCV21 INTERRUPT PB BIT=1	P	10
		I	3
		D	0
8	1. CONFIGURATION=5 2. ENGINE TEST SET-UP BIT=1 3. TC2_SETUP_MEM_AETF2_EGD BIT=1 4. FCV21 INTERRUPT PB BIT=1	P	10
		I	3
		D	0
9	1. CONFIGURATION=6, 7, 8, 9, 11, 12 2. ENGINE TEST SET-UP BIT=1 3. TC2_SETUP_MEM_AETF2_EGD BIT=1 4. FCV21 INTERRUPT PB BIT=1	P	15
		I	5
		D	0

PCV-22 밸브에도 다음과 같이 PID 제어로직을 추가하였다. PID 제어로직은 앞서 검증한