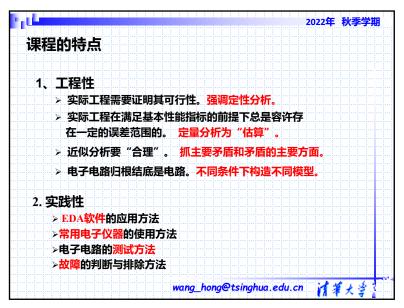
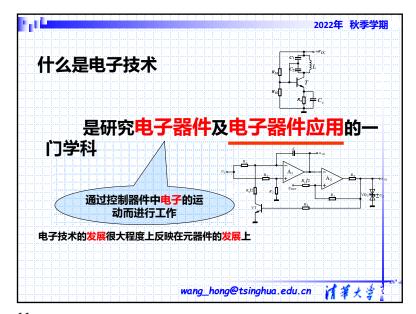




2022年 秋季学期 课程目的: 掌握基本概念、基本设计和分析的方法、以及基 本实验技能; 具有能够继续深入学习和接受电子技术新发展 的能力,以及将所学知识用于本专业的能力。 学习方法: 入门阶段以听课为线索, 强调实践环节; 建立工 程的观念、系统的观念、科学进步的观念和实践的观念。 注意定性分析和近似分析的重要性 学会辩证、全面地分析电子电路中的问题 —— 打破唯一性 > 根据需求,最适用的电路才是最好的电路。 > 要研究利弊关系,通常"有一利必有一弊"。 注意电路中常用定理在电子电路中的应用, 电子电路归根结底是电路。 wang\_hong@tsinghua.edu.cn 指著大学

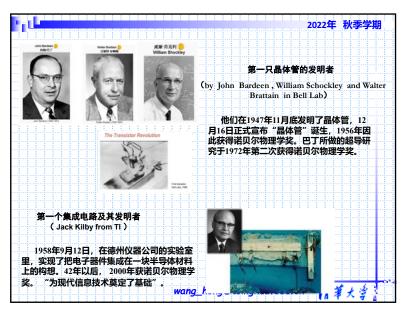


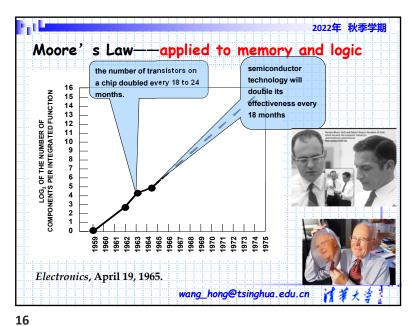


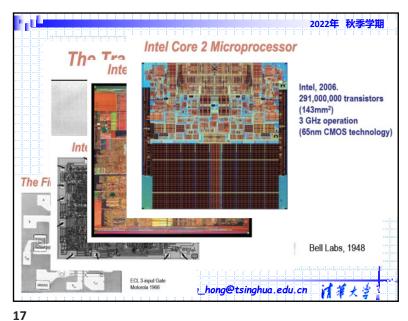


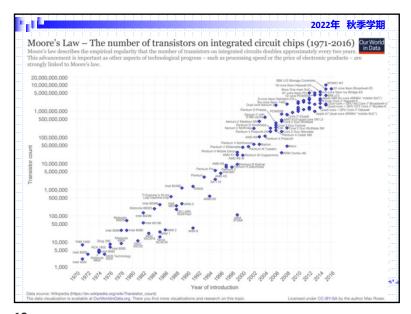


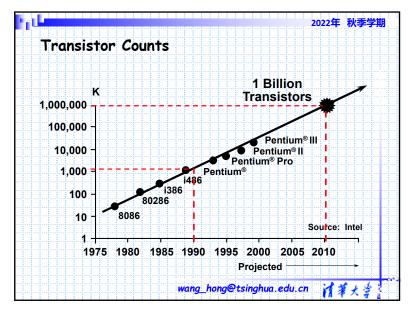




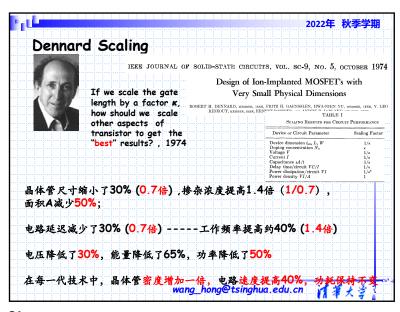


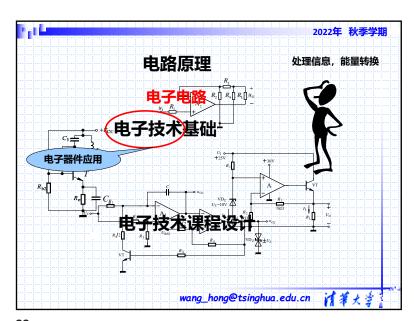






ri H		2022年	秋季学期
	emiconductor nanufacturing processes	State of the Art	
0		As of September 2018, mass production of 7 nm devices has begun. The first mainstrean mobile processor intended for mass market use, the Apple A12 Bionic, was released at til September 2018 event.	
6		Although Huawei announced its own 7 nm processor before the Apple A12 Bionic, the K 980 on August 31, 2018, the Apple A12 Bionic was released for public, mass market use consumers before the Kirin 980. Both chips are manufactured by TSMC. AMD is currently working on their "Rome" workstation processors, which are based on the 7 nanometer 1	to ly
	D PER S	and feature up to 64 cores.	
	μm – 1971 μm – 1974	▶ 5nm	
	µm - 1977	The 5 nm node was once assumed by some experts to be the end of	
	5 µm - 1982	Transistors smaller than 7 nm will experience quantum tunnelling through the gate	
. 1	μm - 1985	layer. Due to the costs involved in development, 5 nm is predicted to take longer to market than the two years estimated by Moore's law. Beyond 7 nm, it was initially	
800	0 nm - 1989	that major technological advances would have to be made to produce chips at this	
600	0 nm - 1994	scale. In particular, it is believed that 5 nm may usher in the successor to the	
350	0 nm - 1995	FinFET, such as a gate-all-around Architecture.	
250	0 nm - 1997	Although Intel has not yet revealed any specific plans to manufacturers or	
180	0 nm - 1999	2009 roadmap projected an end-user release by approximately 2020. In early	
130	0 nm - 2001	Samsung announced production of a 4 nm node by 2020 as part of its revised	
91	0 nm - 2004	On January 26th 2018, TSMC announced production of a 5 nm node by 2020 on its fab 18. In October 2018, TSMC disclosed plans to start risk production of 5 nm	
68	5 nm - 2006	April2019.	
4	5 nm - 2008	S Plane S	nFET around
3:	2 nm - 2010	+ 3.5nm	-3 -3
2	2 nm - 2012	3.5 nm is a name for the first node beyond 5 nm.ln 2018, IMEC and	
14	4 nm - 2014	Cadence had taped out 3 nm test chips. Also, Samsung announced that	
-10	0 nm - 2017	they plan to use Gate-All-Around technology to produce 3 nm FETs in	Supplied Williams
	7 nm - 2018		lateral by gots
	5 nm - ~2020	Elpinssiviben	AICI from a
		wang_hong@tsinghua.edu.cn 📝 🛊	5 4 25 1





2022年 秋季学期 Electronic Design 电子技术的发展 Automation 贝尔实验室制成第一只晶体管 ・47年 ・58年 集成电路 (4-12-100-1000) ・69年 大规模集成电路 (10万) ・75年 超大规模集成电路(15万) VLSI ULSI GLSI SSI MSI LSI 第一片集成电路只有4个晶体管,而97年一片集成电路上 有40亿个晶体管。预测集成度按10倍/6年的速度---wang\_hong@tsinghua.edu.cn

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