Wave Shapping

Wave Shapping:

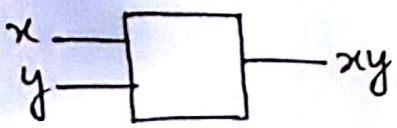
A signal is called a wave. Every wave has a certain shape when it is represented in a graph / shape. This is called wave shapping. There are two types of wave shapping. That is -

a) Linear Wave Shapping:

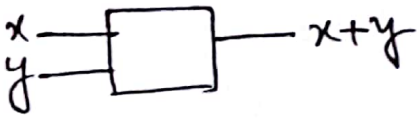
It is the process by which a non sinusoidal signal is altered by transmission through a linear workplace. Such as RC. RL and RTC etc.

Characteristics:

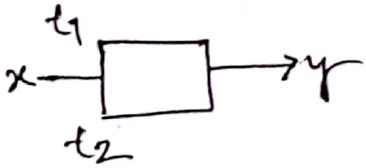
1. It can hold the waveform to a particular d.c. level.
2. It also generate one wave form to another.
3. It limits the voltage level of the waveform of some presenting value.
4. It cuts-offs the positive and negative portion of the output waveform.
5. Homogenity i.e.



6. Additive i.e.



7. Shift



Filter:

A filter is a circuit that can remove unwanted points of a signal at its input.

Characteristics:

* A capacitor has the property to allow AC and to block DC.
* An inductor has the property to allow DC but block AC.

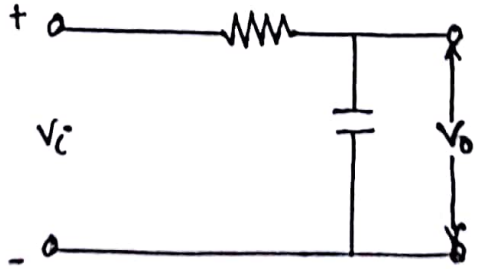
Types of filter:

There are four types of filter i.e.

1. Low pass filter:

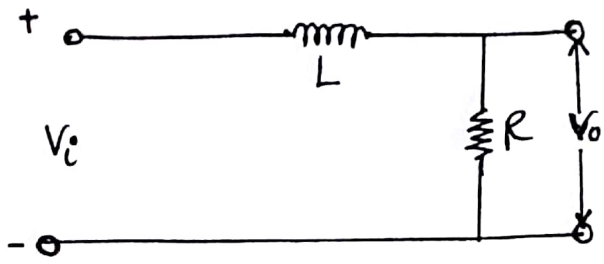
A filter circuit which allows a set of frequencies that are below a specified value can be termed as a low pass filter.

a) The RC filter: As the capacitor is placed in shunt. The AC allows it grounded. This by passes all the high frequency components while allow's DC at the output.



Low pass RC circuit

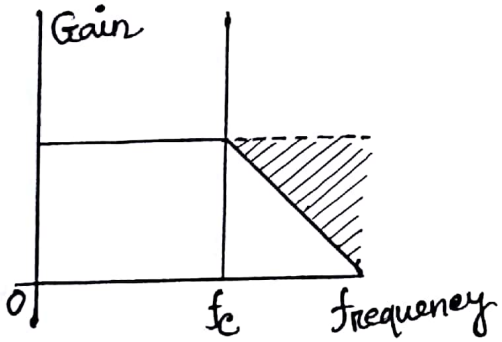
b) The RL filter: As the inductor is placed in series, the DC is allows to the output. The inductor blocks AC which is not allowed at the output.



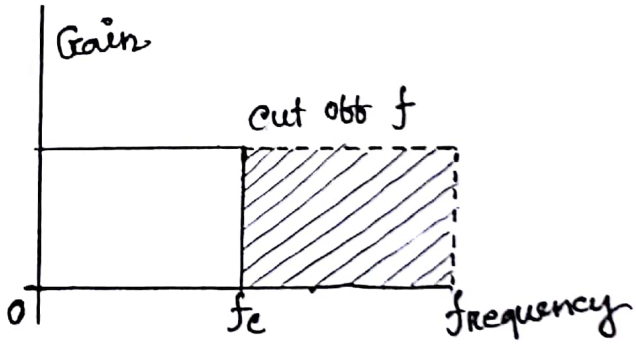
Low pass RL circuit

Symbol of low pass filter:

Frequency Response:

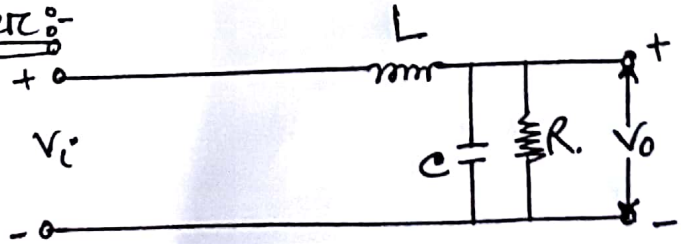


Frequency response for LPF



Ideal Frequency response for LPF

The RLC Filter:-

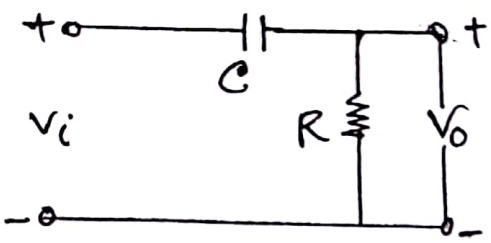


RLC Low pass filter circuit.

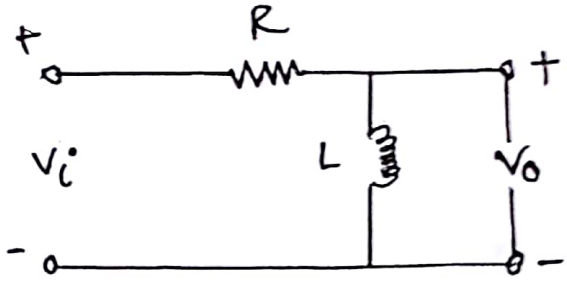
This required a, inductor, a capacitor and a resistor.

High pass filter:

It is a filter circuit which allow's a set of frequencies that are above a specified value can be termed as a high pass filter.



High pass RC circuit

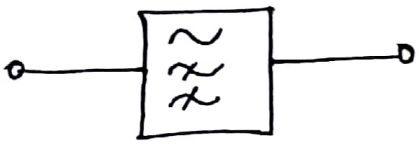


High pass RL circuit

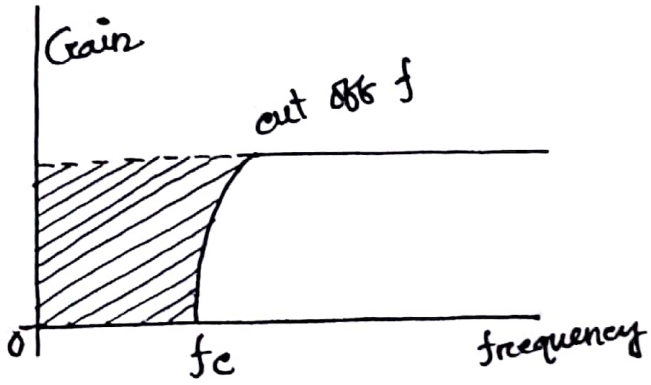
The RC filter: As the capacitor is placed in series, it blocks the DC components and allow AC component as outp

The RL filter: As the inductor is placed in shunt the DC is allowed to be grounded. The remaining AC components appear's at the output.

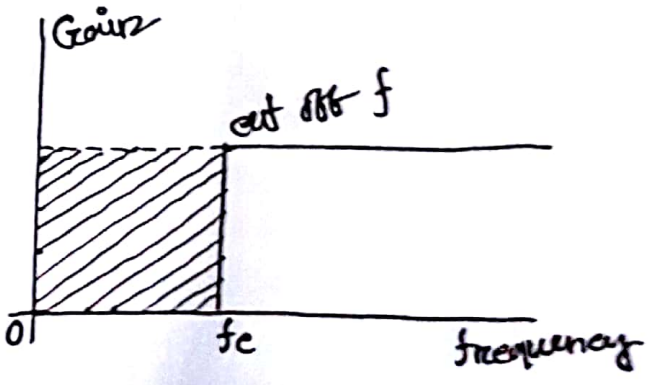
Symbol of HPF:



Frequency Response:

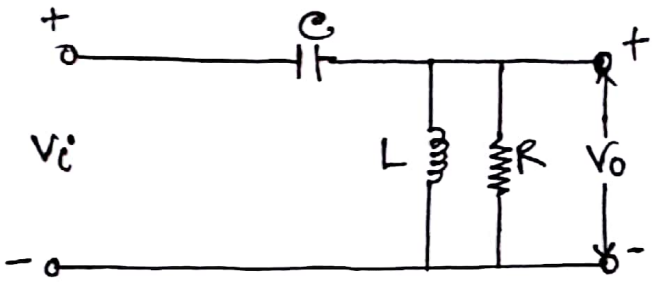


Frequency response of HPF



Ideal frequency response HPF

The RCL Filter:



High pass RLC circuit

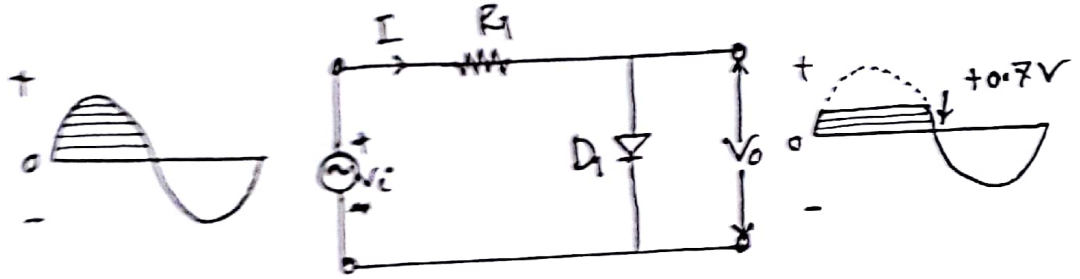
There are a capacitor connected with a inductor and a resistors in parallel.

Clipper & Clamper

☆ Clipper:

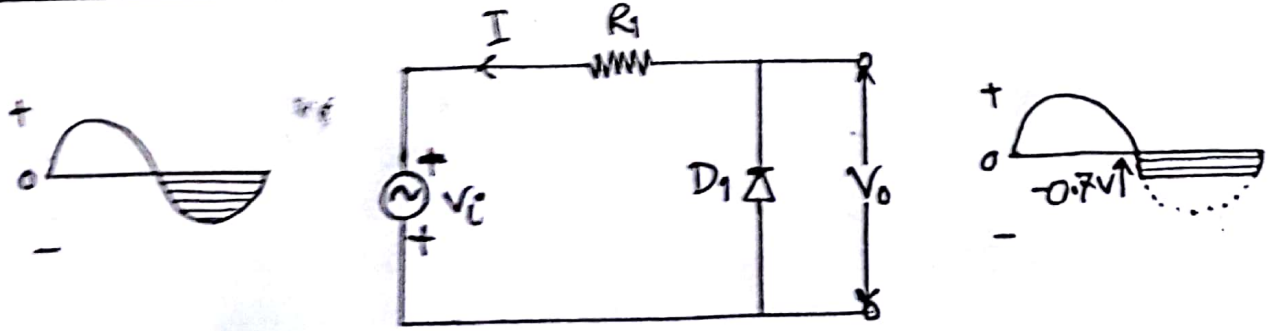
It is an electric device that prevent the output of a circuit from exceeding a pre-determinated voltage level without distoring the remaining part of the applied wave form.

Positive diode clipping circuit:



In this diode clipping circuit, the diode is formed biased during the positive half cycle. It must have the input voltage magnitude greater from +0.7 V, when this happens the circuit cut off the magnitude as the figure shown.

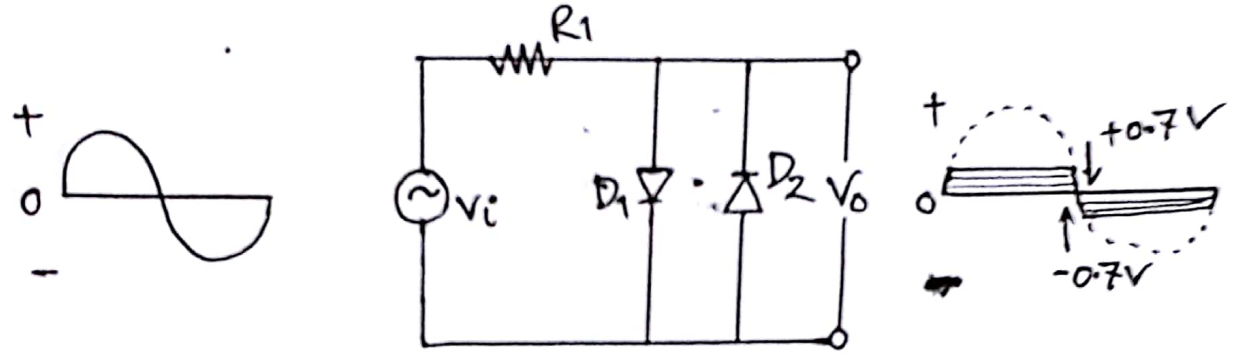
Negative Diode clipping:



Here the reverse is true. The diode is forward

biased during the negative half cycle of the sinusoidal waveform and limits or clips it to -0.7V while allowing the positive half cycle to pass unaltered when reverse biased.

Clipping of Both half Cycle:



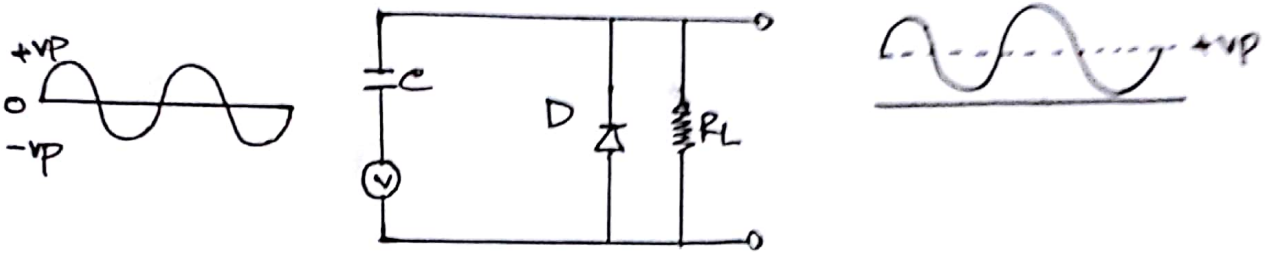
When the voltage of the positive half cycle reaches +4.7V diode D_1 conducts and limits the waveform of +4.7V Dide D_2 does not conduct until the voltage reaches -6.7V. Therefore, all positive voltage above +4.7V and negative voltage below the advantage of biased diode clipping circuits.

Clampers:

It is a ~~negative~~ networks that shifts a waveform to a different level without change the appearance of the applied signal.

Positive Clamper:

- Shifts its input waveform in a positive direction
- Lies above a dc reference voltage



~~Negative Clamper for~~ Positive half cycle:

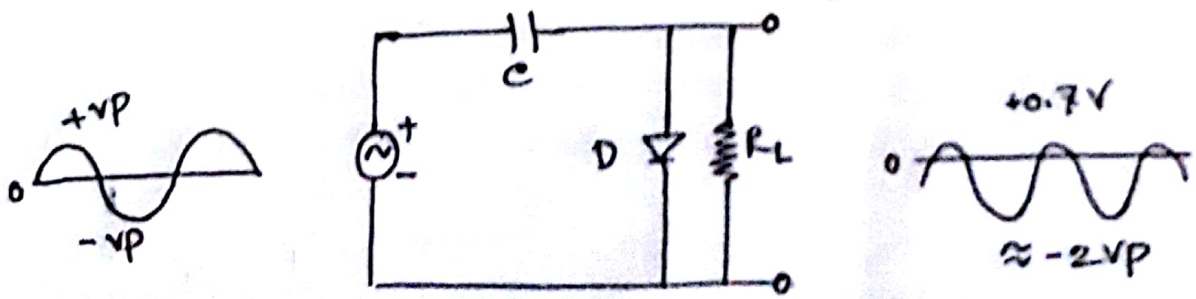
Conductor acts as short circuit and acts as shunt circuit and output V=0. Capacitor is charged to peak value and behave like battery.

Negative half cycle:

- Does not conduct and act as open circuits
- Output voltage

Negative Clamper:

- Shifts it's input waveform in a negative direction
- Lies below a DC reference voltage.



- **Positive half cycle:**
  - Diode conducts and acts as short circuit.
  - Capacitor is charged to peak value and behave like battery output $v = 0$.
- **Negative half cycle:**
  - Diode is open and output can be borrowed by applying KVL.

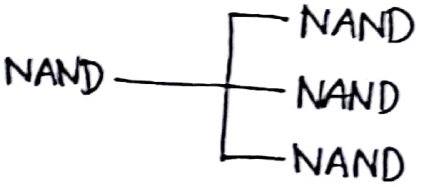
Digital Logic Family:

A digital logic family is a logic family of monolithic digital integrated circuit devices is a group of electronic logic gate constructed using several different design, usually with compatible logic levels and power supply characteristics.

Fan in: It is the number of input's of a gate that it can handle without improving it's normal operation.

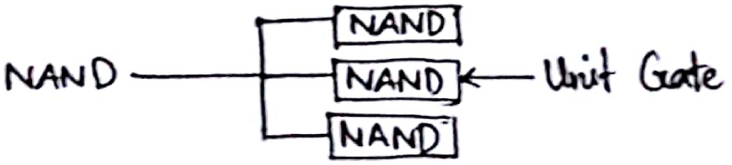
Fan in - 1

Fan out: The maximum number of digital input's that the output of single logic gate can faced and the gate must be in same logic family.



$$\text{Fan out} = \frac{I_{OL}}{I_{IL}} \text{ or } = \frac{I_{OH}}{I_{IH}}$$

Unit gate: Each of the connected logic gate will be considered an unit gate.



High Stage:

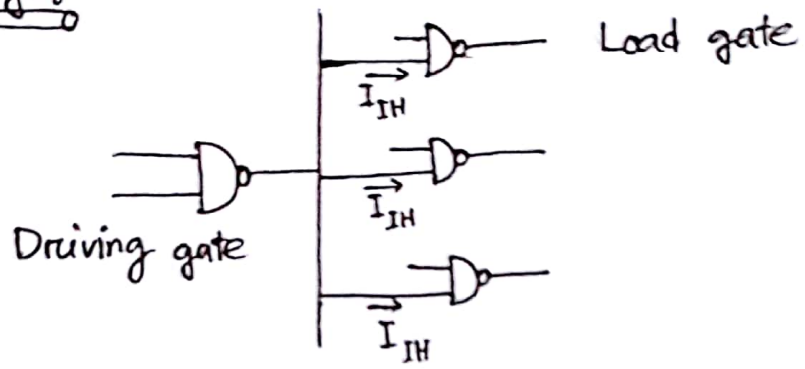


Figure: Current sourcing high stage

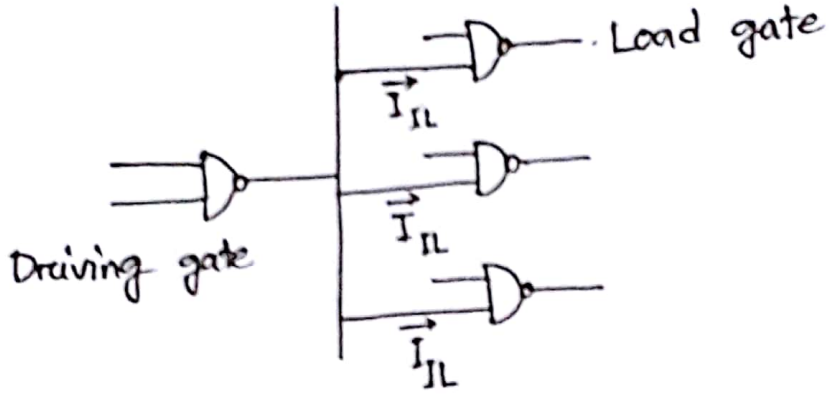


Figure: Current sourcing low stage

Propagation:

Time taken bore the output of a gate delay to change abter the input is applied.

$T_{PLH} \rightarrow 0$ to 1

$T_{PHL} \rightarrow 1$ to 0

Noise Margin:

A ability of the gate to tolerate bunctuations of the voltage levels.

Logic Family

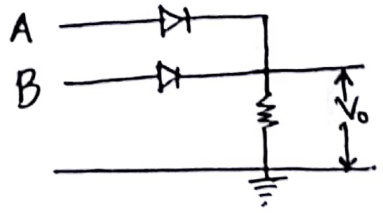
- Bipolar
  - Satured
  - Non-satured
- Unipolar
  - PMOS
  - NMOS
  - CMOS

Satured:

1. DL = Diode Logic
2. DTL = Diode Transistor Logic
3. TTL = Transistor Transistor Logic
4. IIL = Integrated Injection Logic
5. RTL = Resistor Transistor Logic

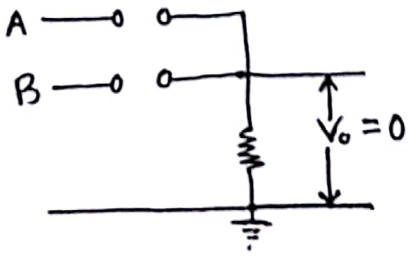
1. DL = Diode Logic :

OR :

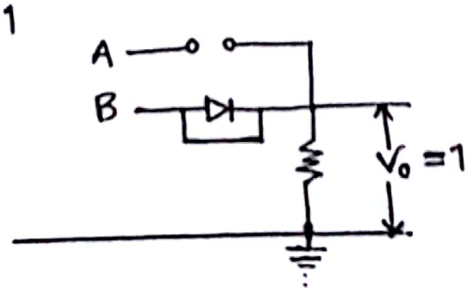


A	B	V_o
0	0	0
0	1	1
1	0	1
1	1	1

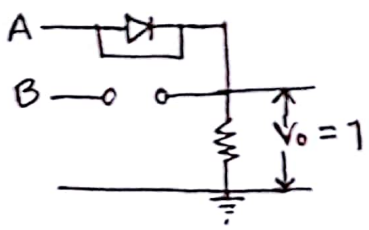
A=0, B=0



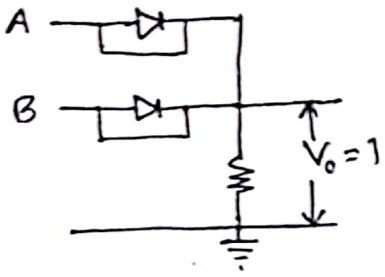
A=0, B=1



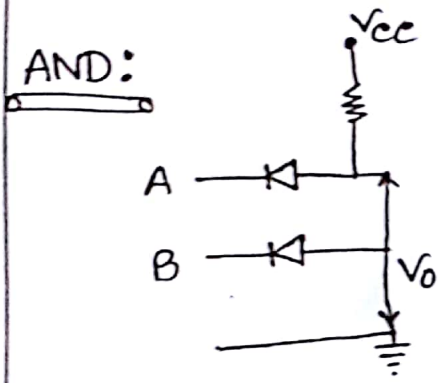
A=1, B=0



A=1, B=1

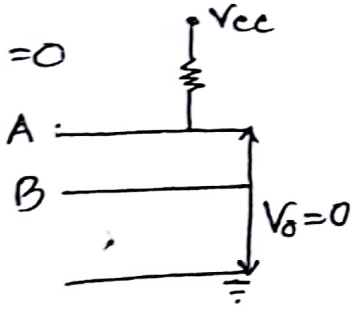


AND:

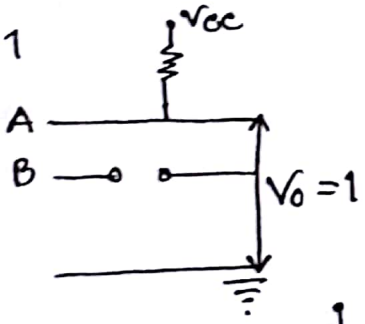


A	B	V_o
0	0	0
0	1	0
1	0	0
1	1	1

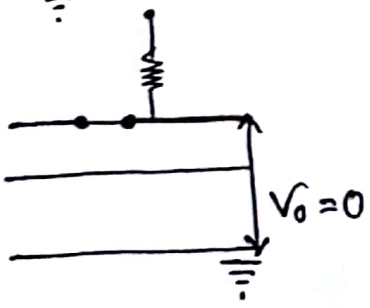
A=0, B=0



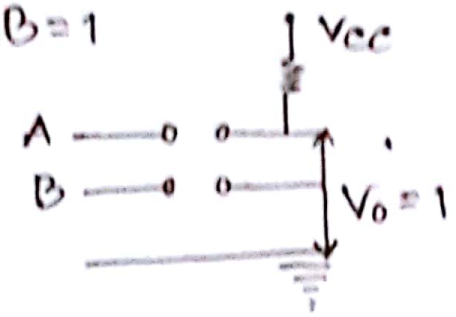
A=0, B=1



A=1, B=0

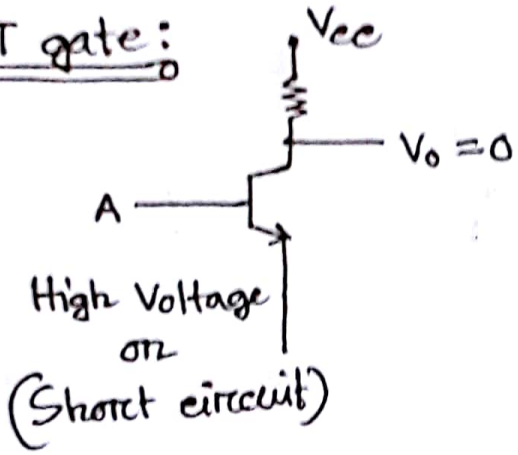


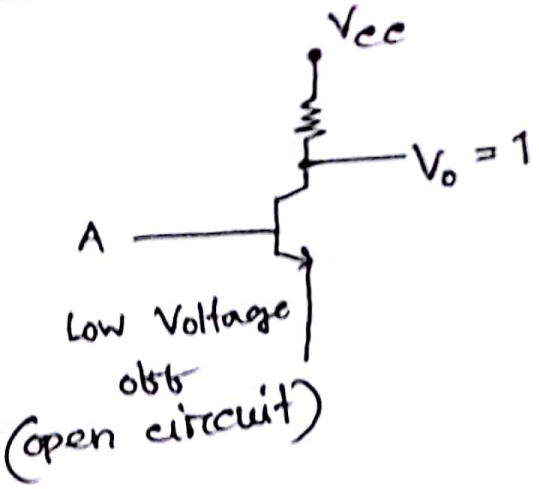
A=1, B=1



RTL: Resistance Transistor Logic:

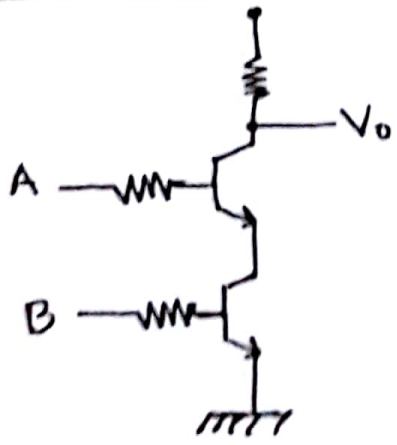
NOT gate:





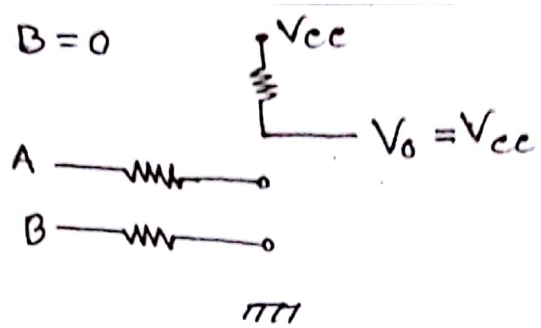
A	Vo
0	1
1	0

NAND Gate:

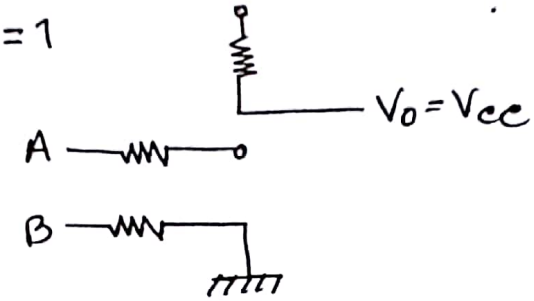


A	B	Vo
0	0	1
0	1	1
1	0	1
1	1	0

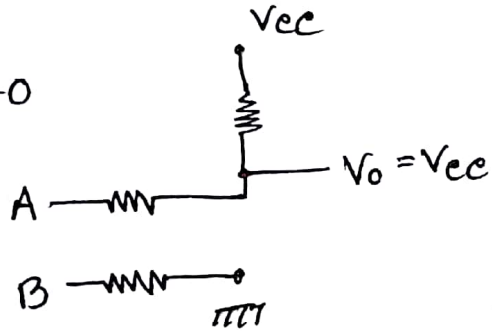
A=0, B=0



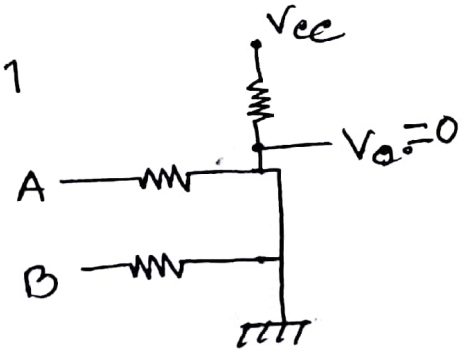
A=0, B=1



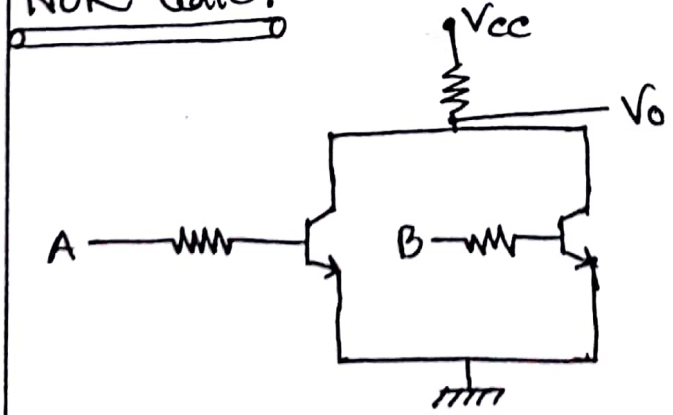
A=1, B=0



A=1, B=1

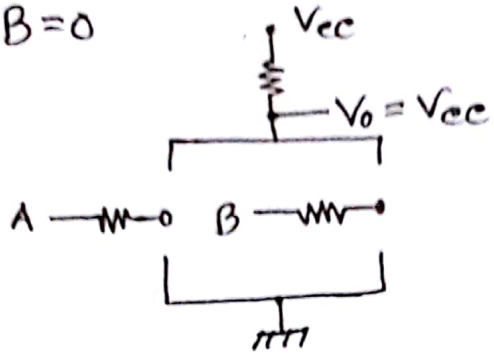


NOR Gate:

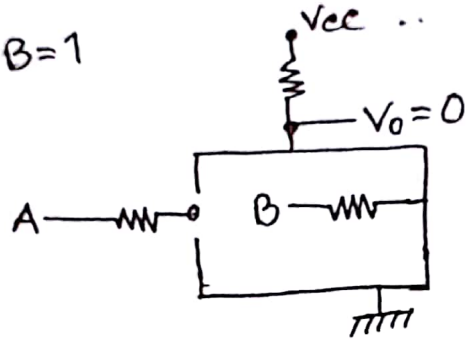


A	B	V_0
0	0	1
0	1	0
1	0	0
1	1	0

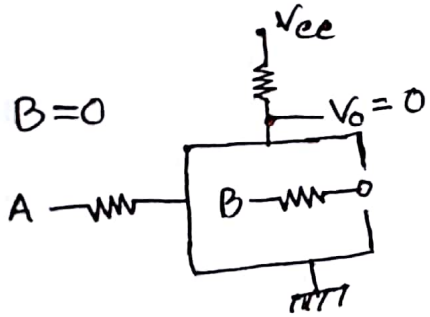
A=0, B=0



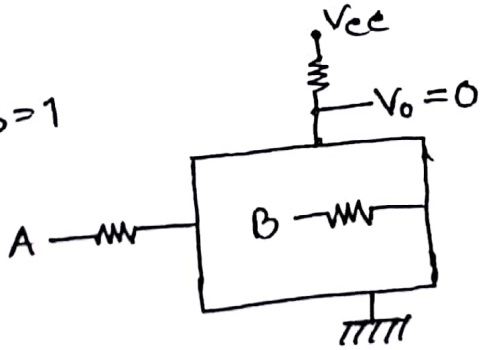
A=0, B=1



A=1, B=0



A=1, B=1



MOS Logic Family

MOS Logic Family:

The MOS inverter is the basic circuit exhibits all of the essential features of MOS logic. Extension of MOS inverter concepts to NOR and NAND Gate is very simple. Digital MOS circuits can be classified into two categories-

a) Static Circuits: It is required no clock or other periodic signal for operation. Clocks are required for for static circuit in sequential Logic.

b) Dynamic Circuits: It is required periodic clock signals, synchronized with data signals, for proper operation even in combinational logic.

Characteristics of MOS:

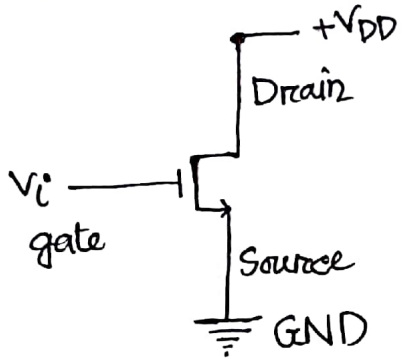
1. Packaging Density: very high, VLSI usable.
2. Operation speed/propagation delay: high, 50 nsec.
3. Process complexity: no process complexity.
4. Power dissiption: very low power dissiption.
5. Noise Mergin: Maximum noise aviabilaty normal 1V.
6. Fan out: Infinity fan out.

Switching property of NMOS:

To get output signal minimum input may be greater than V_{th}. It may be positive voltage. The condition is -

$V_i > V_{th} \rightarrow$ NMOS = on

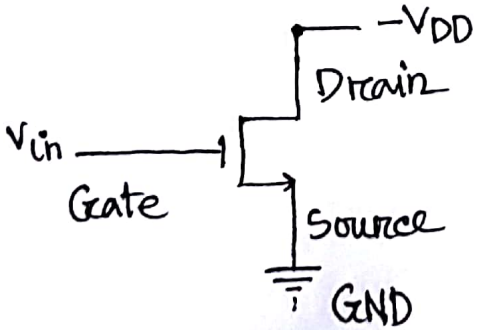
Otherwise → off



when switch on transistor behave as 1KΩ. and when switch off then it behave $10^{12}\Omega$.

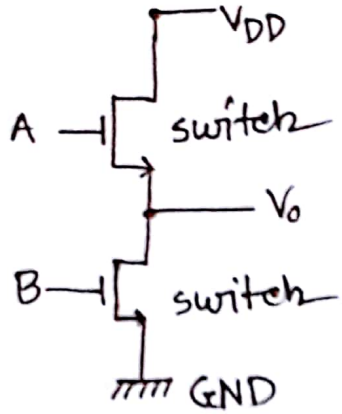
Switching property of PMOS:

When V_{in} be negative voltage then the switch will be on and behave as 1KΩ. The figure of PMOS switching property-

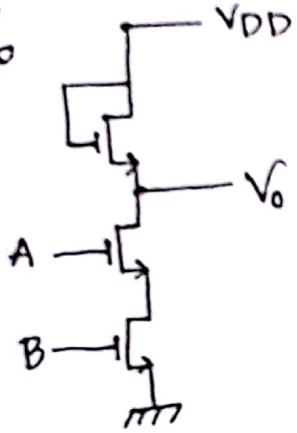


CMOS Inverter:

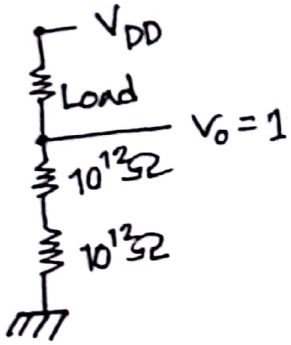
The CMOS inverter consists of two transistor types which are processed and connected, as



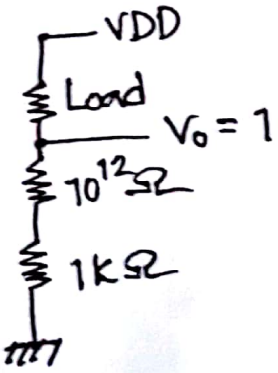
NAND Gate:



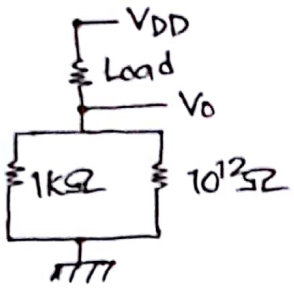
A=0, B=0



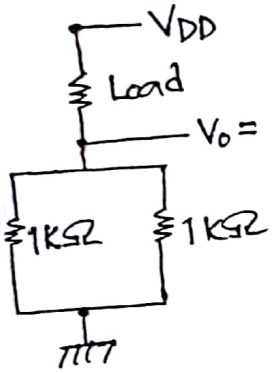
A=0. B=1



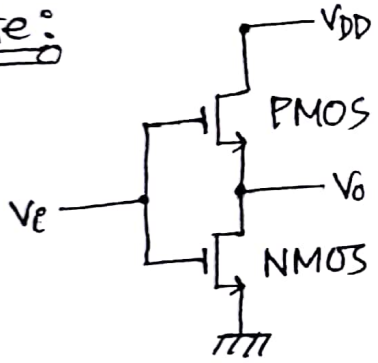
A = 1, B = 0



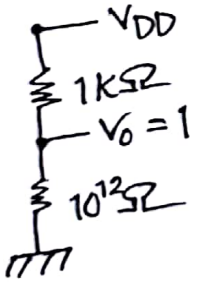
A = 1, B = 1



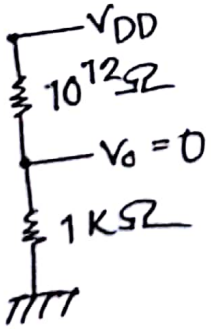
NOT Gate:



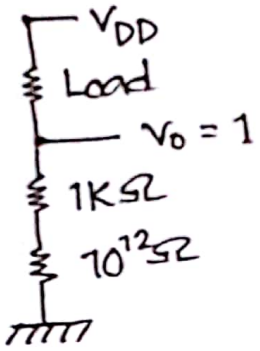
$V_i = 0$



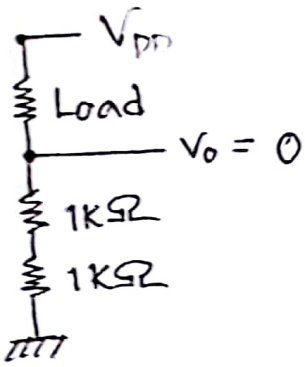
$V_i = 1$



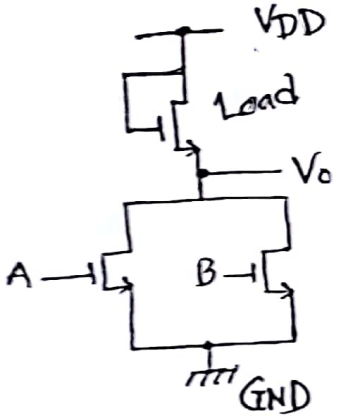
A=1, B=0



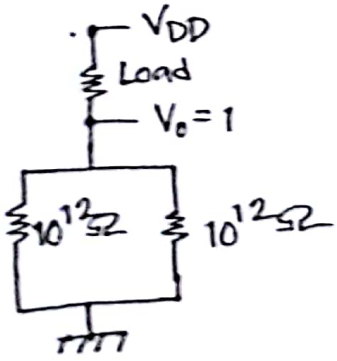
A=1, B=1



NOR Gate:



A=0, B=0



A=0, B=1