CE 100 Lab Report 8

Breadboard Construction

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Lab Section: Tuesday, Thursday 2:00pm – 4:00pm

Date: March 14th 2016

Description:

The purpose of this lab was to get us to understand and familiarize ourselves with constructing digital systems using breadboards, chips, and wires. For this lab, the systems we created were building and measuring the propagation delay of an inverter, building an edge-triggered flip-flop, and discover the depth design of a FPGA.

Some background into the logic designs I built, **Figure 1**. The first design was, again, to measure the propagation delay of the CMOS inverter. What that means is that the delay is determined by the time it takes to charge and discharge the capacitances present in a logic circuit. In my logic case network, I have put 9 inverters in series together and take the measurement. The reason being for putting so many inverters together is for accuracy measures, the delay will be the time for several transitions and divided by the number of transitions. As well, the inverters may not be the same, so we would want to take a weighted average.

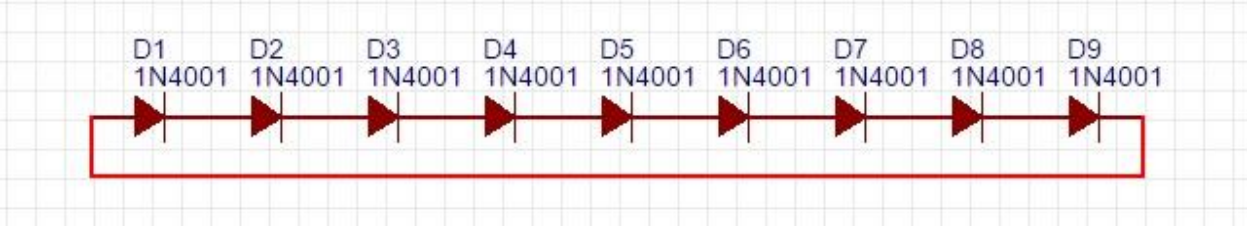


Figure 1

9 inverter Ring Oscillator for Part I of Lab 8

Furthermore, in order to build an edge-triggered flip-flop, I had to understand the logic design behind their sequential circuits. Essentially, I wanted to deal with synchronous sequential logic, which uses states that change in lock step across all storage elements using a clock signal. Given the option to construct an edge triggered flip flop using synchronous sequential logic, I chose to create a positive edge-triggered flip-flop using six NAND gates. The way the circuit is implemented is displayed on **Figure 2**.

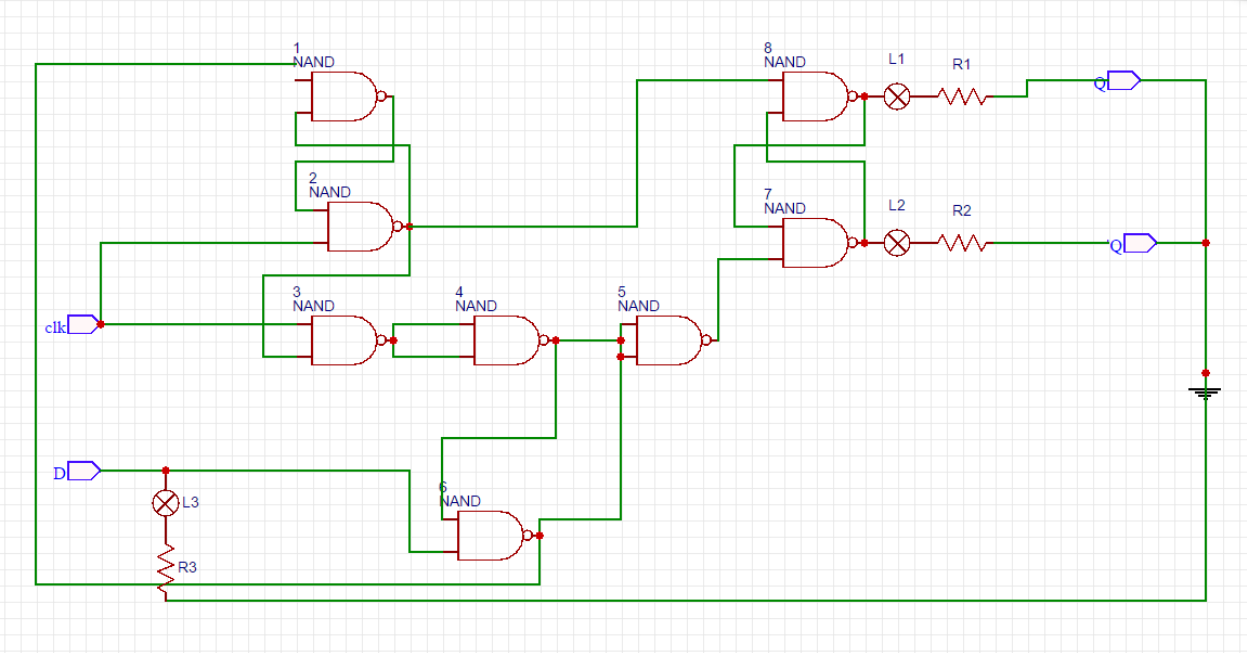


Figure 2

Positive Edge Triggered Schematic for Part II of Lab 8

Part I: Measuring Propagation Delay

In order to measure my ring oscillator, I chose to parts that are compatible with my ring oscillator. One which was an output of Figure 1 and ground, thus allowing me to get a waveform of **Figure 3**. From here, we can see figure out the measurements for Part 1. We take the period of the waveform, which is .1µs and calculate frequency using the formula f= 1/period * 1/ (9 inverters) = 9 * 10^7 Hz. According to the specified datasheet, they had 9 Nano seconds, which if we take the frequency of that time period; get 1/ (9e-9) = 11 * 10^7 Hz which was near 9 * 10^7 Hz. There might has been some human error that calculates with the discrepancy; such as the wires.

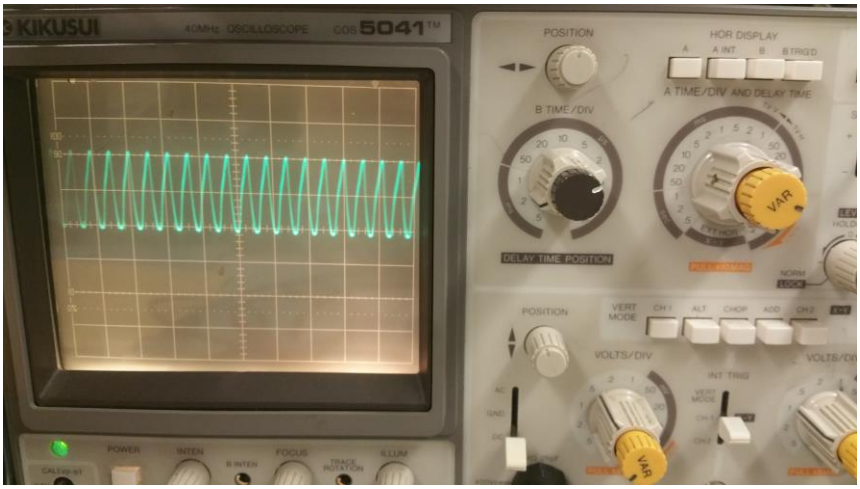


Figure 3

Waveform of **Figure 1**

Switching Characteristics

• **HD74LS04**

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	min.	typ.	max.	Unit	Condition
Propagation delay time	t_{PLH}	—	9	15	ns	C_L = 15 pF, R_L = 2 kΩ
	t_{PHL}	—	10	15	ns	

Figure 4

Data Sheet of the HD74LS04 inverters I used

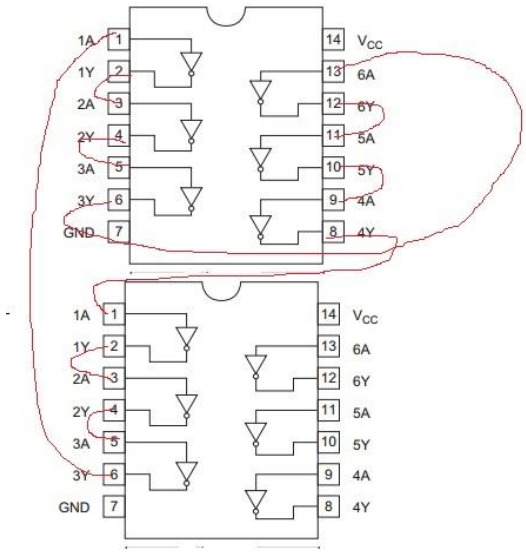


Figure 5

Wiring diagram of Part I of Lab 8

Part II: Edge Triggered Flip-Flop

Here I constructed a positive edge triggered flip-flop out of HD74LS00 parts. I used the 8 nor gates explained in the previous part and used LEDs to indicated the logic level of my flip-flops. I used the resistor with the bands as followed (Brown, Black, Red, Gold) which is 1 kilo ohm and 5% tolerance. The way I arrived at their values was that we had a 5 Volt generator and the data sheet specified the current being at max 400 micro amps. Using ohm's law, V/ I = theoretical resistor value to be 1250 ohms, which with the resistor tolerance can withstand that current flow.

Electrical Characteristics

(Ta = –20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage	V_{IH}	2.0	—	—	V		
	V_{IL}	—	—	0.8	V		
Output voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = –400 µA	
	V_{OL}	—	—	0.5	V	I_{OL} = 8 mA	V_{CC} = 4.75 V, V_{IH} = 2 V
		—	—	0.4		I_{OL} = 4 mA	

Figure 6

The HD74LS00 datasheet

Pin Arrangement

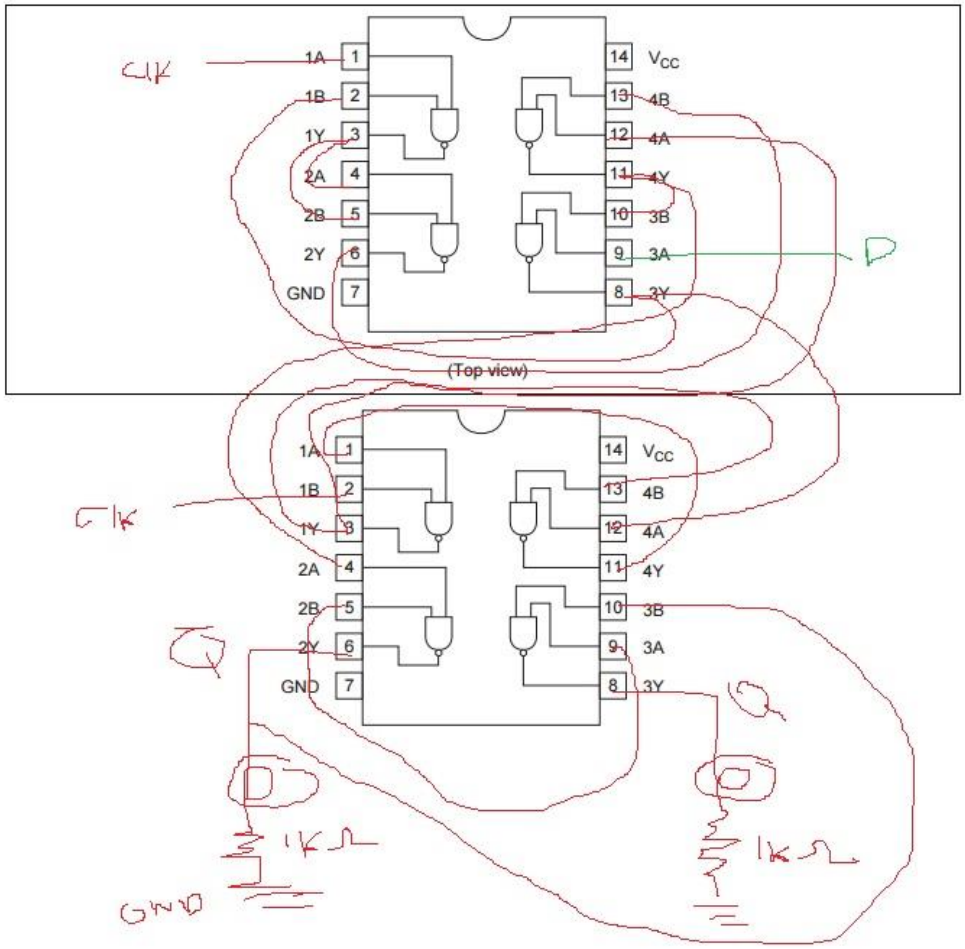


Figure 7

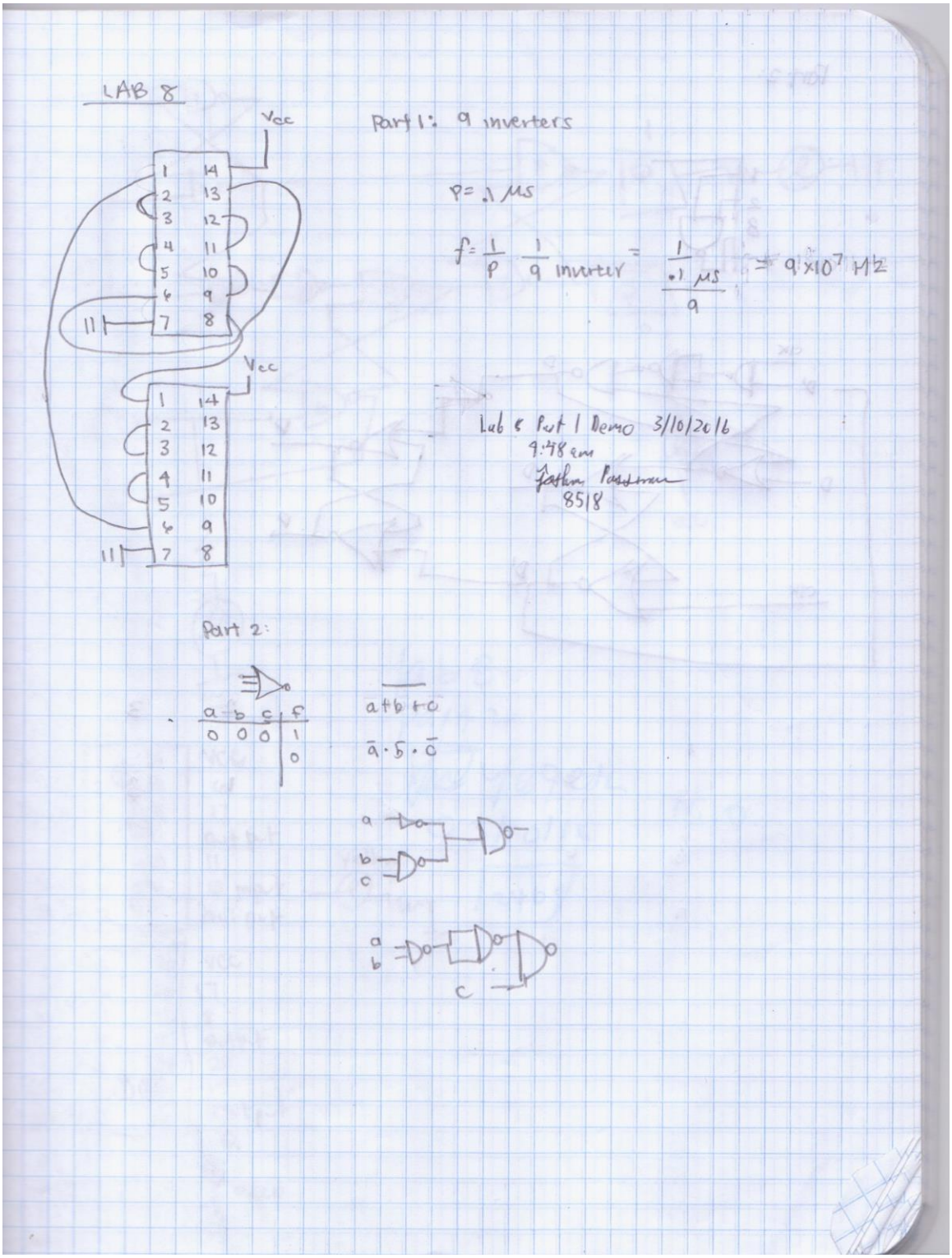
The wiring diagram for Part II of Lab 8

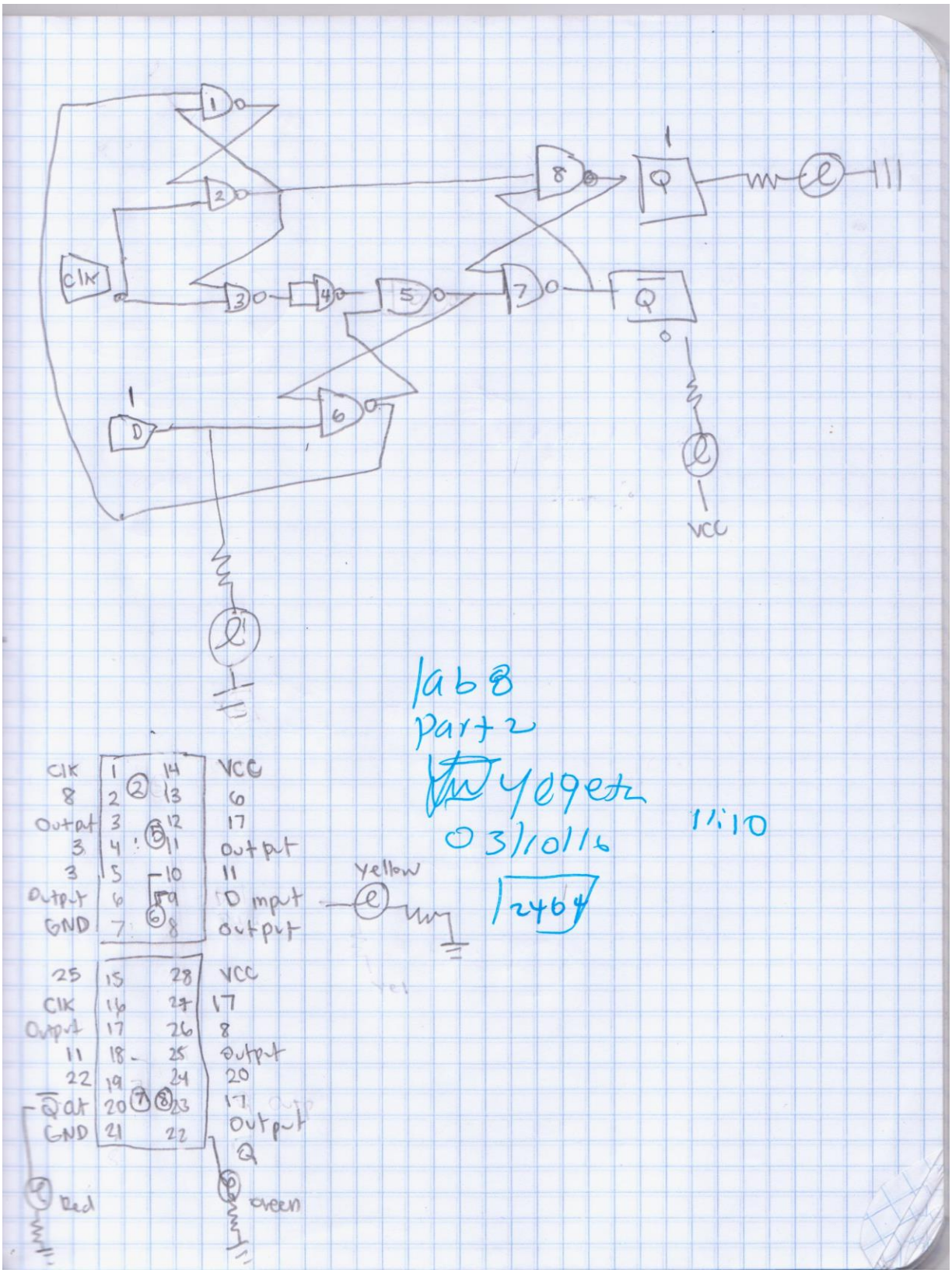
Conclusion

This lab helped demonstrate the physical design of a ring oscillator along with a positive edge triggered flip flop. Using Texas instrument manuals, I was able to build and create these circuits along with compare theoretical values with experimental values. For example, I used the datasheet to come up with a theoretical value resistor, along with using ohm's law to help not fry my LEDs. As well, the delay time in the datasheet helped me come up with the theoretical value of the frequency, which helped me predict what the waveform of Part I should look like. Through these theoretical results, I was successful in creating a physical logic design and was close enough with my experimental values.

Along with that I learned that the grader grades strict like there is no tomorrow. As for me, I finally finished the class and finally won't have such a rough time with these graders. Hope you can relax in life and enjoy it. Best Armando.

Appendix:


LAB 8
Vcc
Part 1: 9 inverters
P = .1 μs
f = 1/P 1/9 inverter = 1/(.1 μs/9) = 9 x 10^7 Hz
Lab 8 Part 1 Demo 3/10/2016
9:48 am
8518
Part 2:
a b c f
0 0 0 1
0
a+b+c
ā · b̄ · c̄


CLK
D
Q
VCC
lab 8
part 2
3/10/16
1:10
CLK 1 14 VCC
8 2 13 6
Output 3 12 17
3 4 11 output
3 5 10 11
Output 6 9 D input
GND 7 8 output
25 15 28 VCC
CLK 16 27 17
Output 17 26 8
11 18 25 output
22 19 24 20
Q out 20 23 17
GND 21 22 output
Q
Red
Green
Yellow