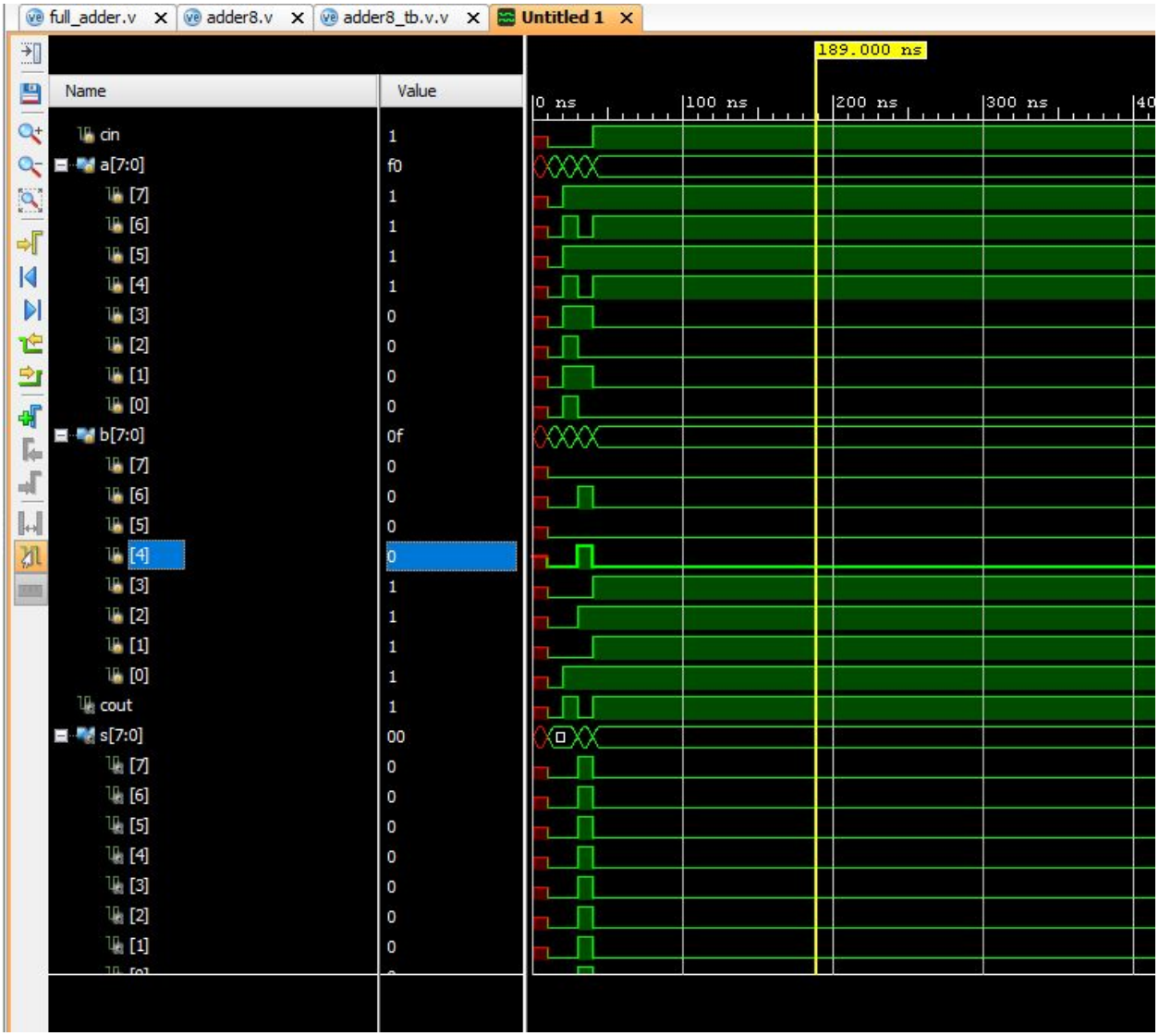
Lab 1

Title: Verilog Design Entry, Synthesis, and Behavioral Simulation
Date: 6/12/2018

Procedure:
Using Vivado, a new project was created in which a full adder module was created. Verilog code to do so was provided. After this, several full adders were combined to create an 8 bit adder, adder8. Finally, a testing file called adderh_tb was created from code given in lab. The test consisted of a timed setting of inputs and displaying of outputs. At time = 5 ns, inputs were set to certain values, and then at time = 10, the outputs were displayed to the console, this was repeated for t = 15, 20, 25, etc. The results of the test were viewed by running a simulation with XSim, in which adder8_tb was set as the sole simulation source.

Results:
A snapshot of the results of the test is shown below. Further details can be found in the google drive under 01.



Summary/Conclusion:
Through the course of this lab, students received their first taste of the design/create process using vivado (with less emphasis placed on design). Using typical design procedure, an 8-bit adder (the most basic component of any machine) was created and fully tested.