Lab 3

Title: Downloading to the FPGA Board
Date: 6/19/2018

Procedure:
In this lab, files from lab 2 were saved into the new folder, and downloaded to the basys3 board. To this end, a bitstream was generated using Vivado's built-in software, and the basys3 board was connected to the computer via micro USB and connected via "open target" in the hardware manager of Vivado. Finally, the program was downloaded to the device via the JTAG method (the program is erased upon powering off). After verifying that the 8 bit adder was working properly, an 8 bit subtractor was created and downloaded onto the device. The method by which this was achieved was by implementing an 8 bit adder with full adders, but instead adding the two's complement of the second number to the first (ones-complement the number and then set the carry bit to 1). Code for all of this can be found in the google drive under 03. The lab concluded with downloading the 8 bit subtractor to the basys3 and verifying its correctness.

Results:
All code for the lab can be found in the google drive under 03.

Summary/Conclusion:
The purpose of this lab was to teach students about downloading programs to devices and to also provide the first opportunity for independent programming. To this end, the 8-bit adder was downloaded to the basys3 board, and then utilized in the creation of an 8-bit subtractor, which was also downloaded to the basys3 board.