AN98488

Quick Guide to Common Flash Interface

Common Flash Interface (CFI) is a standard introduced by the Joint Electron Device Engineering Council (JEDEC) to allow in-system or programmer reading of flash device characteristics. Refer to the JEDEC CFI publications JEP137B and JESD68.01.

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1 Introduction

Common Flash Interface (CFI) is a standard introduced by the Joint Electron Device Engineering Council (JEDEC) to allow in-system or programmer reading of flash device characteristics, which is equivalent to having data sheet parameters located in the device. The JEDEC Solid State Technology Association defines industry standards for semiconductor devices, with CFI being one of the many. The CFI is used to standardize flash device characteristics and to define feature differences between various flash manufacturers. For a detailed definition of CFI, see the JEDEC CFI publications JEP137 and JESD68.

2 Common Flash Interface

CFI is a way of defining the flash device characteristics in silicon. It is implemented in a set of tables that define the various characteristics of the flash device, which application software can interrogate. CFI tables are divided into the following five separate parts:

- CFI Query Identification String
- System Interface String
- Device Geometry Definition
- Primary Vendor-Specific Extended Query
- Alternate Vendor-Specific Extended Query

The CFI Query Identification String, System Interface String, and Device Geometry Definition table descriptions are identical for all flash manufacturers. The Primary Vendor-Specific Extended Query and Alternate Vendor-Specific Extended Query table sections allow flash manufacturers to indicate unique features.

CFI addressing depends on the device and its mode of operation. For devices that are x8-only, x16-only, x32-only, x8/x16-capable, but operating in the x16-mode, or x16/x32-capable but operating in the x32 mode, byte addressing starts at 10h and is incremented by a factor of one. For x8/x16-capable devices operating in the x8-mode or x16/x32-capable device operating in the x16-mode, word addressing starts at 20h and is incremented by a factor of two. For x8/x32-capable devices operating in the x8-mode, double-word addressing starts at 40h and is incremented by a factor of four.

CFI addressing in the following examples are shown with the maximum data bus width, which means x32 or x16/x32 capable device in x32-mode, x16 or x8/x16 capable device in x16-mode, and x8 device in x8-mode. CFI codes are taken from various flash devices; these do not represent individual devices.

2.1 Cypress CFI Implementation

Not all Cypress flash devices implement all the five CFI parts.

For parallel NOR flash, Alternate Vendor- Specific Extended Query is not implemented, while all the other four parts are implemented.

For SPI flash, FL-K and FL-P do not have CFI tables implemented. FL-S and FS-S implement all the five CFI parts, including Primary Vendor-Specific Extended Query, and Alternate Vendor- Specific Extended Query table sections.

3 CFI Tables

3.1 CFI Query Identification String

The CFI Query Identification String table starts from the flash device physical address 10h and ends at 1Ah.

Addresses 10h to 12h define the ASCII string “QRY” that is used in Query Structure Output to indicate the flash device bus width and its bus mode.

Table 1. Query Structure Output

Address	Data (x8)	Data (x16)	Definition
10h	51h	0051h	'Q' in ASCII
11h	52h	0052h	'R' in ASCII
12h	59h	0059h	'Y' in ASCII

Addresses 13h and 14h define the flash manufacturer identification number, or the Primary Vendor Command Set and Control Interface ID Code. The Cypress Manufacturer ID for flash devices is 0002h (historically the AMD ID is 0002h and the Fujitsu ID is 0004h; the former Spansion ID is 0002h).

In the CFI tables, lower and upper bytes are assigned to consecutive addresses whenever a definition can have a 16-bit data value. For example, the Manufacturer ID value is 0002h. For the x8 case, the lower data byte is 02h at Address 13h and the upper data byte is 00h at Address 14h. For the x16 case, the data values are the same, but 00h is added as the high byte to each data value.

Table 2. Primary Vendor Command Set and Control Interface ID Code

Address	Data (x8)	Data (x16)	Definition
13h	02h	0002h	Manufacturer ID Lower Byte
14h	00h	0000h	Manufacturer ID Upper Byte

Addresses 15h and 16h define the starting address of the Primary Vendor-Specific Extended Query table. The starting address for the Primary Vendor-Specific Extended Query table starts at address 40h for Cypress products, whereas it may start at address 31h for other manufacturers.

Table 3. Primary Vendor-Specific Extended Query

Address	Data (x8)	Data (x16)	Definition
15h	40h	0040h	Starting Address for the Primary Vendor-Specific Extended Query table Lower Byte
16h	00h	0000h	Starting Address for the Primary Vendor-Specific Extended Query table Upper Byte

Addresses 17h and 18h define the alternate flash manufacturer identification number or the Alternate Vendor Command Set and Control Interface ID Code. Cypress NOR devices do not implement this feature, so the data is

00h 00h (none exists). Cypress SPI FL-S and FS-S devices have this feature implemented; the data is 46h 53h, which is ASCII characters “FS”. “F” is for SPI interface; “S” represents the 65-nm Technology Node.

Table 4. Alternate Vendor Command Set and Control Interface ID Code

Address	Data	Definition
17h	00h/53h	Alternate Manufacturer ID Lower Byte
18h	00h/46h	Alternate Manufacturer ID Upper Byte

Addresses 19h and 1Ah define the starting address of the Alternate Vendor-Specific Extended Query table.

Cypress NOR devices do not implement this feature; the data is 00h 00h (none exists). The starting address for the Alternate Vendor-Specific Extended Query table for Cypress SPI FL-S and FS-S starts at Address 51h.

Table 5. Alternate Vendor-Specific Extended Query

Address	Data	Definition
19h	00h/51h	Starting Address for Alternate Vendor-Specific Extended Query table Lower Byte
1Ah	00h	Starting Address for Alternate Vendor-Specific Extended Query table Upper Byte

3.2 System Interface String

The System Interface String table starts from the flash device physical address 1Bh and ends at 26h.

Addresses 1Bh and 1Ch define the minimum and maximum limits of the Power Supply Voltage (V_{CC}). Note that when rounding the V_{CC}, the lower limit (address 1Bh) should always be rounded up and the higher limit (address 1Ch) should always be rounded down.

Table 6. Power Supply Voltage

Address	Data	Definition
1Bh	27h	27 / 10 = 2.7 V V_{CC} lower limit (D7-D4: V, D3-D0: 100 mV)
1Ch	36h	36 / 10 = 3.6 volts V_{CC} upper limit (D7-D4: V, D3-D0: 100 mV)

Addresses 1Dh and 1Eh define the minimum and maximum limits of the Dual Supply Programming Voltage (V_{PP}). This is only available on legacy devices since newer devices have migrated to single-supply programming.

Table 7. Dual Supply Programming Voltage

Address	Data	Definition
1Dh	00h	V_{PP} lower limit (00h = no V_{PP} pin present)
1Eh	00h	V_{PP} upper limit (00h = no V_{PP} pin present)

Addresses 1Fh and 23h define the typical and maximum timeout values of single byte/word programming in microseconds. Typical time = 2^N µs and maximum time = 2^N times typical.

Table 8. Single Byte/Word Programming

Address	Data	Definition
1Fh	07h	2^7 = 128 µs Typical word programming time from Erase and Programming Performance table in the datasheet
23h	01h	2^1 = 2 -> 2*128 µs = 256 µs Maximum word programming time, which is the maximum programming time expected before a timeout is generated

Addresses 20h and 24h define the typical and maximum timeout values of the entire buffer programming in microseconds. Typical time = 2^N µs and maximum time = 2^N times typical. For SPI, it is for Page Program.

Table 9. Buffer Programming Timeout Values

Address	Data	Definition
20h	07h	2^7 = 128 µs typical buffer programming time
24h	05h	2^5 = 32 -> 32*128 µs = 4096 µs maximum buffer programming time

Addresses 21h and 25h define the typical and maximum timeout values of the sector erase operation in milliseconds. Typical time = 2^N ms and maximum time = 2^N times typical.

Sector and block are equivalent names for the smallest erasable size in Cypress flash memories. The boot sector flash memory contains multiple sector sizes, but the Address 21h definition corresponds to the time taken to erase the largest sector size of the device.

Table 10. Sector Erase Timeout Values

Address	Data	Definition
21h	0Ah	2^{10} = 1024 ms Typical sector erase time
25h	04h	2^4 = 16 -> 16*1024 ms = 16,384 ms Maximum sector erase time

Addresses 22h and 26h define the typical and maximum timeout values of the chip erase operation in milliseconds. Typical time = 2^N ms and maximum time = 2^N times typical.

Table 11. Chip Erase Timeout Values

Address	Data	Definition
22h	4Fh	2^N ms Typical chip erase time
26h	04h	2^N = N * typical chip erase time Maximum chip erase time (00h = not supported)

3.3 Device Geometry Definition

The Device Geometry Definition table starts from the flash device physical address 27h and ends at 3Ch.

Address 27h defines the device density in bytes.

Table 12. Device Density

Address	Data	Definition
27h	17h	17h = 23 -> 2^{23} = 8 MB

Addresses 28h and 29h define the flash device data bus interface. It defines parallel NOR and SPI flash interfaces. For parallel NOR, these values are as follows:

00h = x8-only interface

01h = x16-only interface

02h = x8/x16 interface

03h = x32 interface

Table 13. Data Bus Interface — Parallel NOR

Address	Data	Definition
28h	02h	x8/x16 interface Lower byte
29h	00h	x8/x16 interface Upper byte

For SPI serial Flash devices:

04h = Single I/O SPI, 3-byte address

05h = Multi I/O SPI, 3-byte address

0102h = Multi I/O SPI, 3- or 4-byte address

Table 14. Data Bus Interface — SPI Flash

Address	Data	Definition
28h	04h	SPI flash interface Lower byte
29h	00h	SPI flash interface Upper byte

Addresses 2Ah and 2Bh define the maximum number of bytes in a multi-byte write operation, which is equal to 2^N. 00h is indicated if the multi-byte write feature not supported.

Table 15. Maximum Number of Bytes

Address	Data	Definition
2Ah	05h	2^5 = 32 bytes / Buffer length Lower byte
2Bh	00h	Buffer length Upper byte

Addresses 2Ch through 3Ch define the Erase Block regions of the flash device. The information stored at these address locations indicate how the flash memory map is organized.

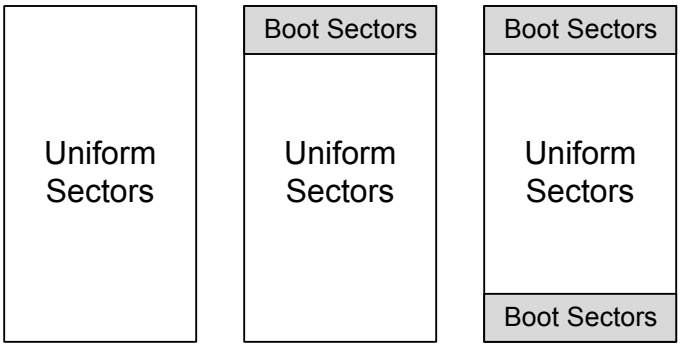
Address 2Ch defines the number of Erase Block regions within the flash device.

Table 16. Number of Erase Block Regions

Address	Data	Definition
2Ch	01h	Number of Erase Block regions

Figure 1 shows some examples of defining the number of erase block regions within a Cypress flash device.

Figure 1. Examples of Erase Block Regions



Each erase block region refers to a group of sectors that have the same sector size. For example, a flash device with Uniform Sectors has sectors of the same size across the entire flash array; the number of erase block regions for this flash device is 01h.

A top or bottom boot flash device has uniform, smaller-size boot sectors at the top or the bottom. The rest of the flash array is of uniform larger-size sectors; thus, there are two Erase Block regions and the number of erase block regions is 02h.

A top and bottom boot flash device has uniform smaller-size boot sectors at both top bottom. The rest of the flash array has larger-sized uniform sectors; thus, there are three Erase Block regions and the number of erase block regions is 03h.

Addresses 2Dh through 30h, 31h through 34h, 35h through 38h, and 39h through 3Ch define the information of Erase Block Regions 1, 2, 3, and 4, respectively. These include the following:

1. The number of sectors
2. The sector size inside each Erase Block region.

The lower two addresses specify the number of sectors. The number of sectors equals the CFI data plus 1. For example, if the data in the CFI table is 07h, then the number of sectors in the Erase Block region is 8.

The upper two addresses specify the sector size. The sector size equals the CFI data multiplied by 256 bytes. For example, if the data in the CFI table is 20h, then the sector size is 20h x 256 (decimal) bytes, which is 8 KB.

Table 17 is an example of a top-and-bottom boot flash. At both ends of the memory map, there are eight 8-KB boot sectors. Besides the boot sectors located at the two ends of the memory map, there are 64-KB uniform sectors between the top and bottom boot sectors. Boot sectors at each end of the memory map can be classified as individual regions, while all uniform sections are another region. Thus, there are three regions, which include the first eight boot sectors, the middle uniform sectors, and then the second eight boot sectors. Each of the three regions is defined as below:

Table 17. Region 1

Address	Data	Definition
2Dh	07h	07h = 07h + 01h = 8 sectors Lower byte
2Eh	00h	number of sectors Upper byte
2Fh	20h	20h = 32 * 256 bytes = 8-KB sector size Lower byte
30h	00h	Sector size Upper byte

Table 18. Region 2

Address	Data	Definition
31h	FDh	FDh = FDh + 01h = FEh = 254 sectors Lower byte
32h	00h	number of sectors Upper byte
33h	00h	100h = 256 * 256 bytes = 64-KB sector size Lower byte
34h	01h	sector size Upper byte

Table 19. Region 3 (Sheet 1 of 2)

Address	Data	Definition
35h	07h	07h = 07h + 01h = 8 sectors Lower byte
36h	00h	Number of sectors Upper byte

Table 19. Region 3 (Sheet 2 of 2)

Address	Data	Definition
37h	20h	20h = 32 * 256 bytes = 8KB sector size Lower byte
38h	00h	Sector size Upper byte

The unused erase block regions, address 39h through 3Ch, are left empty at 00h.

3.4 Primary Vendor-Specific Extended Query

Addresses 40h to 42h define the ASCII string “PRI”. The string PRI indicates the beginning of the Primary Vendor-Specific Extended Query table.

Table 20. Primary Vendor-Specific Extended Query

Address	Data	Definition
40h	50h	'P' in ASCII
41h	52h	'R' in ASCII
42h	49h	'I' in ASCII

Address 43h and 44h defines the Major and Minor version number of the Cypress CFI version implemented.

Table 21. Cypress CFI Version

Address	Data	Definition
43h	31h	Version 1.4 major version number '1' in ASCII
44h	34h	Version 1.4 minor version number '4' in ASCII

Address 45h specifies whether the flash device has the Address-Sensitive Unlock functionality and indicates the Process Technology of the flash device.

The Address-Sensitive Unlock functionality shows that the addresses during command cycles are don't cares.

DQ7-DQ6 are reserved

DQ5-DQ2 defines the Process Technology

DQ1-DQ0 defines the Address-Sensitive Unlock; 0 = Supported, 1 = Not Supported

Table 22. Address-Sensitive Unlock and Process Technology

Address	Data	Definition
45h	08h	08h = 00001000b
		DQ1-DQ0 -> 00b -> Address-Sensitive Unlock supported
		DQ5-DQ2 -> 0000b -> 230-nm Floating Gate technology 0001b -> 170-nm Floating Gate technology 0010b -> 230-nm MirrorBit technology 0011b -> 130-nm Floating Gate technology 0100b -> 110-nm MirrorBit technology 0101b -> 90-nm MirrorBit technology 0110b -> 90-nm Floating Gate technology 0111b -> 65-nm MirrorBit Eclipse technology 1000b -> 65-nm MirrorBit technology 1001b -> 45-nm MirrorBit technology
		DQ7-DQ6 -> 00b -> Reserved

Address 46h defines rase Suspend and indicates 00h if Erase Suspend is not supported; 01h if support is for Read Only; or 02h if support is for both Read and Write.

Table 23. Erase Suspend

Address	Data	Definition
46h	02h	Erase Suspend supports both Read and Write operations

Address 47h defines the number of sectors in the smallest Sector Group protected in the flash device.

Table 24. Sector Group

Address	Data	Definition
47h	01h	Sector Protect 00 = Not supported X = Number of sectors in smallest group

Address 48h defines the Temporary Sector Unprotect functionality. Temporary Sector Unprotect is a functionality that unlocks protected sectors by applying a high-voltage V_{ID} to the RESET# pin.

Table 25. Temporary Sector Unprotect

Address	Data	Definition
48h	01h	Temporary Sector Unprotect 00 = Not supported 01 = Supported

Address 49h defines the Sector Protection Scheme.

Table 26. Sector Protection Scheme

Address	Data	Definition
49h	04h	Sector Protect/Unprotect Scheme

Table 27 provides different data code and definition mode options for Address 49h, as shown in Table 26.

Table 27. Address 49h Data and Definition Table

Data Code	Definition Mode
04h	High-Voltage Method
05h	Software Command-Locking Method
08h	Advanced Sector-Protection Method
09h	Secure

Address 4Ah specifies whether simultaneous operations are supported and the number of banks in the flash device.

Table 28. Number of Sectors Outside Bank 1

Address	Data	Definition
4Ah	00h	Simultaneous operation 00 = Not supported X = Number of banks

Address 4Bh defines if the flash device supports burst mode.

Table 29. Burst Mode

Address	Data	Definition
4Bh	00h	Burst Mode 00 = Not supported 01 = Supported

Address 4Ch specifies whether the flash device supports page mode and page size.

Table 30. Page Mode

Address	Data	Definition
4Ch	00h	Not supported
	01h	4-word page supported
	02h	8-word page supported
	03h	16-word page supported (for NOR) 256-byte program page (for SPI)
	04h	512-byte program page (for SPI)

Addresses 4Dh and 4Eh define the minimum and maximum limits of the Acceleration Power Supply Voltage (A_{CC}). Bits 7-4 represent the volts in hex, while bits 3-0 represent the BCD equivalent value in 100-mV increments. Data 00h means that this feature is not supported.

Table 31. Acceleration Power Supply Voltage

Address	Data	Definition
4Dh	B5h	11.5 V (Bits 7-4: 1011 and Bits 3-0: 0101) A_{CC} lower limit
4Eh	C5h	12.5 V (Bits 7-4: 1100 and Bits 3-0: 0101) A_{CC} higher limit

Address 4Fh specifies whether the flash device consists of uniform sectors, uniform sectors mixed with boot sectors, and the write protect function from the WP# pin.

00 = Flash device without WP Protect

01 = Eight 8-KB sectors at TOP and Bottom with WP Protect (for NOR)

= Whole Chip (for SPI)

02 = Bottom Boot Device with WP Protect

03 = Top Boot Device with WP Protect

04 = Uniform, Bottom WP Protect

05 = Uniform, Top WP protect

06 = WP protect for all sectors

07 = Uniform, Top or Bottom WP protect (user selected)

Table 32. Sector and WP# Pin Protection Scheme

Address	Data	Definition
4Fh	02h	Bottom Boot with WP#

Address 50h defines Program Suspend. For SPI, 50h is the last CFI Primary Vendor-Specific Extended Query data. Starts from 51h, is CFI Alternate Vendor-Specific Extended Query data.

Table 33. Program Suspend

Address	Data	Definition
50h	01h	Program suspend 00 = Not supported 01 = Supported

Address 57h defines Bank Organization. If data at Address 4Ah is 00h, indicating that Simultaneous Operation is not supported, Address 57h will also indicates 00h.

Table 34. Bank Organization

Address	Data	Definition
57h	04h	04h = 04 = Number of Banks

Addresses 58h to 5Bh define the “Bank Region Information” – the number of sectors in bank for Banks 1, 2, 3, and 4 respectively.

Table 35. Bank Region Information

Address	Data	Definition
58h	27h	Bank A Region Information: 27h = 39 = Number of sectors in Bank 1
59h	60h	Bank B Region Information: 60h = 96 = Number of sectors in Bank 2
5Ah	60h	Bank C Region Information: 60h = 96 = Number of sectors in Bank 3
5Bh	27h	Bank D Region Information: 27h = 39 = Number of sectors in Bank 4

3.4.1 Primary Vendor-Specific Extended Query Changes in Version 1.4 and Newer

Cypress 65-nm and newer parallel NOR devices implement Version 1.4 and newer Primary Vendor-Specific Extended Query. There are some new parameters added that are not defined in version 1.3 and earlier versions.

Address 51h defines the Unlock Bypass feature.

Table 36. Unlock Bypass

Address	Data	Definition
51h	01h	Unlock Bypass 00 = Not supported 01 = Supported

Address 52h defines the Secured Silicon Sector (Customer OTP Area) size in bytes. The sector size is two to the power of N. For example, if the CFI data is 09h, the Secured Silicon Sector Size is 2 to the power of 9, which equals 512 bytes.

Table 37. Secured Silicon Sector Size

Address	Data	Definition
52h	09h	Secured Silicon Sector (Customer OTP Area) Size 2^N (bytes)

Address 53h defines the software features supported in the flash device. Each bit represents a software feature; a ‘1’ specifies that it is supported, while a ‘0’ specifies that it is not supported. The software features are defined as below:

Bit 0: status register polling (1 = supported, 0 = not supported)

Bit 1: DQ polling (1 = supported, 0 = not supported)

Bit 2: New program suspend/resume commands (1 = supported, 0 = not supported)

Bit 3: Word programming (1 = supported, 0 = not supported)

Bit 4: Bit-field programming (1 = supported, 0 = not supported)

Bit 5: Autodetect programming (1 = supported, 0 = not supported)

Bit 6: RFU

Bit 7: multiple writes per Line (1 = supported, 0 = not supported)

Table 38. Software Features

Address	Data	Definition
53h	8Fh	Software features

Address 54h defines the Page Size in bytes. The Page Size is two to the power of N. For example, if the CFI data is 05h, the Page Size is 2 to the power of 5, which equals 32 bytes.

Table 39. Page Size

Address	Data	Definition
54h	05h	Page Size = 2^N bytes

Address 55h defines the Erase Suspend Maximum Timeout time in us. The maximum timeout time is 2 to the power of N. For example, if the CFI data is 06h, the Erase Suspend Maximum Timeout time is 2 to the power of 6, which equals 64 μs.

Table 40. Erase Suspend Maximum Timeout

Address	Data	Definition
55h	06h	Erase Suspend Timeout Maximum < 2^N (μs)

Address 56h defines the Program Suspend Maximum Timeout time in μs. The maximum timeout time is 2 to the power of N. For example, if the CFI data is 06h, the Program Suspend Maximum Timeout time is 2 to the power of 6, which equals 64 μs.

Table 41. Program Suspend Maximum Timeout

Address	Data	Definition
56h	06h	Program Suspend Timeout Maximum < 2^N (μs)

Addresses 5Ch to 77h are added to define the “Bank Region Information” – the number of sectors in the bank for Bank 5 to Bank 32.

Address 78h defines the Embedded Hardware Reset Maximum Timeout time in μs. Embedded Hardware Reset refers to a reset with the Reset Pin. The maximum timeout time is 2 to the power of N. For example, if the CFI data is 06h, the Embedded Hardware Reset Maximum Timeout time is 2 to the power of 6, which equals 64 μs.

Table 42. Embedded Hardware Reset Maximum Timeout

Address	Data	Definition
78h	06h	Embedded Hardware Reset Timeout Maximum < 2^N (μs)

Address 79h defines the Non-Embedded Hardware Reset Maximum Timeout time in μs. Non-Embedded Hardware Reset refers to Power-on-Reset. The maximum timeout time is 2 to the power of N. For example, if the CFI data is 09h, the Non-Embedded Hardware Reset Maximum Timeout time is 2 to the power of 9, equals to 512 μs.

Table 43. Non-Embedded Hardware Reset Maximum Timeout

Address	Data	Definition
79h	09h	Non-Embedded Hardware Reset Timeout Maximum < 2^N (μs)

3.5 Alternate Vendor-Specific Extended Query

Cypress parallel NOR devices do not have Alternate Vendor-Specific Extended Query table implemented. Currently only SPI FL-S and FS-S families implement this feature.

In FL-S and FS-S, Addresses 51h to 53h define the ASCII string “ALT”. The string ALT indicates the beginning of the Alternate Vendor-Specific Extended Query table.

Table 44. Alternate Vendor-Specific Extended Query String

Address	Data	Definition
51h	41h	'A' in ASCII
52h	4Ch	'L' in ASCII
52h	54h	'T' in ASCII

Addresses 54h and 55h define the Major and Minor version numbers of the Alternate Vendor-Specific Extended Query implemented.

Table 45. Alternate Vendor-Specific Extended Query Version

Address	Data	Definition
54h	32h	Major version number = 2, ASCII
55h	30h	Minor version number = 0, ASCII
52h	54h	'T' in ASCII

For more detail parameter definitions, see the FL-S and FS-S datasheets.

4 Conclusion

This application note provides the user with an understanding of how to derive the CFI table data, which are listed in Cypress Parallel NOR and SPI (FL-S and FS-S) flash data sheets.

Cypress supports the CFI tables in all parallel NOR Flash families and FL-S, FS-S SPI flash families.

Document History Page

Document Title: AN98488 - Quick Guide to Common Flash Interface Document Number: 001-98488				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**			03/28/2008	Initial release
*A			06/05/2008	Minor update to Section 3.3; Changes to Table 3.23
*B	4909544	YOQI	09/05/2015	Updated in Cypress template
*C	4922334	MSWI	09/16/2015	Edited the document

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