

Goal: Reduce power consumption in a chip (IC)

Objective: Introduction to CMOS power & power dissipation sources in CMOS circuits.

Topics: 1. Some definitions related to power

2. Switching power

3. Sources of power dissipation in CMOS devices

Definitions

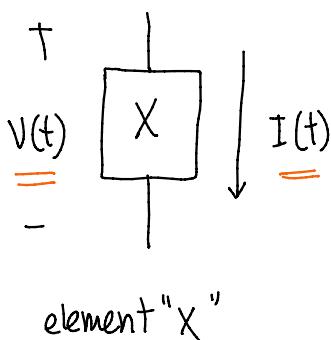
At any moment, an electronic element has ① a current through the element $I(t)$

② a voltage across the element $V(t)$

③ the relationship between I and V

is called the I-V characteristics

(usually governed by some law)



Instantaneous power

The instantaneous power $P(t)$ consumed or supplied by a circuit element

$$P(t) = V(t) I(t)$$

Energy

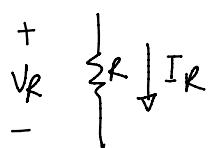
The energy consumed or supplied over some time interval "T", $E = \int_0^T P(t) dt$

Average power

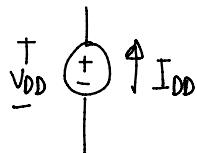
The average power over this interval "T", $P_{avg} = \frac{E}{T} = \frac{1}{T} \int_0^T P(t) dt$

Examples

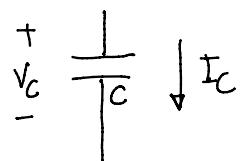
① Resistor



② Voltage source



③ Capacitor



I-V:

$$V = IR$$

$$V = \text{constant}$$

$$I_C = C \cdot \frac{dV_C}{dt}$$

Power: $P(t) = V_R(t) I_R(t) = \frac{V_R(t)}{R} = I_R^2(t) R$

$$P(t) = V_{DD} I_{DD}(t)$$

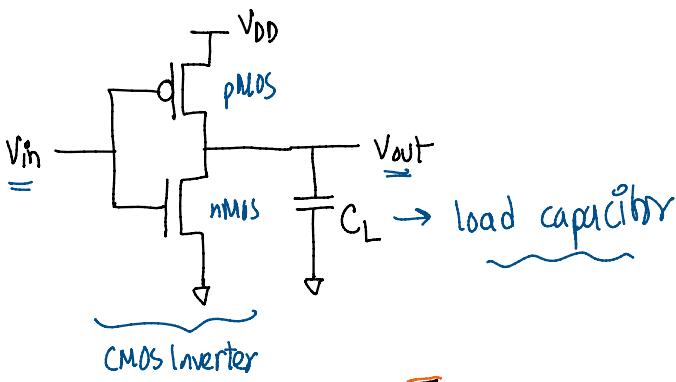
$$P(t) = V_C(t) I_C(t) = V_C(t) C \frac{dV_C}{dt}$$

Energy: $E = \int_0^T P(t) dt$

$$E = \int_0^T P(t) dt = \int_0^T V_{DD} I_{DD}(t) dt$$

$$\begin{aligned} E &= \int_0^{V_C} V_C(t) C \frac{dV_C}{dt} dt \\ &= \int_0^{V_C} C V_C(t) dV_C = \frac{1}{2} C V_C^2 \end{aligned}$$

CMOS inverter driving a load capacitance



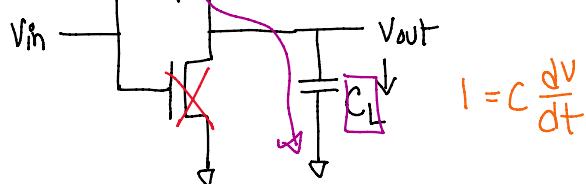
Case 1: $V_{in} : \underline{\underline{1}} \rightarrow \underline{\underline{0}}$ $V_{out} : \underline{\underline{0}} \rightarrow \underline{\underline{1}}$

Capacitor: Charging to V_{DD} through pMOS

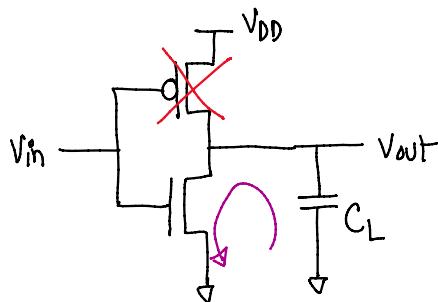
Case 2: $V_{in} : \underline{\underline{0}} \rightarrow \underline{\underline{1}}$ $V_{out} : \underline{\underline{1}} \rightarrow \underline{\underline{0}}$

Capacitor: Discharging to ground through nMOS

$$E_C = \frac{1}{2} C_L V_{DD}^2$$



$$I = C \frac{dV}{dt}$$



$$E_{V_{DD}} = \int_0^{\infty} I(t) V_{DD} dt = V_{DD} \int_0^{\infty} C \frac{dV_C}{dt} dt = V_{DD} \cdot C_L \cdot V_{DD} = C_L V_{DD}^2$$

Switching power of CMOS :

$\underline{\underline{V_{DD}}}$ charging & discharging C

Suppose, gate switches at some average frequency " f_{sw} " over some time " T ".

\therefore The load capacitor (C) will be charged and discharged : $f_{sw} \cdot T$ times

\therefore The load capacitor (C) will be charged and discharged : $f_{sw} \cdot T$ times
 switched

Energy required to charge & discharge a capacitor (C) with supply (V_{DD}) once : $\underline{\underline{C V_{DD}^2}}$

Total energy required for switching, $E_{switching} = f_{sw} T \cdot C V_{DD}^2$

Average power dissipated during this period, $P_{switching} = \frac{E_{switching}}{T} = \frac{f_{sw} T C V_{DD}^2}{T} = \underline{\underline{f_{sw} C V_{DD}^2}}$

Define $\alpha \triangleq \frac{f_{sw}}{f}$ where f is the clock frequency, α is activity factor

$$\Rightarrow f_{sw} = \alpha \cdot f$$

$$P_{switching} = f_{sw} \cdot C V_{DD}^2 = \alpha f C V_{DD}^2$$

$$P_{switching} = \alpha f C V_{DD}^2$$

$V_{DD} \rightarrow$ supply voltage

$C \rightarrow$ capacitance

$f \rightarrow$ clock frequency

$\alpha \rightarrow$ activity factor

Sources of power dissipation :

① Dynamic power dissipation

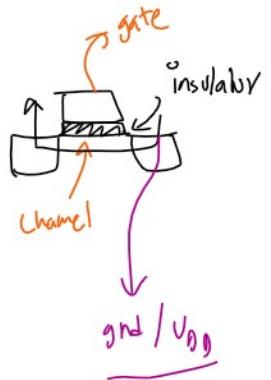
→ charging & discharging load capacitances as gates switch $P_{switching}$

→ "short-circuit" current when the PUN & PDN are momentarily "ON" $P_{shortcircuit}$

$$P_{dynamic} = P_{switching} + P_{shortcircuit}$$

② Static power dissipation:

- subthreshold leakage through "off" transistors I_{sub}
- gate leakage through gate dielectric insulator I_{gate}
- junction leakage from source/drain diffusions I_{junct}
- contention current in ratioed circuits $I_{\text{contention}}$



$$P_{\text{static}} = (I_{\text{sub}} + I_{\text{gate}} + I_{\text{junct}} + I_{\text{contention}}) V_{\text{DD}}$$

$$P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}}$$

Problem

A digital system-on-chip in a **1 V** 65 nm process (with 50 nm drawn channel lengths and $\lambda = 25 \text{ nm}$) has **1 billion transistors**, of which **50 million** are in logic gates and the remainder in memory arrays. The average logic transistor width is **12 λ** and the average memory transistor width is **4 λ** . The memory arrays are divided into banks and only the necessary bank is activated so the **memory activity factor is 0.02**. The static CMOS logic gates have an average activity factor of 0.1. Assume each transistor contributes **1 fF/ μm** of gate capacitance and **0.8 fF/ μm** of diffusion capacitance. Neglect wire capacitance for now (though it could account for a large fraction of total power). Estimate the **switching power** when operating at **1 GHz**.

logic transistor

$$N_{\text{logic}} = 50 \times 10^6$$

$$V_{\text{DD}} = 1 \text{ V}$$

memory transistor

$$N_{\text{mem}} = 950 \text{ M} = 950 \times 10^6$$

$$V_{\text{DD}} = 1 \text{ V}$$

$$V_{DD} = 1V$$

$$\lambda = 25 \text{ nm}$$

$$W_{\text{logic}} = 12 \lambda$$

$$\alpha_{\text{logic}} = 0.1$$

total cap of 1 transistor = gate + diff

$$\begin{aligned} \text{at unit width} \\ &= 1 \text{ fF}/\mu\text{m} + 0.8 \text{ fF}/\mu\text{m} \\ &= 1.8 \text{ fF}/\mu\text{m} \end{aligned}$$

$$V_{DD} = 1V$$

$$\lambda = 25 \text{ nm}$$

$$W_{\text{mem}} = 4A$$

$$\alpha_{\text{mem}} = 0.02$$

total cap. of 1 unit width

$$\begin{aligned} \text{tran.} &= \text{gate} + \text{diff} \\ &= 1.8 \text{ fF}/\mu\text{m} \end{aligned}$$

total cap. of 1 tran = $1.8 \text{ fF}/\mu\text{m} \times W_{\text{logic}}$

$$\begin{aligned} &= 1.8 \text{ fF}/\mu\text{m} \times 12 \lambda \xrightarrow[25 \text{ nm}]{(= 25 \times 10^{-3} \mu\text{m})} \\ &= 1.8 \text{ fF}/\mu\text{m} \times 12 \times 25 \times 10^{-3} \mu\text{m} \\ &= 0.54 \text{ fF} \end{aligned}$$

total cap. 1 tran = $1.8 \times W_{\text{mem}}$

$$\begin{aligned} &= 1.8 \text{ fF}/\mu\text{m} \times 4 \lambda \\ &= 1.8 \text{ fF} \times 4 \times 25 \times 10^{-3} \\ &= 0.18 \text{ fF} \end{aligned}$$

$$\text{total cap} = N_{\text{logic}} \times 0.54 \text{ fF}$$

↑

$$\begin{aligned} P_{\text{switching(logic)}} &= \alpha_{\text{logic}} C_{\text{logic}} f V_{DD}^2 \\ &= 0.1 \times 50 \times 10^6 \times f V_{DD}^2 \end{aligned}$$

$$\text{total cap} = N_{\text{mem}} \times 0.18 \text{ fF}$$

$$\begin{aligned} P_{\text{switching(mem)}} &= \alpha_{\text{mem}} C_{\text{mem}} f V_{DD}^2 \\ &= 0.02 \times 950 \times 10^6 \times 0.18 \\ &\quad \times 10^{-15} \times f \times V_{DD}^2 \end{aligned}$$

$$P_{\text{switching}} = P_{\text{switching(logic)}} + P_{\text{switching(memory)}}$$

$$= \left(0.1 \times 50 \times 10^6 \times 0.54 \times 10^{-15} + 0.02 \times 950 \times 10^6 \times 0.18 \times 10^{-15} \right) \times$$
$$\frac{f \times V_{DD}^2}{1 \times 10^9 \times 1^2}$$
$$= 6.12 \text{ W}$$