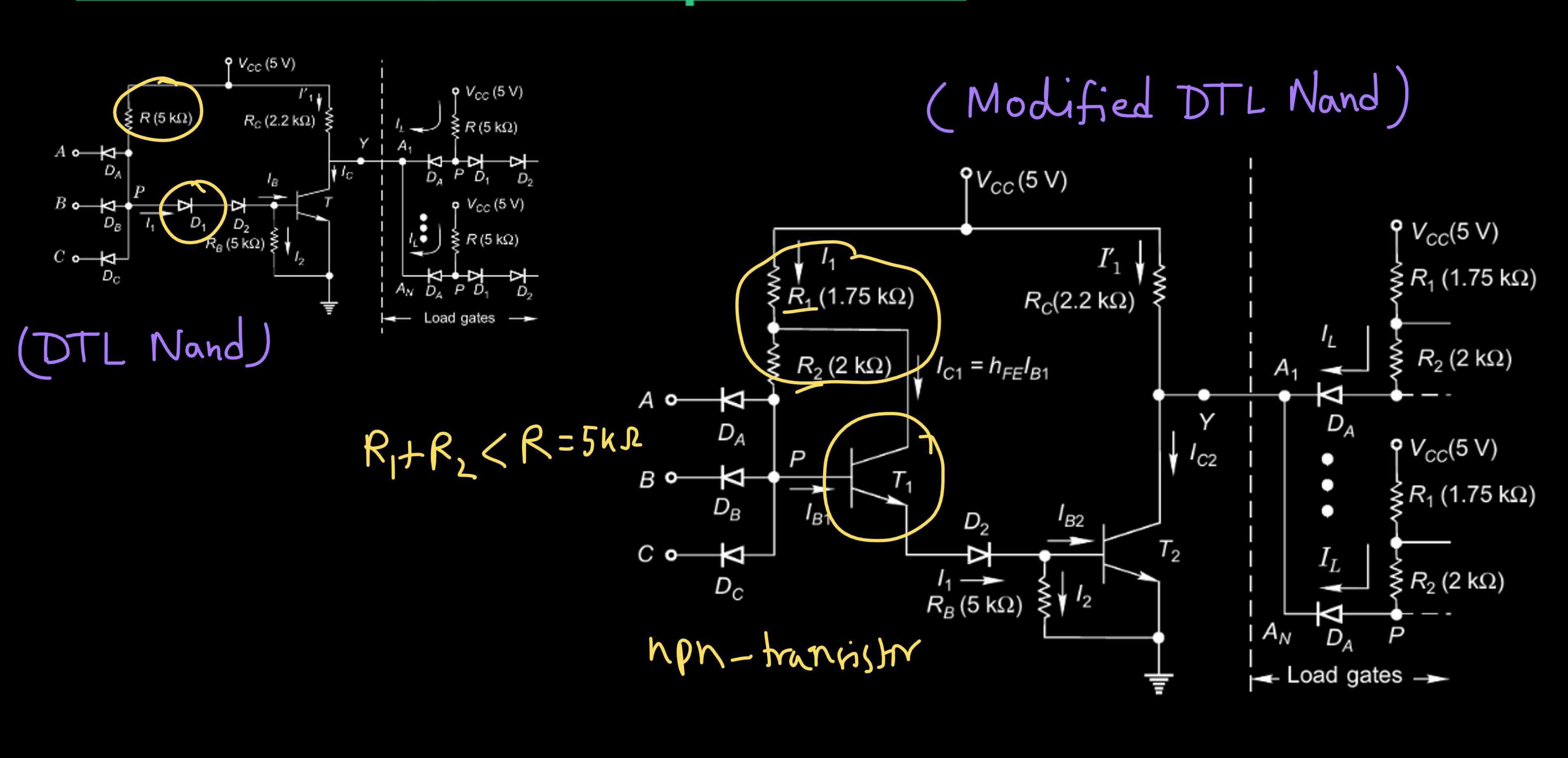
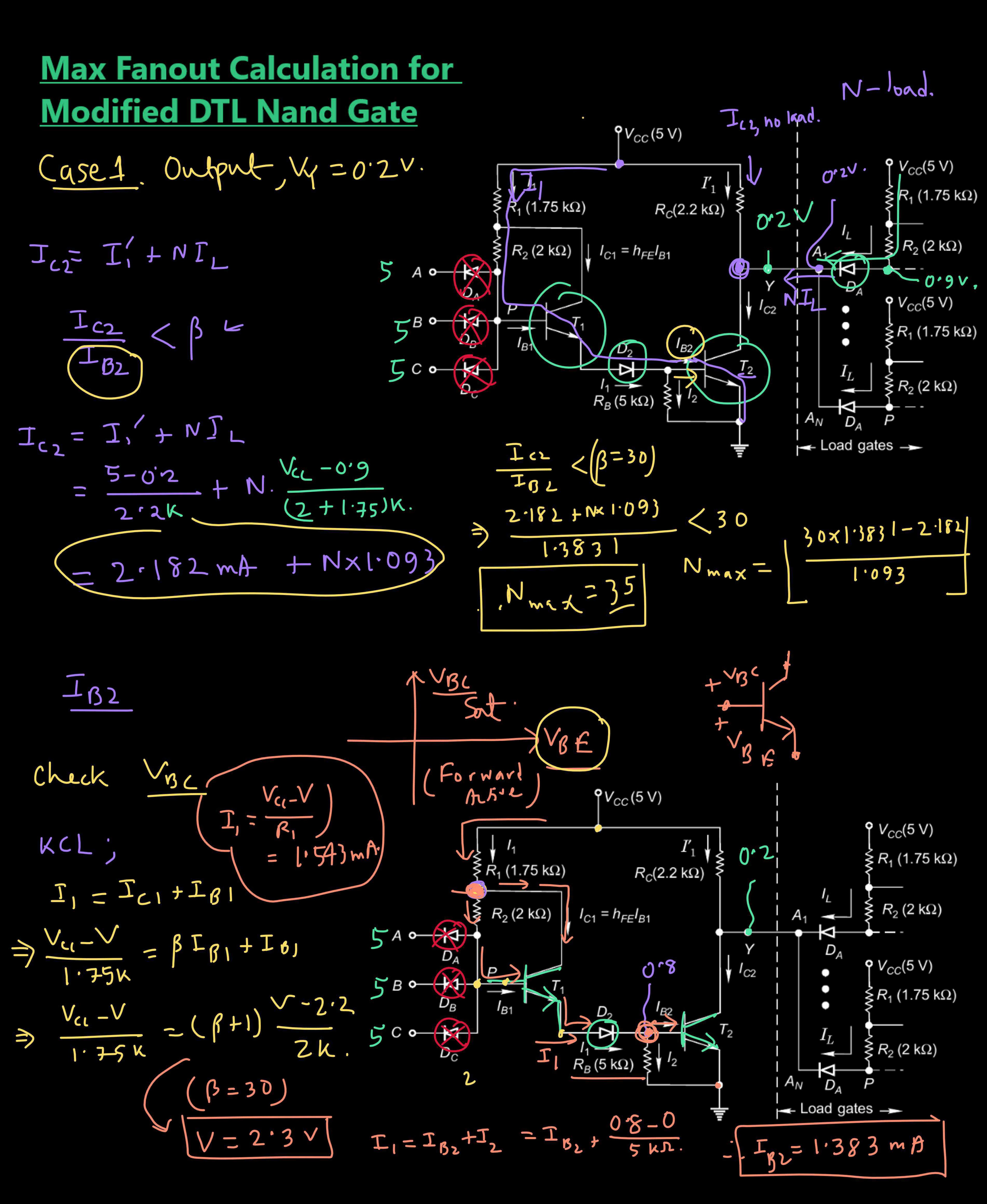
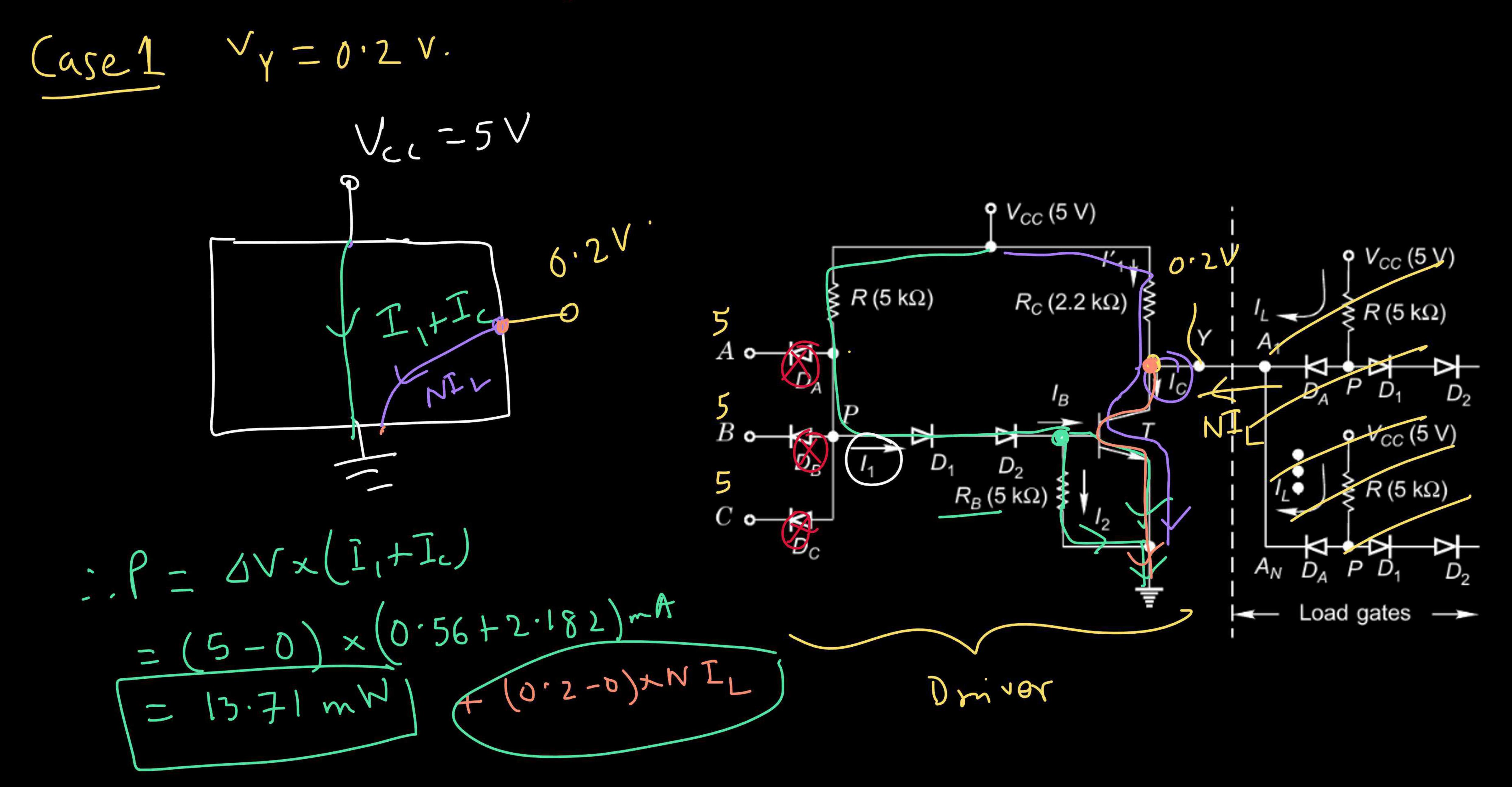
Modified DTL (Fanout Improvement)

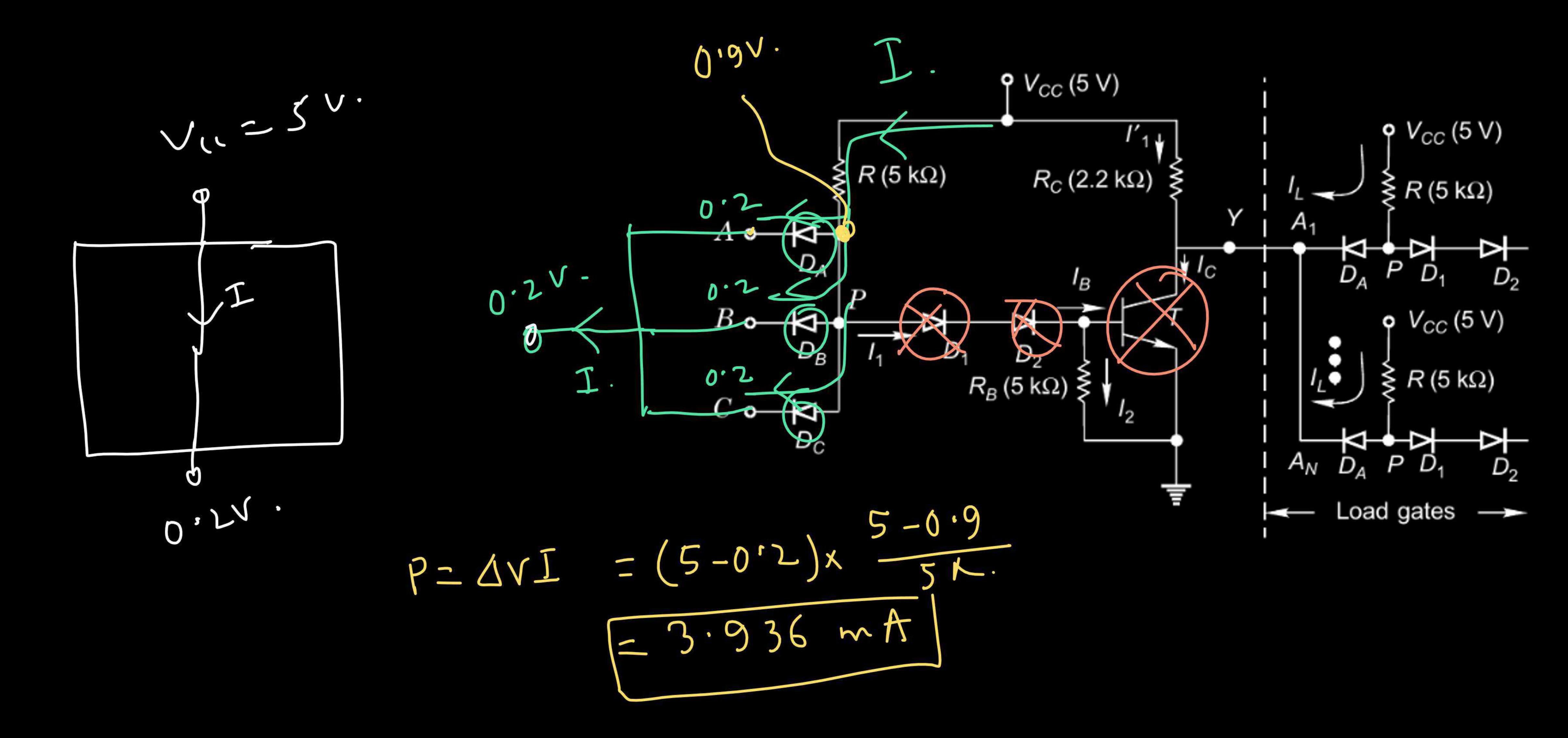




<u> Maximum Power Dissipation</u>



Caf2
$$V_{y} = 5 V$$
.



<u> High Threshold Logic (HTL)</u>

46.97

Q. If all the inputs are high, then what is magnitude of noise voltage at one of the input terminals which will cause the gate to malfunction? Assume no load connected to output.

