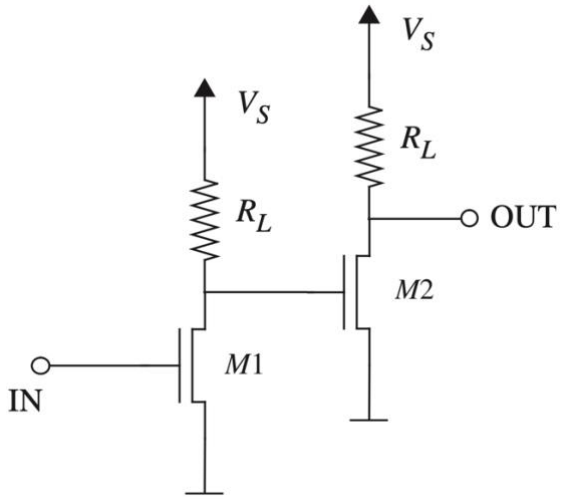
Problem 1 – Static Discipline [~2 pages]

For this problem, use the S-model of the MOSFET with $V_T = 2V$. Consider the following circuit with $V_S = 5V$ and $R_L = 2k\Omega$.



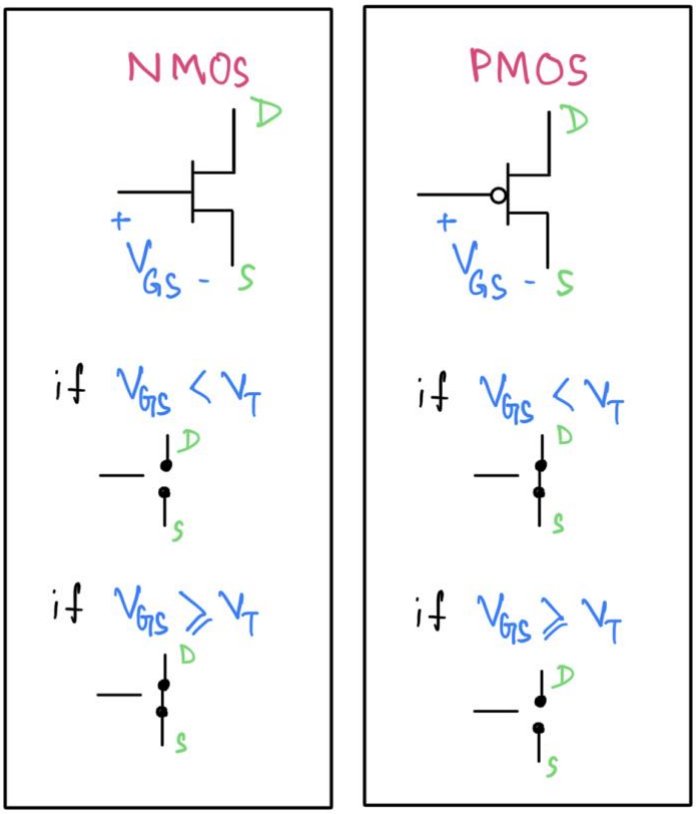
a. If $IN < 2V$, what will be the state and output of $M1$? Hence what would be the state of $M2$ and the voltage value of OUT?
b. If $IN \geq 2V$, what will be the state and output of $M1$? Hence what would be the state of $M2$ and the voltage value of OUT?
c. From the results of a. and b., what logical function does this circuit perform (NOT? Buffer? NAND? NOR?)
d. From the results of a. and b., draw the voltage transfer characteristics of the entire circuit, i.e., draw the $OUT\ vs\ IN$ graph.
e. Does the circuit satisfy the static discipline for the voltage thresholds $V_{OL} = 1V$, $V_{IL} = 1.5V$, $V_{OH} = 4V$ and $V_{IH} = 3V$? Why or why not?
[**Hint**: use graphical method as shown in lecture videos]
f. Does the circuit satisfy the static discipline if the V_{IL} specification was changed to $V_{IL} = 2.5V$? Why or why not?
[**Hint**: use graphical method as shown in lecture videos]
g. What is the *maximum* value of V_{IL} for which the circuit will (marginally) satisfy the static discipline? What is the NM_0 in this case?
h. What is the *minimum* value of V_{IH} for which the circuit will (marginally) satisfy the static discipline? What is the NM_1 in this case?

Problem 2 – CMOS Logic Gates [~1.5 pages]

Background

We have learned about NMOS and its S-model in the lectures. According to this model, the **NMOS** will be "OFF" (open circuit) if $V_{GS} < V_{Tn}$ (for example $V_{GS} = 0V$) and it will be "ON" (short circuit) if $V_{GS} \geq V_{Tn}$ (for example $V_{GS} = 5V$). Here, the threshold voltage V_{Tn} is positive for NMOS.

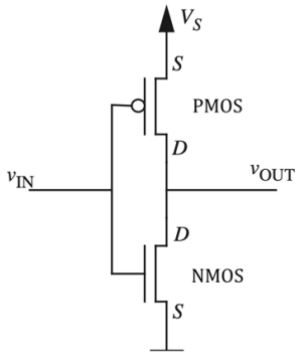
The other type of MOSFET, i.e., the **PMOS**, has a similar S-model, but the conditions are reversed. That is, the PMOS will be "OFF" (open circuit) if $V_{GS} \geq V_{Tp}$ (for example $V_{GS} = 0V$) and it will be "ON" (short circuit) if $V_{GS} < V_{Tp}$ (for example $V_{GS} = -5V$). The summary of the S-model for both NMOS and PMOS is given below. Unlike NMOS, the threshold voltage V_{Tp} for PMOS is negative.



Currently, the most popular technology used in computer chip design, including CPU and RAM, is called CMOS. **CMOS** stands for **C**omplementary **MOS**, and this technology takes advantage of a pair of PMOS and NMOS to build ICs with very low power consumption. In fact, CMOS circuits have almost zero static power consumption, they only require small amount of power to switch states.

Main Question Part 1

Consider the following CMOS circuit. Assume $V_S = 5V$, $V_{Tn} = 1V$ for the NMOS, and $V_{Tp} = -1V$ for the PMOS. Notice how the Drain and the Source of the PMOS are connected. **Use the S-model for both NMOS and PMOS for the rest of the question**.



a. If $V_{IN} = 0V$, what is the value of V_{GS} for the NMOS? What is the value of V_{GS} for the PMOS? Hence, what are the states (ON/OFF) of the NMOS and the PMOS? Therefore, what is the value of the output voltage V_{OUT}?
[**Hint**: Will the node V_{OUT} get shorted to ground or V_S in this case?]

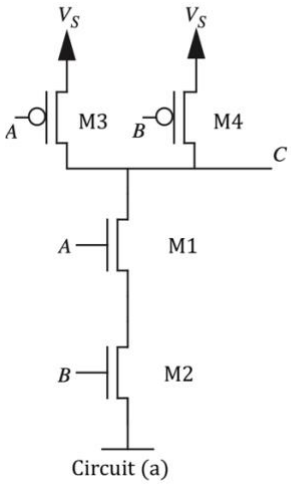
b. If $V_{IN} = 5V$, what is the value of V_{GS} for the NMOS? What is the value of V_{GS} for the PMOS? Hence, what are the states (ON/OFF) of the NMOS and the PMOS? Therefore, what is the value of the output voltage V_{OUT}?
[**Hint**: Will the node V_{OUT} get shorted to ground or V_S in this case?]

c. Considering **0V as logical 0** and **5V as logical 1**, What logical operation does this circuit perform? Write down the Boolean truth table of $IN\ vs\ OUT$.

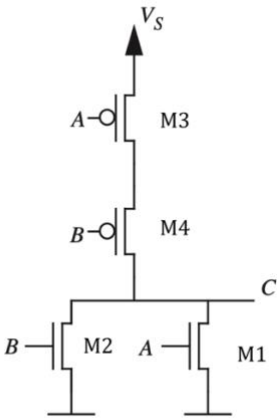
Main Question Part 2

$V_A(V)$	$A(0/1)$	$V_B(V)$	$B(0/1)$	$State_{M1}$	$State_{M2}$	$State_{M3}$	$State_{M4}$	$V_C(V)$	$C(0/1)$
$0\ V$	0	$0\ V$	0						
$0\ V$	0	$5\ V$	1						
$5\ V$	1	$0\ V$	0						
$5\ V$	1	$5\ V$	1						

Fill out the above table twice, once for each of the following circuits. Here assume $V_S = 5V$. Note that if the input voltage 5V, you can consider an NMOS to be ON and a PMOS to be OFF. On the other hand, if the input voltage is 0V, consider the NMOS to be OFF an the PMOS to be ON. What logic function does Circuit (a) perform? What about Circuit (b)?



Circuit (a)



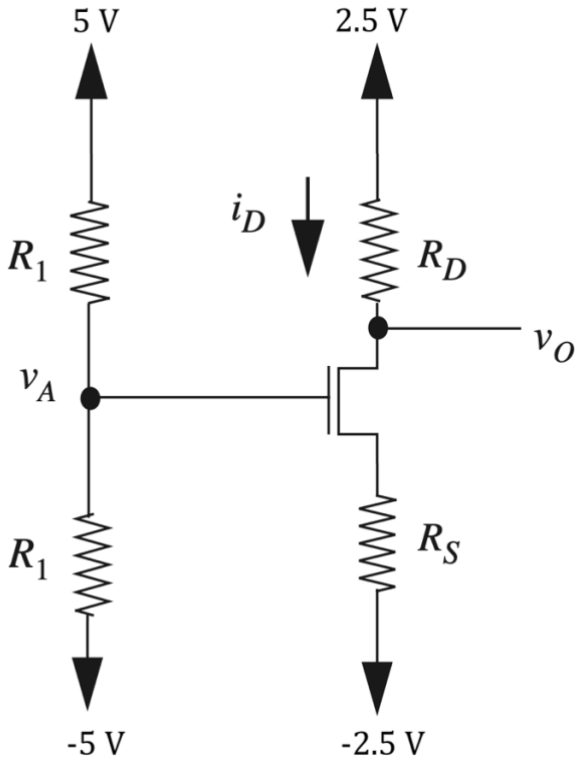
Circuit (b)

Hint: The first row of the table for **Circuit (a)** is done for you. The node C will be shorted to V_S in this case.

$V_A(V)$	$A(0/1)$	$V_B(V)$	$B(0/1)$	$State_{M1}$	$State_{M2}$	$State_{M3}$	$State_{M4}$	$V_C(V)$	$C(0/1)$
$0\ V$	0	$0\ V$	0	OFF	OFF	ON	ON	$5\ V$	1

Problem 3 – Method of Assumed State for MOSFET [~2 pages]

Design the following circuit in such a way that the MOSFET operates at a drain current, i_D, of $0.5\ mA$ and $v_o = 0.5V$. That is, find the value of R_D and R_S. Here, $V_T = 0.7V$, $K = 2\frac{mA}{V^2}$, and $R_1 = 10\ k\Omega$. Note that you MUST verify your assumption! **Use real MOSFET equations**.

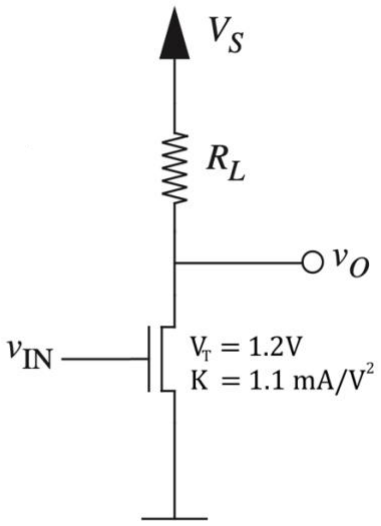


Hint: Here are some questions that will guide you to the solution:

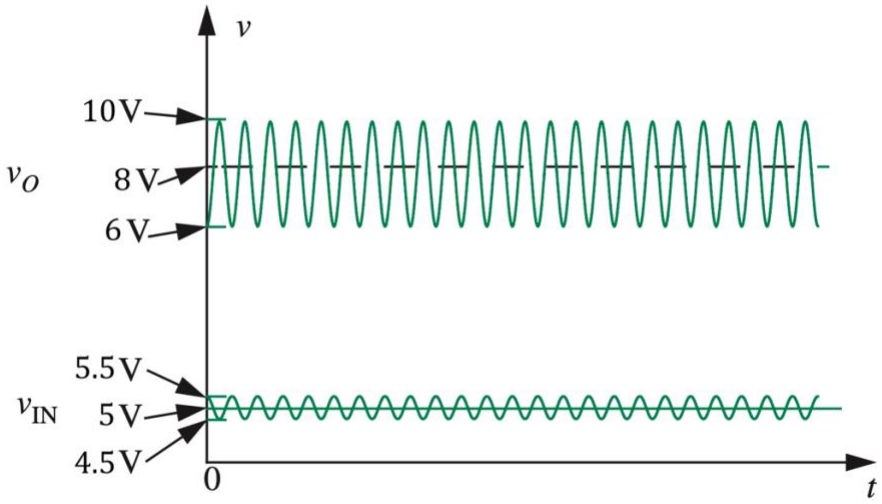
1. What is the value of the voltage v_A? [Hint: Week 1, Lecture 1, Part 3, Last 4 minutes]
2. What is the gate voltage V_G? [Hint: The gate is shorted to ….]
3. The value of i_D is given, and you know the voltage of the two terminals of R_D. What is the equation relating i_D, $v_o = 0.5V$, and $2.5V$?
4. Assume the MOSFET is in one of the states. Which one should you start with?
5. From the equation of i_D for the state you assumed, find the value of V_S.
   [Hint: $V_{GS} = V_G - V_S$ and $V_{DS} = V_D - V_S$. What's the value of V_G? What about V_D?
6. Is your assumption correct? Why or why not? If not, go back to step 4 and repeat for another assumption.
7. Now you know the voltage of the two nodes of R_S and the current through it. Find R_S.

Problem 4 – MOSFET Amplifier [~1 page]

Consider the following small signal MOSFET amplifier circuit.



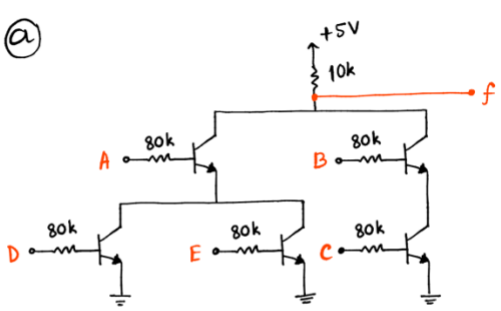
The input voltage is given as $V_{IN} = V_{GS} = X + v_i(t) = 5V + v_i(t)$ and output voltage is given as $v_O = Y + Av_i(t) = 8 + v_i(t)$. Here, $v_i(t)$ is a sinusoidal voltage with amplitude a, X is the input DC voltage, Y is the output DC voltage. The input and output waveforms are given below. Notice the output small signal is inverted compared to input small signal. Hence, the small signal gain, A, will be negative.

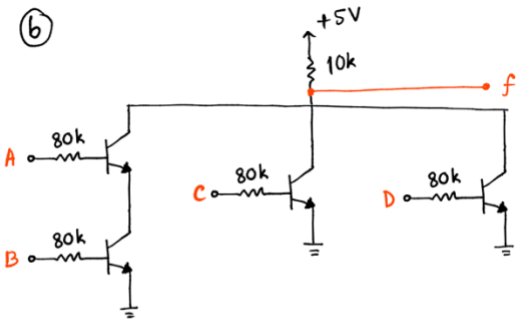


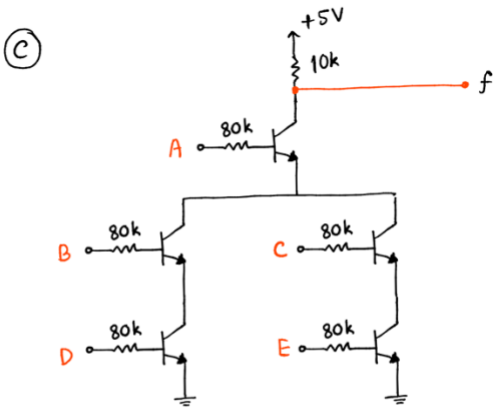
a. From the above graph, what is the amplitude of the input small signal $v_i(t)$?
b. From the above graph, what is the amplitude of the output small signal?
c. Hence, what is the small signal gain A? (Note: A should be negative)
d. From the above graph, what is the value of input DC voltage X and the output DC voltage Y?
e. Design the circuit, i.e., find the value of V_S and R_L to achieve given input-output voltage relation and the given small signal amplification.
   [Hint: See Week 8, Lecture 2 - Part 6 and Pop Quiz 2. Work backward from A and Y to find R_L and V_S]

Problem 5 – BJT Logic Gates [~0.5 page]

Find the logic functions f as function of the Boolean inputs A, B, C, D, and E for the following three BJT circuits. **Use the S-model for the BJT**.

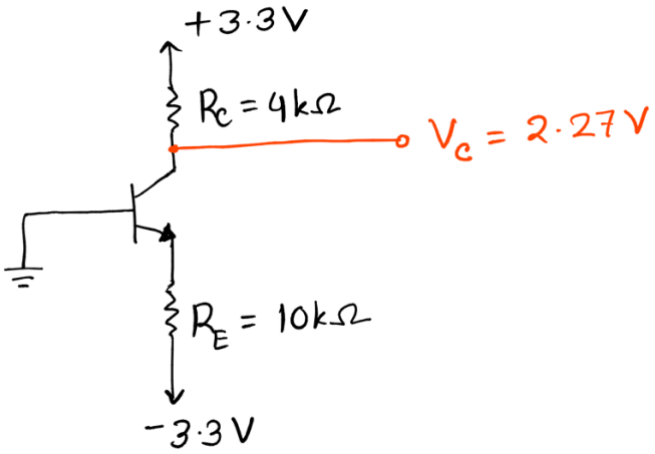






Problem 6 – Method of Assumed State for BJT [~2 pages]

For the following BJT, $V_{BE\ (active)} = 0.7\ V, V_{BE\ (saturation)} = 0.8\ V$, and $V_{CE\ (saturation)} = 0.2\ V$.



Use method of assumed state to find the following (note that you MUST verify your assumption):

(i) I_C
(ii) I_E
(iii) I_B
(iv) β
(v) α

[**Hint**: See the solved problems in the handout of Week 9 Lecture 2]