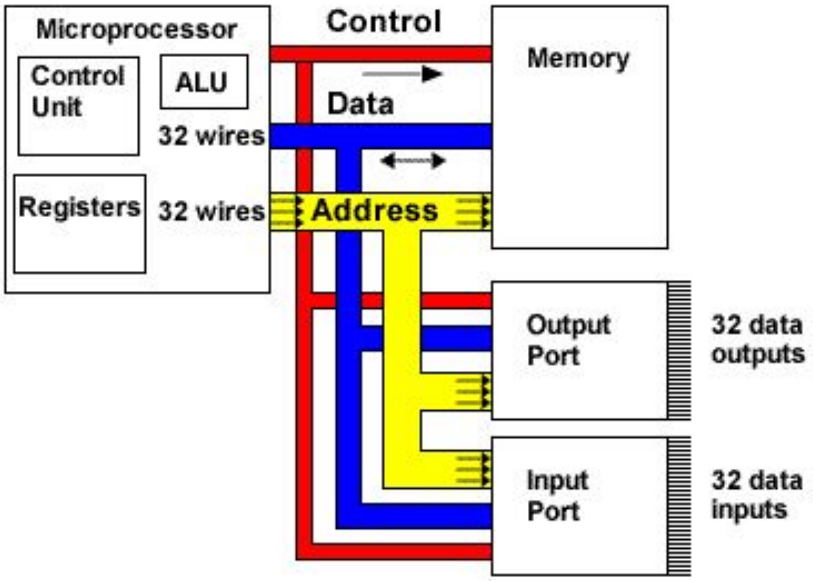
CSE360-Computer Interfacing
BRAC University



Bus Interfacing

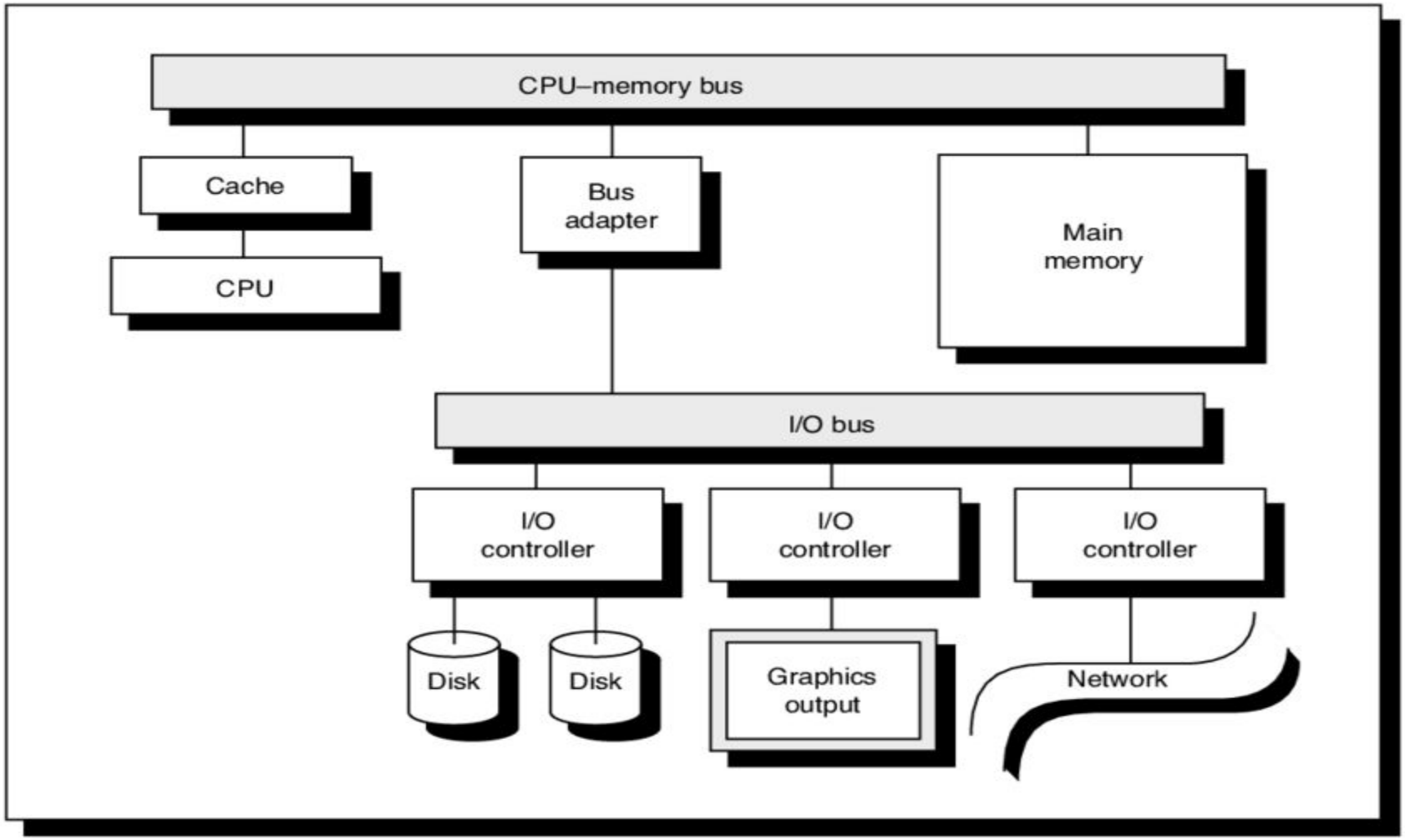
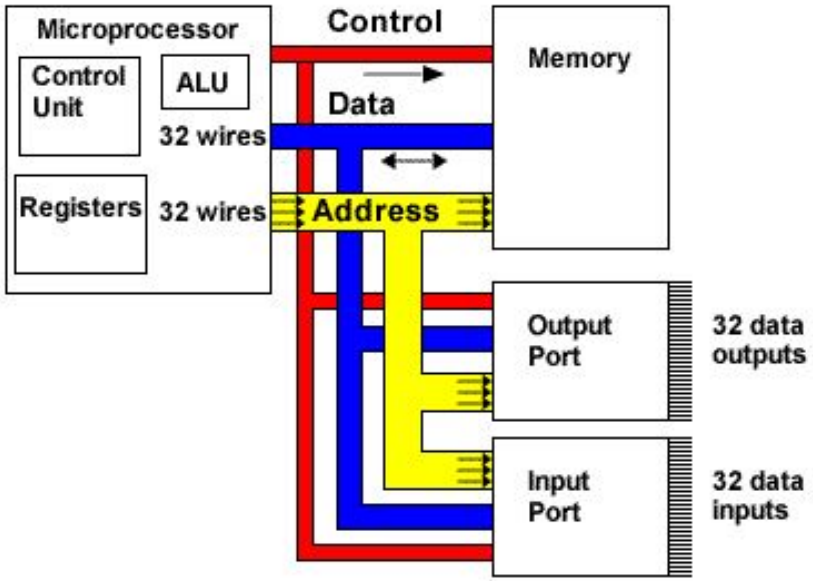


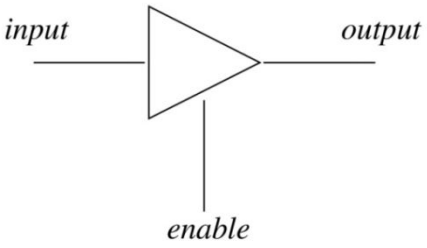
Figure: Different components interfaces with shared bus line

Tri- state Bus

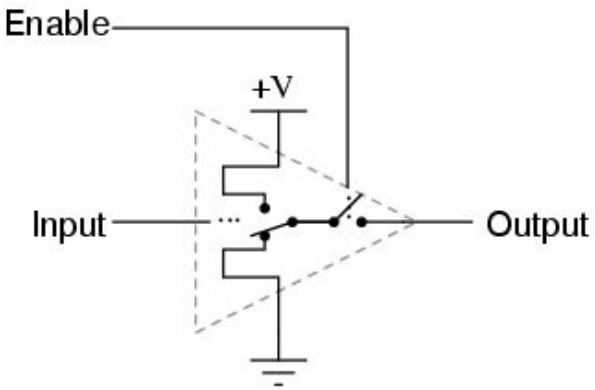
Buses and Tri-state Logic



enable	input	output
0	X	Z
1	0	0
1	1	1

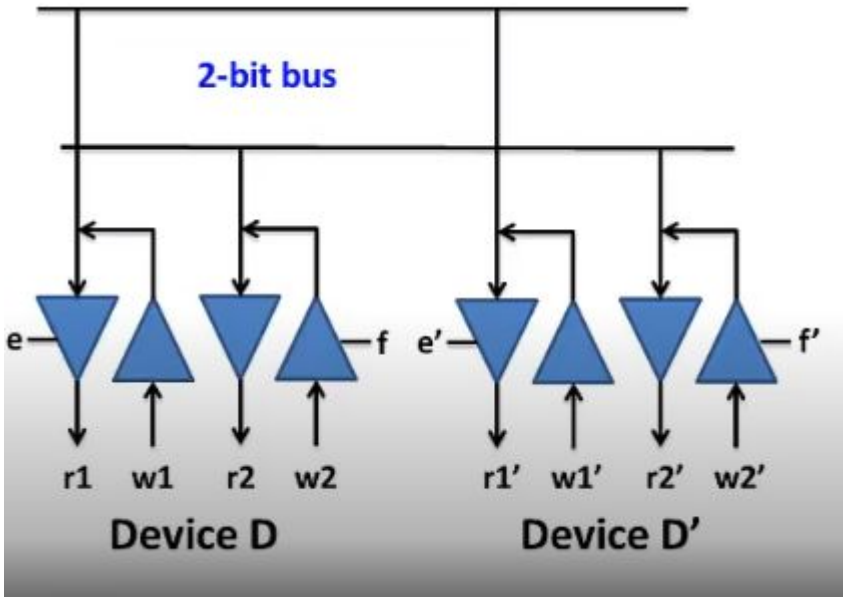


Tristate buffer gate



- In Tri-state, only one device can access the bus at anyone time.
- The basic concept of the third state, high impedance (Hi-Z), is to effectively remove the device's influence from the rest of the circuit.

How Tri-Stating works



- D is writing to D'
  - e=0, f=1, e'=1, f'=0
- D' is writing to D
  - e=1, f=0, e'=0, f'=1
- e=f=0 → D is tri-stated
  - D is disconnected from bus

Image and content credit goes to - https://www.youtube.com/channel/UCtaUBoxL2DvNydL3r5KuOOg

Advantages of Tri-State Bus

- To resolve conflict between multiple sources driving the shared bus line.
- To use the same port as both for input and output operation.

  Note: not all devices need to drive all bus lines.
- It higher the bus fan out.

External Bus Interface

- An external bus is a type of data bus that enables external devices and components to connect with a computer.
- It enables connecting devices, carrying data and other control information, but is only restricted to be used external to the computer system.
- An external bus is also known as external bus interface (EBI) and expansion bus.
- These devices can include storage, monitors, keyboard, mouse and more.

External Bus Interface

- Slower than internal buses.
- An external bus can be both serial or parallel.
- Universal Serial Bus (USB) , PCI bus and IEEE 1294 are common examples of external buses.

Bus Interfacing

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Bus Master:

The device that determines who will speak and who will listen is called the **bus master**.

- Usually, the CPU is the bus master, but some clever buses can allow other devices to take over when necessary.
- Input and output are always designated relative to the bus master.
- A **READ** means data is going into the bus master.
- A **WRITE** means that data is going out from the bus master.

***Each bus has several lines dedicated to one of three separate duties.

Bus Interfacing

- **Each bus has several lines dedicated to one of three separate duties.**

  - **Control lines** are (mostly) unidirectional. They coordinate data transfer.
  - **Address lines** are unidirectional. The bus master uses them to designate which device it wants to communicate with.
  - **Data lines** are bidirectional so that they can carry binary data into or out from the bus master.

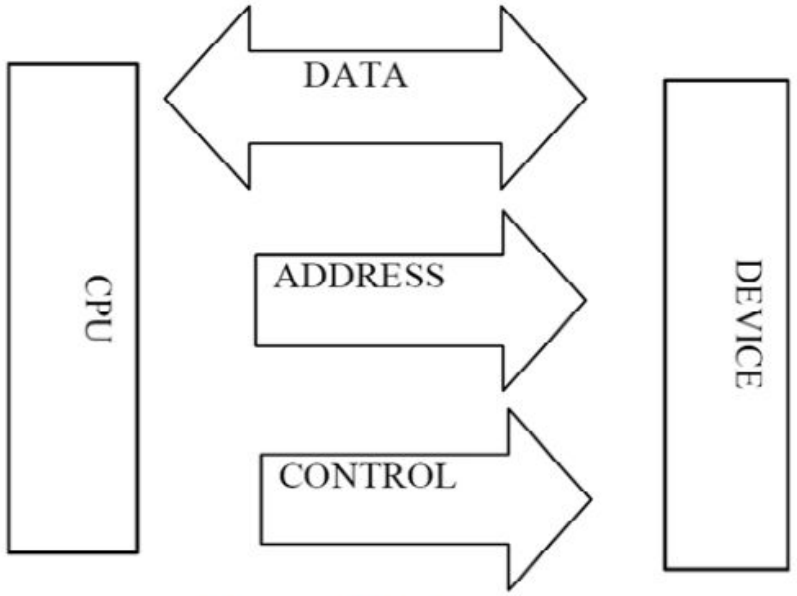

Figure : The bus.

Bus Interfacing

Bus Errors/Conflict

Only one I/O device is allowed to share a bus at any one time as OUTPUT.
If two or more I/O use the bus as OUTPUT causes bus conflict.
If one I/O is used as OUTPUT and multiple I/O are used as INPUT causes NO bus error.

Causes of Bus Error:

1. Caused by multiple device using the bus as Output
2. Wait states are not maintained
3. If an I/O device causes the bus pin to stuck at 1 or 0.
4. Caused by glitch.

Causes of Bus Error

Wait State: A time-out period during which a **CPU** or bus lies idle. **Wait states** are sometimes required because different components function at different clock speeds.
For example, if the **CPU** is much faster than the memory chips, it may need to sit idle during some clock cycles so that the memory chips can catch up.
If wait states are not maintained properly, there will be no synchronization in bus line and it will occur bus error.

Glitch: A **glitch** is a short-lived fault **in a** system. It is often used to describe a transient fault that corrects itself, and is therefore difficult to troubleshoot.
Example: Effects of glitches on the data line which can cause an I^2C bus (or SMBus) interface to invalidate a detected I^2C start command or to erroneously detect an I^2C start command, which occurs when the data signal transitions from a logic high to a logic low while the clock signal has a logic high, are reduced by detecting the logic state of the data signal when the clock signal next transitions from a logic high to a logic low.

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The End