# CSE460: VLSI Design

Lecture 11 + 12

# CMOS Transistor Theory

# Contents

# Introduction

So far, we have treated transistors as ideal switches

An ON transistor passes a finite amount of current

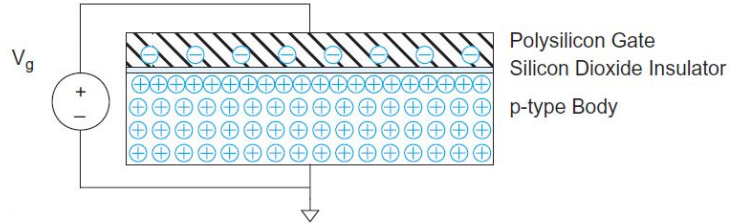
- Depends on terminal voltages
- Derive current-voltage (I-V) relationships

Transistor gate, source, drain all have capacitance

- $I = C (\Delta V/\Delta t) \rightarrow \Delta t = (C/I) \Delta V$
- Capacitance and current determine speed

# MOS Capacitor

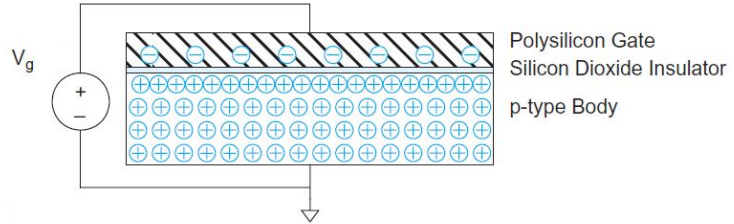
- The MOS transistor is a majority-carrier device
- Current in a conducting channel between the source and drain is controlled by a voltage applied to the gate
  - nMOS majority carriers are electrons
  - pMOS majority carriers are holes
- First, let's examine an isolated MOS structure (of an nMOS)  with a gate and body, but no source or drain



# MOS Capacitor: Operating Modes

MOS Structure

- Top layer: Gate
  - A Good conductor, metal or polysilicon
- Middle layer: Oxide
  - Silicon dioxide, good insulator
- Bottom layer: Silicon (doped)
  - nMOS: p-type, pMOS: n-type




Lets ground the body, connect a voltage source ***Vg*** between the gate and body

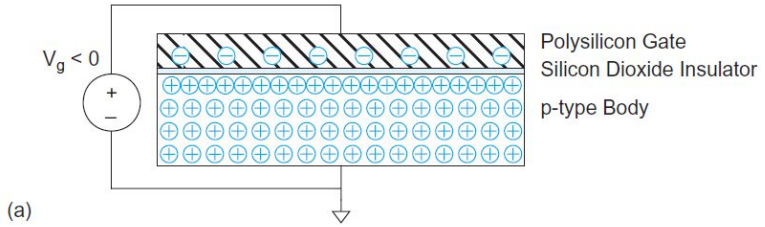
Value of ***Vg*** decides one of three MOS operating modes: (a) Accumulation, (b) Depletion & (c) Inversion

# MOS Capacitor: Accumulation Mode

Case (a): ***Vg < 0***

- a negative voltage is applied to the gate
- there is negative charge on the gate
- The mobile positively charged holes are attracted to the region beneath the gate

This is called the ***accumulation*** mode

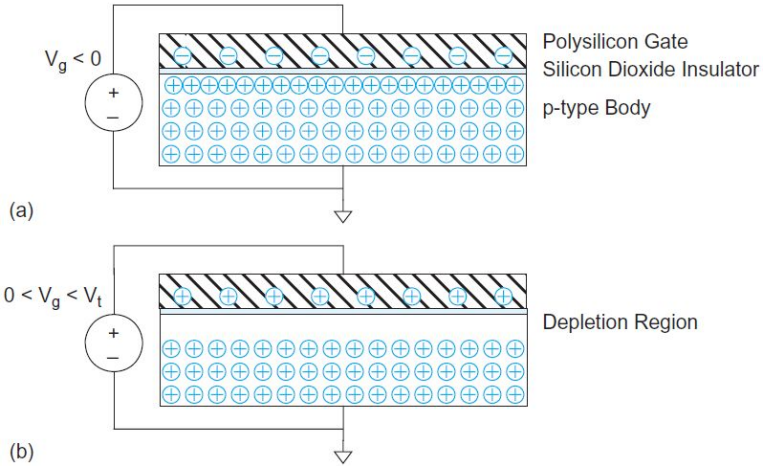


# MOS Capacitor: Depletion Mode

Case (b): **0 < *Vg* < *Vt***

- a small positive voltage is applied to the gate
- resulting in some positive charge on the gate
- The holes in the body are repelled from the region directly beneath the gate, resulting in a *depletion* region forming below the gate

This is called the ***depletion*** mode

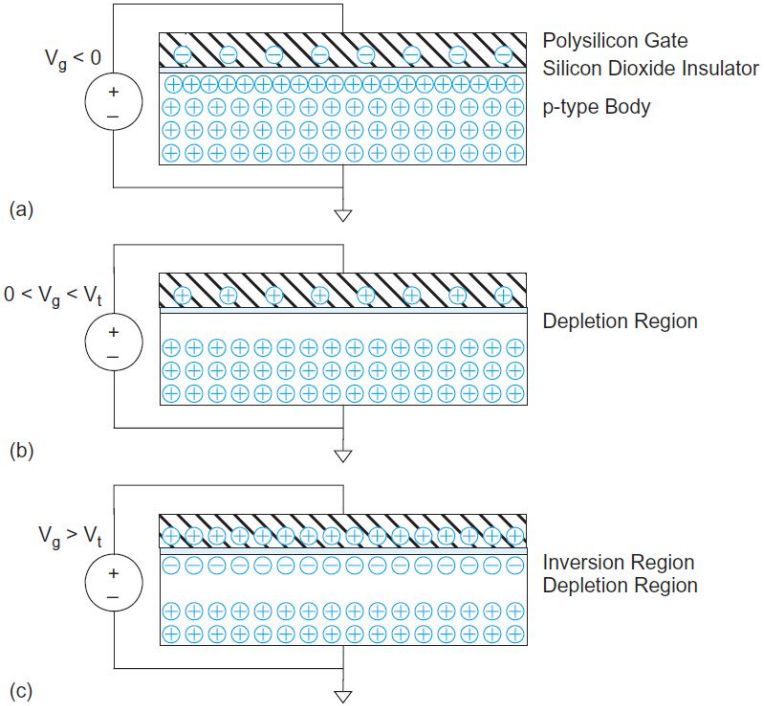


# MOS Capacitor: Inversion Mode

Case (c): ***Vg > Vt***

- a higher positive potential exceeding a critical threshold voltage Vt is applied
- more positive charge at the gate
- the holes are repelled further
- some free electrons in the body are attracted to the region beneath the gate
- this conductive layer of electrons in the p-type body is called the *inversion* layer

This is called the ***inversion*** mode



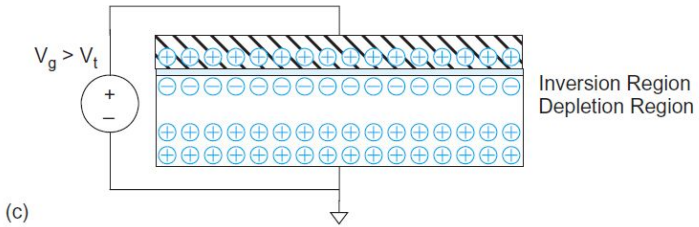
# MOS Capacitor: Inversion Mode

Observation

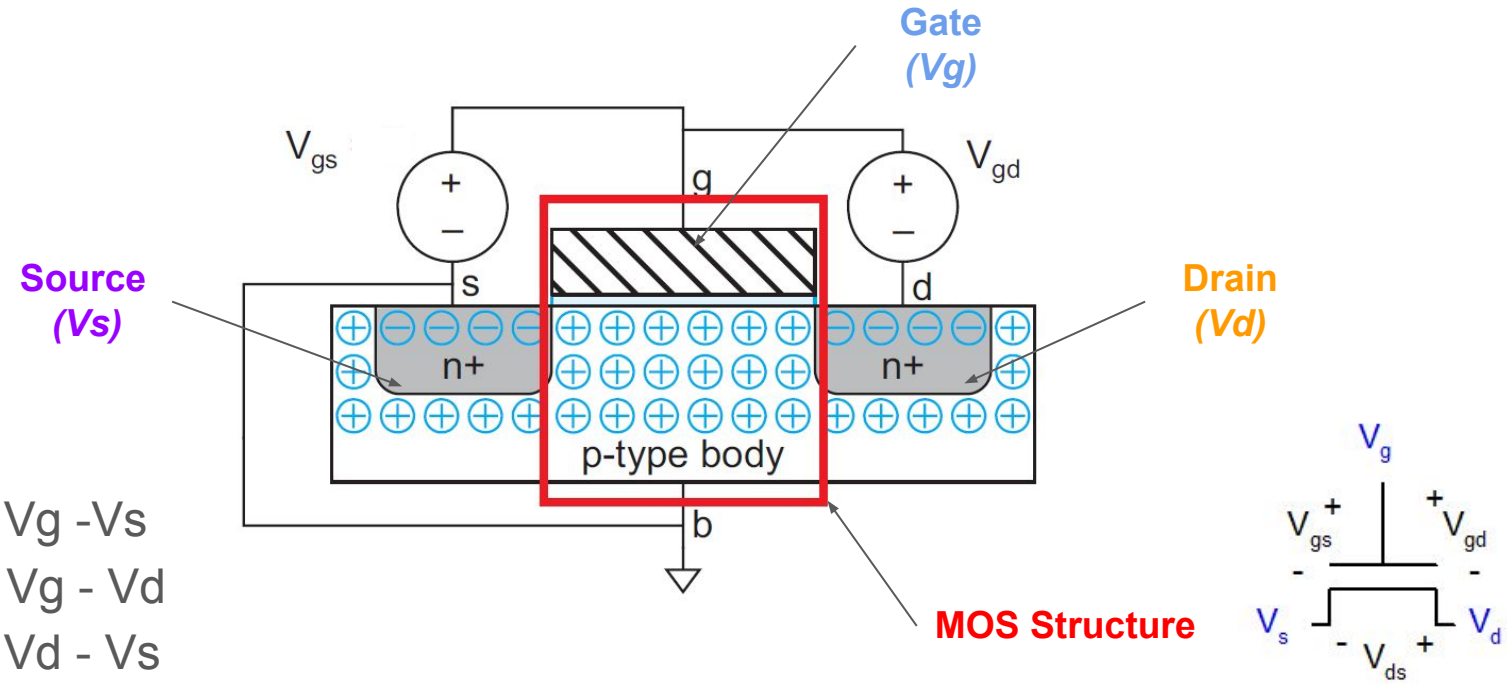
- To conduct current we need a channel between source and drain
- An inversion channel is formed only in the inversion mode when ***Vg > Vt***
- ***Vt*** is called threshold voltage (***Vt > 0***)

Channel exists in **Inversion mode** (***Vg > Vt*** )

No channel exists in **Accumulation or Depletion mode** (***Vg < Vt*** )



# nMOS Transistor




Voltages:

1. Vgs = Vg -Vs
2. Vgd = Vg - Vd
3. Vds = Vd - Vs

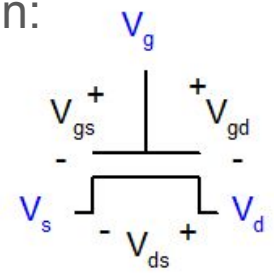
# nMOS Transistor

The gate voltage ***Vg*** merely sets up the conduction path (inversion layer) in the body of the transistor underneath the gate, i.e. it is now ready to conduct current if a voltage is set up across the conducting path, between the source and drain.

The nMOS mode of operation hence depends on all three terminal voltages & the threshold voltage of the transistor: ***Vg, Vd, Vs & Vt***

The source and drain are symmetric diffusion terminals. By convention:

- **nMOS** source is at lower voltage than drain while conducting
- Or, ***Vd ≥ Vs ⇒ Vd - Vs ≥ 0 ⇒ Vds ≥ 0***
- nMOS body is grounded



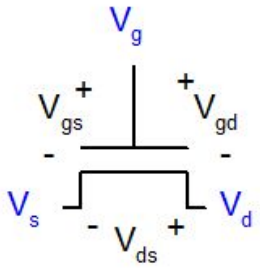
# nMOS Transistor: Operating Regions

Depending on the terminal voltage and their differences, nMOS transistor could be operating in on of the following 3 regions:

1. **Cutoff** (No current flows)
2. **Linear** (Current flows & is *proportional* to the applied voltage)
3. **Saturation** (Current flows & is *independent* of the applied voltage)

We will develop the I-V characteristics for an nMOS transistor

Similar result can be obtained from analysis of a pMOS transistor.



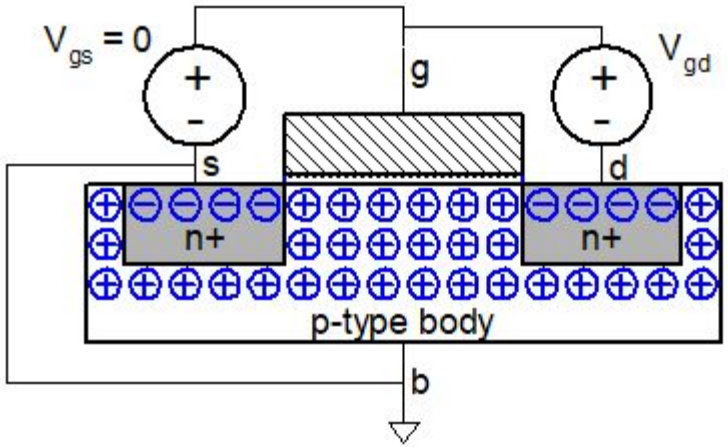
# nMOS Transistor: Cutoff

Conditions:

- ***Vgs < Vt***
- ***Vds*** (doesn't matter)

Results:

- No channel, hence no current
- $I_{ds} \approx 0$ independent of ***Vds***



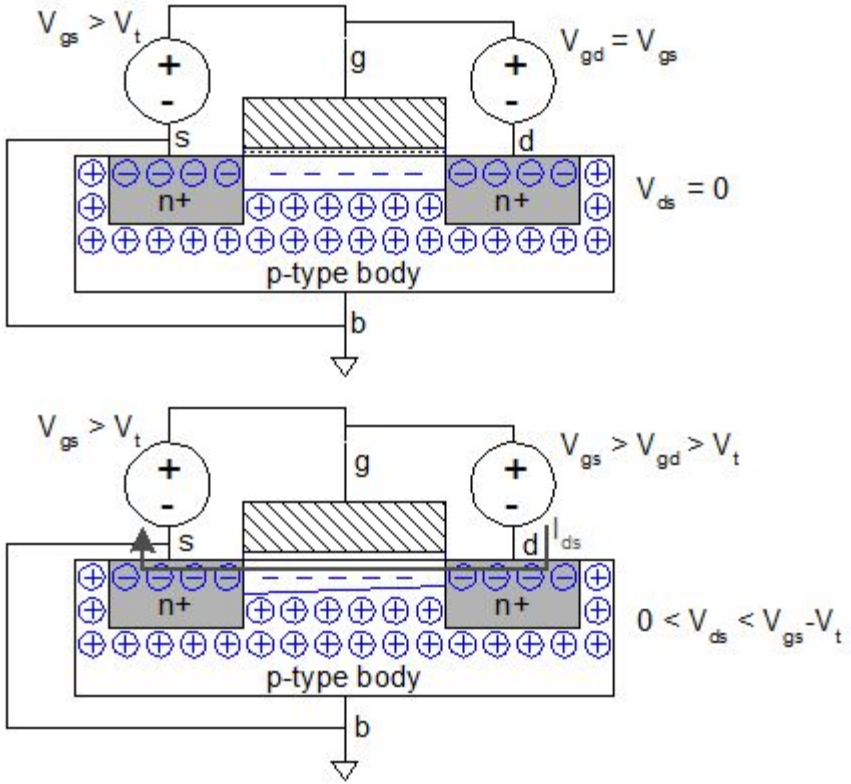
# nMOS Transistor: Linear

Conditions:

- ***Vgs > Vt***
- ***0 ≤ Vds < Vgs - Vt***

Results:

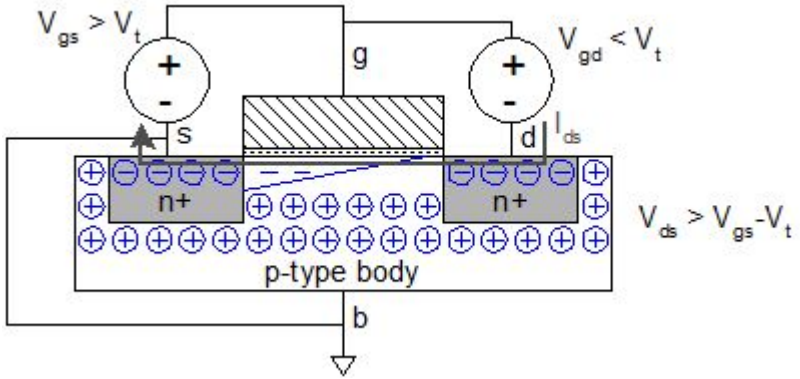
- Channel forms hence current flows
- $I_{ds} > 0$
- $I_{ds}$ increases with ***Vds***
- Similar to a linear resistor



# nMOS Transistor: Saturation

Conditions:

- ***Vgs ≥ Vt***
- ***Vds ≥ Vgs - Vt***




Results:

- Channel forms, hence current flows
- $I_{ds} > 0$
- But channel is pinched off near the drain terminal, $I_{ds}$ saturates
- Ids is independent of ***Vds***
- Similar to a current source

# nMOS Transistor Operating Regions: Summary

***Vt***: nMOS threshold voltage, ***Vt > 0*** (nMOS device property)

***Vgs***: gate to source voltage, ***Vgs = Vg - Vs***

***Vds***: drain to source voltage, ***Vds = Vd - Vs***

| | Vgs < Vt | Vgs ≥ Vt |
|---|---|---|
| 0 < Vds < Vds(sat) | Cutoff | Linear |
| Vds ≥ Vds(sat) | Cutoff | Saturation |

# nMOS Transistor: I-V Summary

$$I_{ds} = \begin{cases} 0 & \text{if } V_{gs} < V_t \text{ (Cutoff)} \\ \beta(V_{gs} - V_t - \frac{V_{ds}}{2})V_{ds} & \text{if } V_{ds} < V_{ds(sat)} \text{ (Linear)} \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & \text{if } V_{ds} \geq V_{ds(sat)} \text{ (Saturation)} \end{cases}$$

Where $\beta = \mu_n C_{ox} W/L$ & $V_{ds(sat)} = V_{gs} - V_t$

# pMOS Transistor Operating Regions: Summary

***Vtp***: pMOS threshold voltage, ***Vtp < 0*** (pMOS device property)

***Vsg***: source to gate voltage, ***Vsg = Vs - Vg***

***Vsd***: source to drain voltage, ***Vsd = Vs - Vd***

| | Vsg < \|Vtp\| | Vsg ≥ \|Vtp\| |
|---|---|---|
| 0 < Vsd < Vsd(sat) | Cutoff | Linear |
| Vsd ≥ Vsd(sat) | Cutoff | Saturation |

# pMOS Transistor: I-V Summary

$$I_{sd} = \begin{cases} 0 & \text{if } V_{sg} < |V_{tp}| \text{ (Cutoff)} \\ \beta_p(V_{sg} - |V_{tp}| - \frac{V_{sd}}{2})V_{sd} & \text{if } V_{sd} < V_{sd(sat)} \text{ (Linear)} \\ \frac{\beta_p}{2}(V_{sg} - |V_{tp}|)^2 & \text{if } V_{sd} \geq V_{sd(sat)} \text{ (Saturation)} \end{cases}$$

Where $\beta_p = \mu_p C_{ox} W/L$ & $V_{sd(sat)} = V_{sg} - |V_{tp}|$

# MOSFET Capacitance

Any two conductors separated by an insulator have capacitance

Gate to channel capacitor is very important (***gate capacitance:*** $C_g$)

- Creates channel charge necessary for operation

Source and drain have capacitance to body (***diffusion capacitance:*** $C_{sb}$, $C_{db}$)

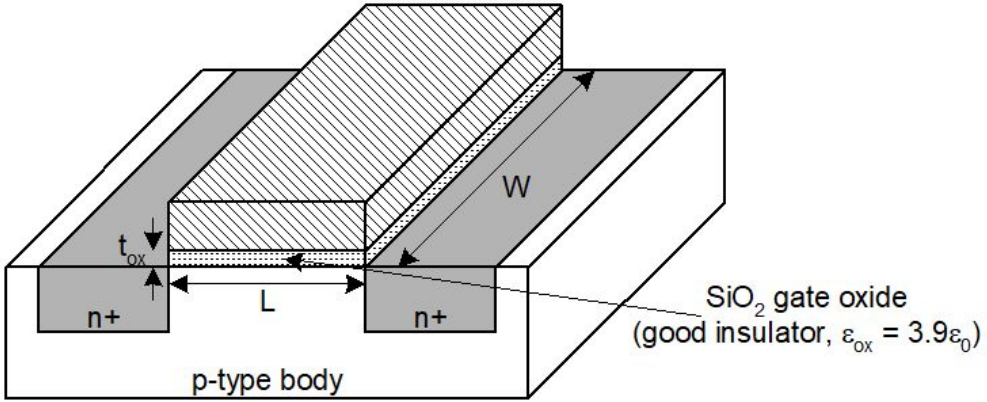
- Across reverse-biased diodes
- Called diffusion capacitance because it is associated with source/drain diffusion
- Remember that nMOS body is connected to ground and pMOS body is connected to supply (Vdd)

# Gate Capacitance

$C_g$ = Gate capacitance

$C_g = \varepsilon_{ox} WL/t_{ox} = C_{ox} WL = C_{permicron} W$

$C_{permicron}$ is typically about 2 fF/mm



# Diffusion Capacitance

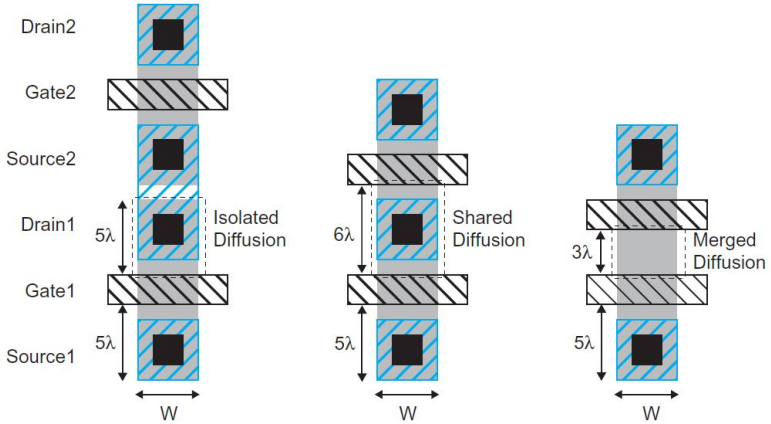
$C_{sb}$ = Source to body capacitance

$C_{db}$ = Drain to body capacitance

Undesirable, called parasitic capacitance

Capacitance depends on area and perimeter

- Use small diffusion nodes
- Comparable to $C_g$ for contacted diff
- ½ $C_g$ for uncontacted
- Varies with process



Thank You!