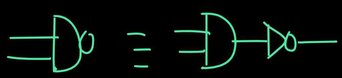
Diode Transistor Logic (DTL)



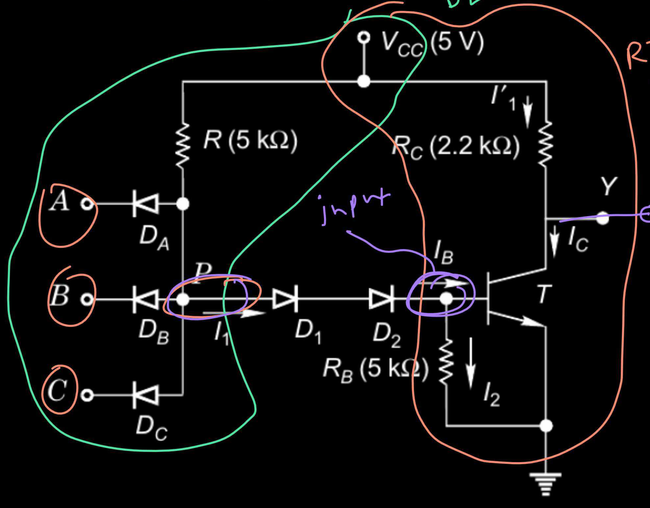
NAND Gate Truth Table

A	B	C	Y
LOW	LOW	LOW	HIGH
LOW	LOW	HIGH	HIGH
LOW	HIGH	LOW	HIGH
LOW	HIGH	HIGH	HIGH
HIGH	LOW	LOW	HIGH
HIGH	LOW	HIGH	HIGH
HIGH	HIGH	LOW	HIGH
HIGH	HIGH	HIGH	LOW

DTL NAND gate

DL AND

RTL inverter.



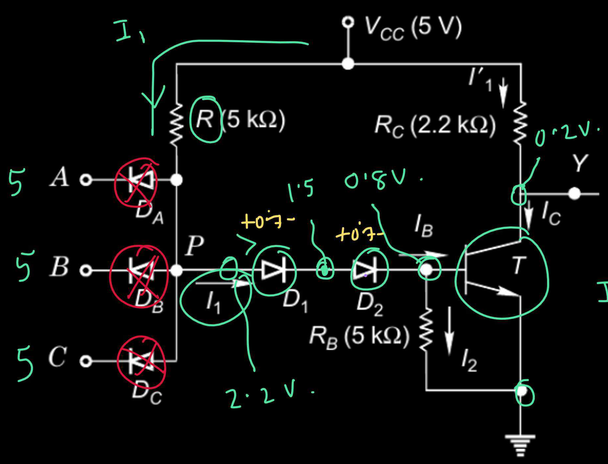
Basic operation for different input combination

V(High) = 5V, V(LOW) = 0·2V.

Saturation

$V_{BE} = 0{\cdot}8\,V$, $V_E = 0$. $V_B = 0{\cdot}8$

$V_{CE} = 0{\cdot}2$.

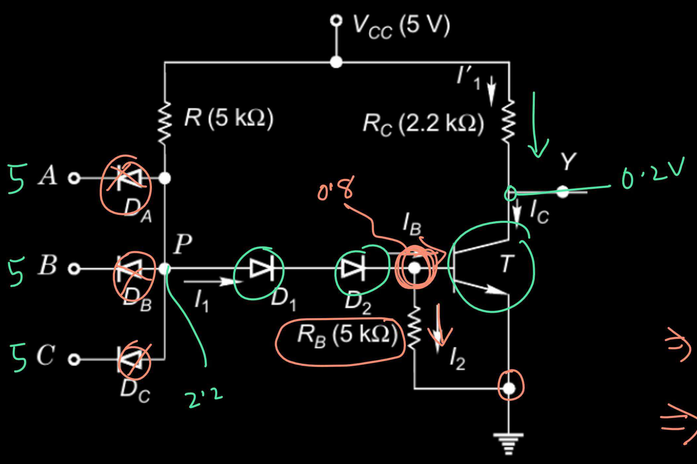


$$I_1 = \frac{V_{CC} - V_P}{R}$$

$$= 0{\cdot}56\ mA$$

Input	V_P	V_Y
At least one input is LOW	0·9	5
All the inputs are HIGH	2·2	0·2

β_{min} calculation



$$I_C = \frac{V_{CC} - V_Y}{R_C}$$

$$= 2{\cdot}182\ mA.$$

KCL;

$$I_1 = I_B + I_2$$

$$\Rightarrow 0{\cdot}56 = I_B + \frac{0{\cdot}8 - 0}{R_B}$$

$$\Rightarrow I_B = 0{\cdot}4\ mA.$$

$$\frac{I_C}{I_B} < \beta \Rightarrow \frac{2{\cdot}182}{0{\cdot}4} < \beta$$

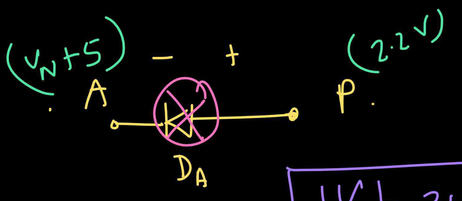
$$\Rightarrow 5{\cdot}46 < \beta$$

$$\beta_{min} = 5{\cdot}46$$

Noise Margin Calculation

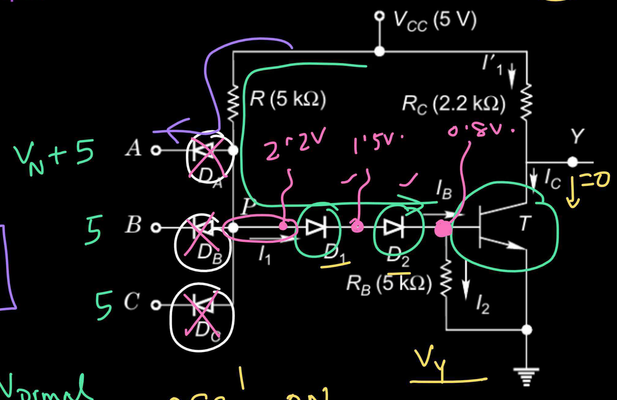
Diode:	Voltage across a conducting diode	= 0.7 V
	Cut-in voltage V_γ	= 0.6 V
Transistor:	Cut-in voltage V_γ	= 0.5 V
	$V_{BE,sat}$	= 0.8 V
	$V_{CE,sat}$	= 0.2 V
$\beta =$	h_{FE}	= 30

Q. If all the inputs are high, then what is magnitude of noise voltage at one of the input terminals which will cause the gate to malfunction? Assume no load connected to output.



$|V_N| = 3.4$

V_N	V_A	V_{D_A}
0	5	−2.8
−3	2	0.2
−3.4	1.6	0.6 V ON.



Normal operation: OFF | ON

Malfunction: ON | OFF 5V

Q. If one of the inputs is low, then what is magnitude of noise voltage at low input terminal which will cause the gate to malfunction? Assume no load is connected to output.

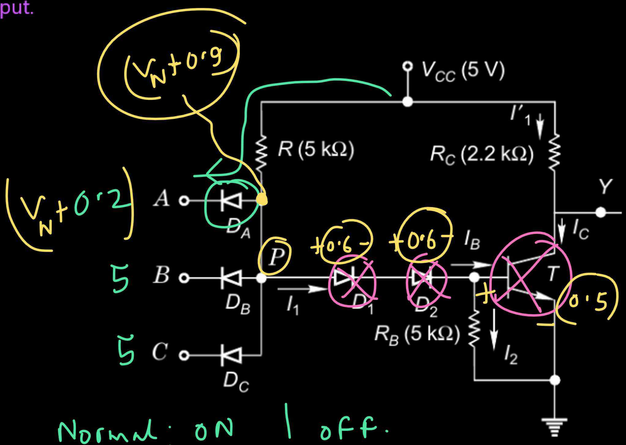
$V_p = 0.6 + 0.6 + 0.5$

$= 1.7V$

$= V_N + 0.9$

$\therefore V_N = 0.8\ V$

$|V_N| = 0.8V$



Normal: ON | off.

Malfunction: OFF | ON.

Noise Margin

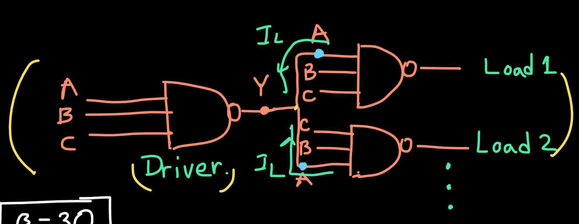
$$NM = \min(NM_L, NM_H)$$

$NM_L = 0.8\ V$

$NM_H = 3.4\ V$

$NM = 0.8\ V$

Max Fanout Calculation



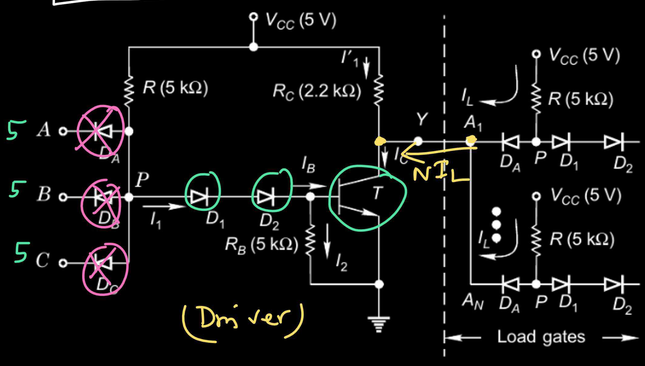
Case 1 All inputs are high (Output is Low)

$\beta = 30$

$I_C = I_1' + N I_L$ $I_C(N)$

$I_1' = \frac{V_{CC} - V_Y}{2.2K} = 2.182\ mA.$

(no-load collector current)



$I_L = \frac{V_{CC} - V_P}{R} = \frac{5 - 0.9}{5K} = 0.82\ mA$

I_L (Standard load) (single load)

$\frac{I_C}{I_B} < \beta$ $\quad (I_B = 0.4\ mA).$

$\Rightarrow I_1' + N I_L < \beta I_B$

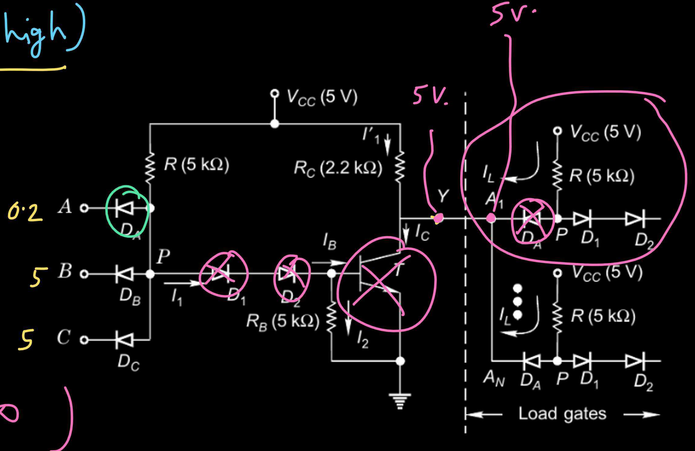
$\Rightarrow N I_L < \beta I_B - I_1'$

$\Rightarrow N < (\beta I_B - I_1')/I_L \Rightarrow N < \frac{30 \times 0.4 - 2.182}{0.82}$

$\Rightarrow N < 11.97$

$N_{max} = \lfloor 11.97 \rfloor = 11$

Case 2 At least one input is low (Output is high)



$I_L = 0$

max fanout $= \infty$.

Max fanout $= \min(11, \infty)$

$= 11$