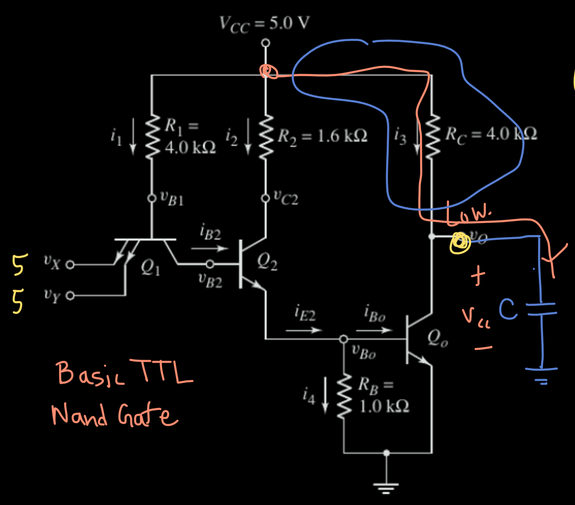
# TTL Output Stages




## Output state Transition.

(High→Low) ⎿ (C has to discharge)

Time ∝ 'C' to discharge ∝ RC

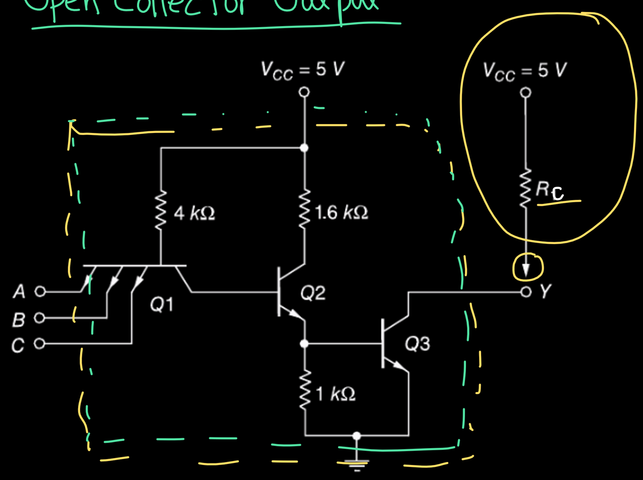
'Pull-Down Network'

(Low→High) ⎾

Time ∝ $R_cC$

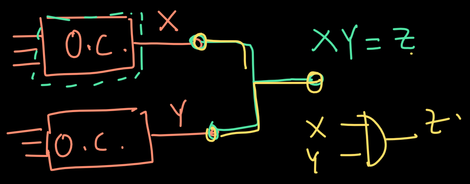
'Pull-Up Network'

## Open Collector Output

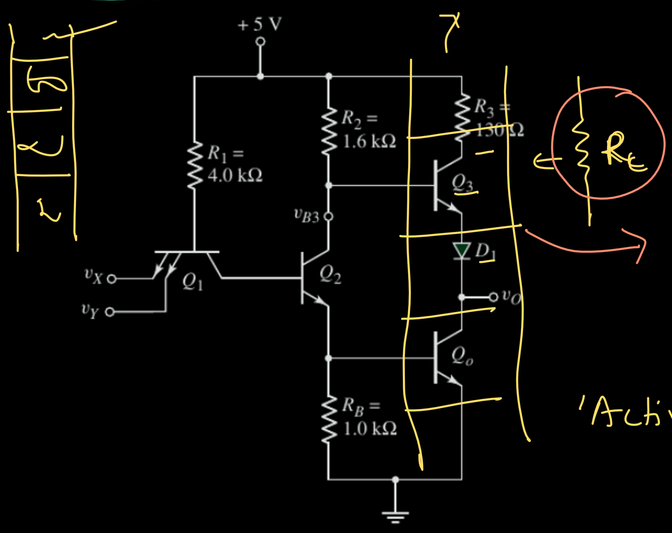



1. Drive external load.

2. Wired 'AND'.




## 'Totem-pole' Output



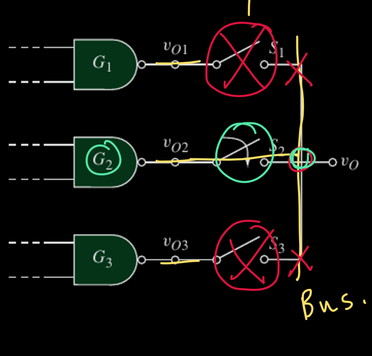

(Low→High) ∝ RC

P↑ R↓ t↓

(Totem-pole output decreases Low→High transition time while not increasing power dissipation proportionately)

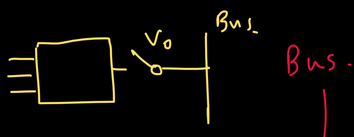
'Active pull-up'.

## Tri-state Output

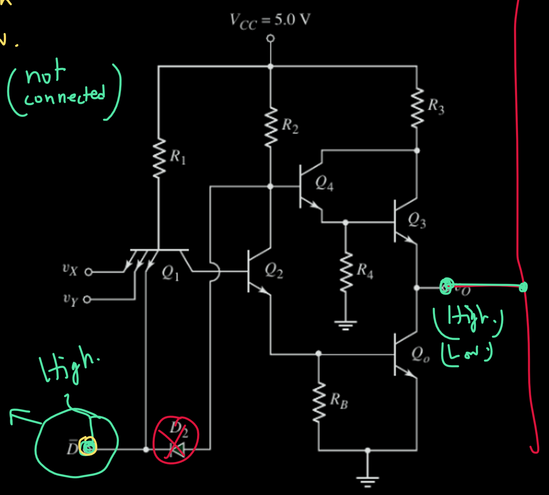



High
Low.

High Impedance. ← Z (not connected)

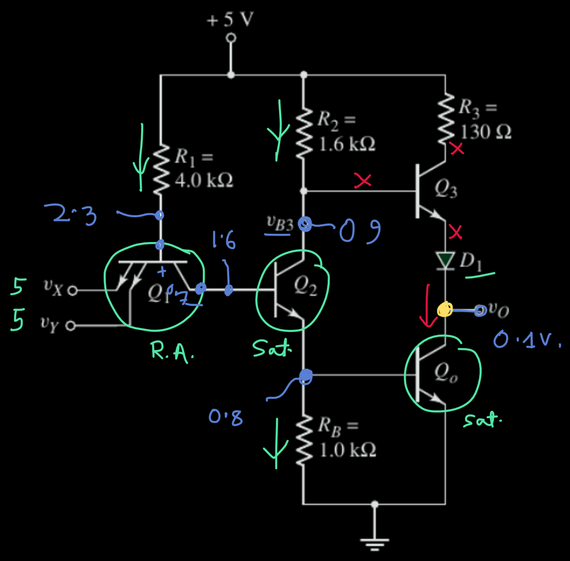



Bus.



# Operation of Totem-pole Nand Gate

$V_{CE(sat)} = 0.1V$, $V_{BE(sat)} = 0.8V$.

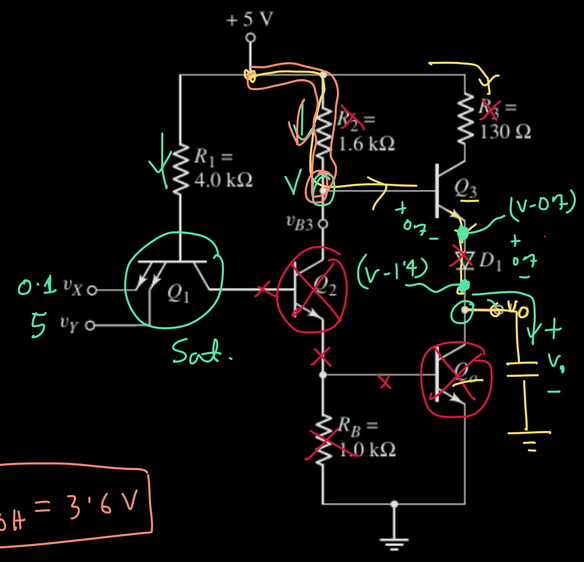



Case 1 $v_X = v_Y =$ High $= 5V$

$i_{B(Q_3)} = 0$, $i_{C(Q_3)} = 0$, $i_{E(Q_3)} = 0$.

$$\boxed{i_{C(Q_0)} = 0}$$

Case 2 Atleast one input 'Low' $(= 0.1)$




$I_{E(Q_3)} = 0$. (Steady-state)

Before S-S

$Q_3$ : F.A.

$V_o = V - 1.4$

$= V$ (steady-state) $- 1.4$

$= 5 - 1.4 = \boxed{3.6V}$

$$\boxed{V_{OH} = 3.6V}$$

# Fanout of Totem-pole Nand Gate

$i_{C2} = \frac{5 - 0.9}{2K} = 2.05$ mA.

$i_{E2} = i_{C2} + i_{B2} = 2.59$ mA.

17.30 In the TTL circuit in Figure P17.30, the transistor parameters are $\beta_F = 20$ and $\beta_R = 0.10$ (for each input emitter). (a) Calculate the maximum fanout for $v_X = v_Y = 5$ V. (b) Calculate the maximum fanout for $v_X = v_Y = 0.1$ V. (Assume $v_O$ is allowed to decrease by 0.10 V from the no-load condition.)

**Table 17.3** Piecewise linear parameters for a pn junction diode and npn bipolar transistor

| Parameter | Value |
|---|---|
| $V_\gamma$ | 0.7 V |
| $V_{BE}$(on) | 0.7 V |
| $V_{BE}$(sat) | 0.8 V |
| $V_{CE}$(sat) | 0.1 V |

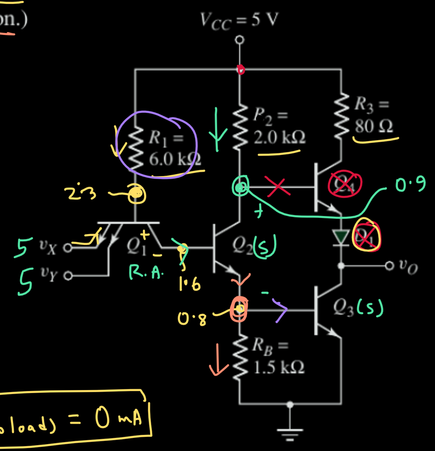



Figure P17.30

(a) $i_{CQ_3} = 0$

$i_{B1} = \frac{5 - 2.3}{6K} = 0.45$ mA.

$i_{Ex} = \beta_R i_{B1} = 0.045$ mA $= i_{Ey}$.

$\therefore i_{C1} = i_{B1} + i_{Ex} + i_{Ey} = 0.54$ mA. $= i_{B2}$

$i_{E2} = i_{B3} + i_{RB}$ $\quad i_{RB} = \frac{0.8}{1.5K} = 0.53$ mA.

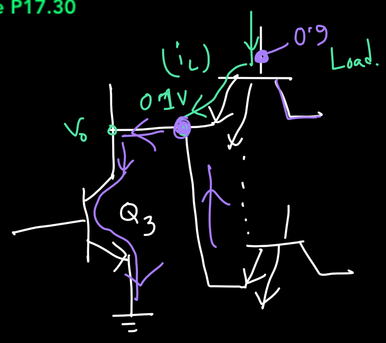
$\therefore \boxed{i_{B3} = 2.06 \text{ mA}}$

$\boxed{i_{C3}(\text{no load}) = 0 \text{ mA}}$

$i_L = \frac{5 - 0.9}{6K} = 0.68$ mA.

$\frac{i_{C3}}{i_{B3}} < \beta_F \Rightarrow i_{C3} < \beta_F i_{B3}$

$\Rightarrow N i_L < \beta_F i_{B3}$ $\quad \boxed{\therefore N_{max} = 60}$




(b) (b) Calculate the maximum fanout for $v_X = v_Y = 0.1$ V. (Assume $v_O$ is allowed to decrease by 0.10 V from the no-load condition.)

$i_{C4} = \frac{5 - V_{C4}}{0.08K}$ $\quad \therefore V_{C4} = 4.92$ V.

$\boxed{V_{CE} = 4.92 - 4.2 = 0.72 > 0.2 \text{ V}}$

$i_{R2} = \frac{5 - 4.9}{2K} = 0.05$ mA. $= i_{B4}$

$i_{C4} = \beta_F i_{B4} = 1$ mA

$\boxed{i_{E4}} = (\beta_F + 1) i_{B4} = 1.05$ mA. (Supply).

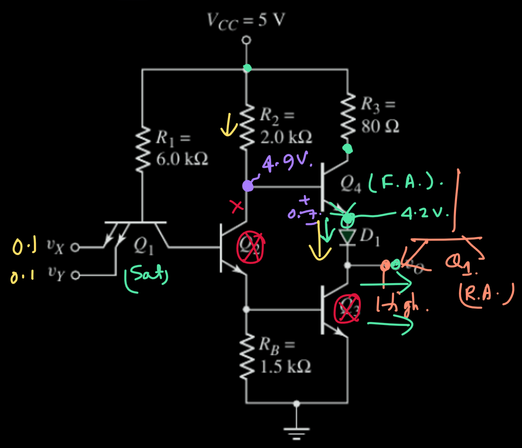



Figure P17.30

Individual demand

$i_L = i_{Ex} = 0.045$ mA $(\longrightarrow)$

Supply $\geq$ Demand.

$\Rightarrow i_{E4} \geq N i_L$

$\therefore N_{max} = \left\lfloor \frac{i_{E4}}{i_L} \right\rfloor = \boxed{23}$

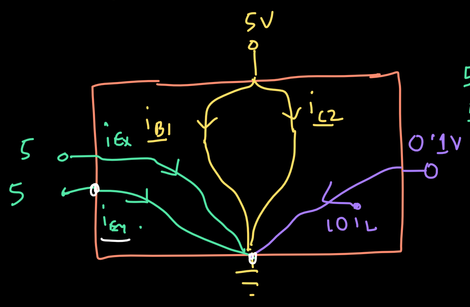
# Power Dissipation in Driver

For the circuit of 17.30, (a) calculate power dissipation in the driver circuit for $V_X = V_Y = 5$ and fanout of 10.

$i_{Ex} = i_{Ey} = 0.045$ mA,

$i_{B1} = 0.45$, $i_{C2} = 2.05$ mA.

$i_L = 0.68$ mA.



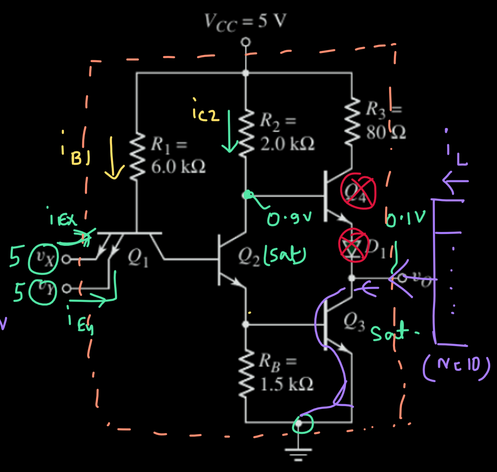




Figure P17.30

$$P_{tot} = \sum \Delta V \times I = 5 \times i_{Ey} + 5 \times (i_{Ex} + i_{B1} + i_{C2}) + (0.1 - 0) \times 10 i_L$$

$$= 13.63 \text{ mW.}$$

(b) Calculate power dissipation in the driver for $V_X = V_Y = 0.1$V and fanout of 10.

$i_{B1} = 0.68$ mA.

$i_{B4} = ?$

$i_{B4} = \frac{5 - V}{2k} = 0.02$

$\therefore \boxed{V = 4.96 \text{ V.}}$

$i_{E4} = 10 i_L = 10 \times 0.045 = 0.45$ mA.

$i_{E4} = (\beta + 1) i_{B4} \Rightarrow i_{B4} = 0.02$ mA.

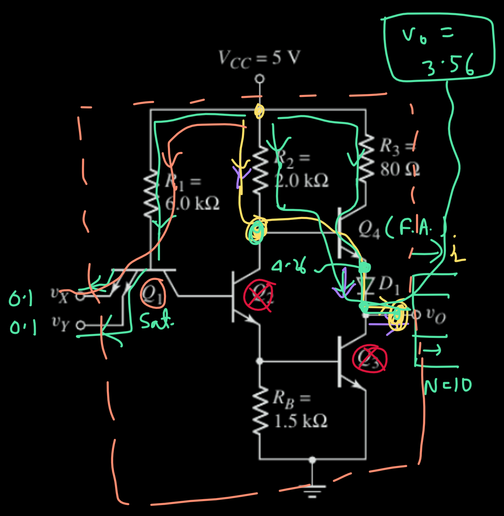
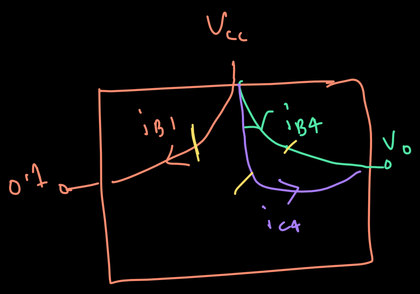



Figure P17.30



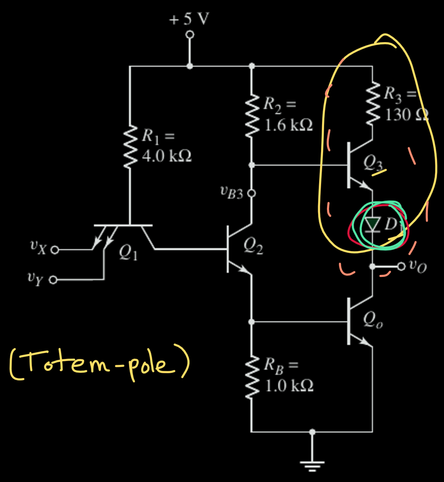

$$P_{tot} = (V_{CC} - 0.1) \times i_{B1} + (V_{CC} - V_o) \times (i_{B4} + i_{C4})$$

$$= 3.94 \text{ mW.}$$

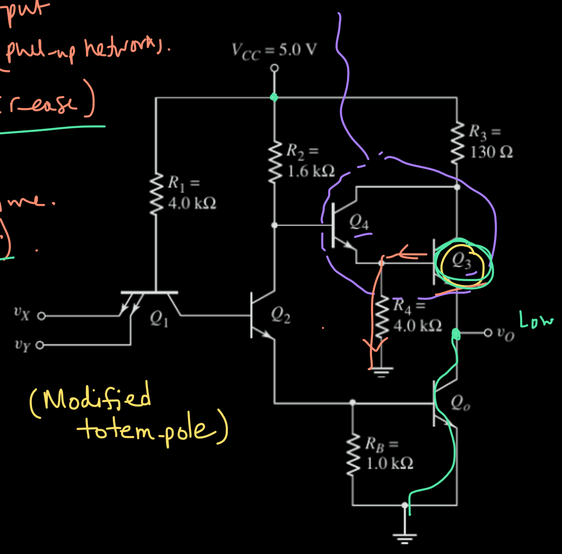
## Modified Totem-pole Output

Darlington Pair.

1. Lower output resistance (pull-up network). (decrease)
2. Storage time. (Lower).

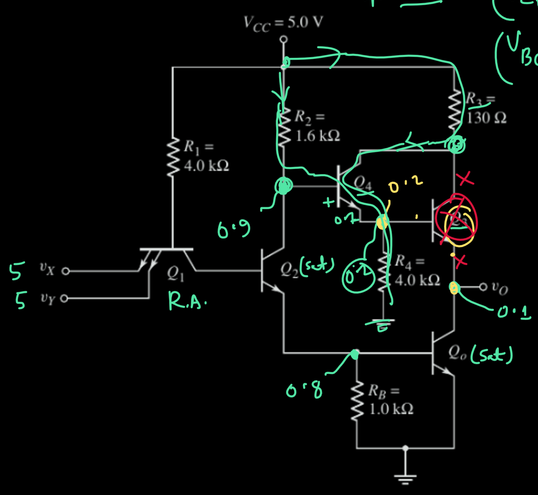



(Totem-pole)

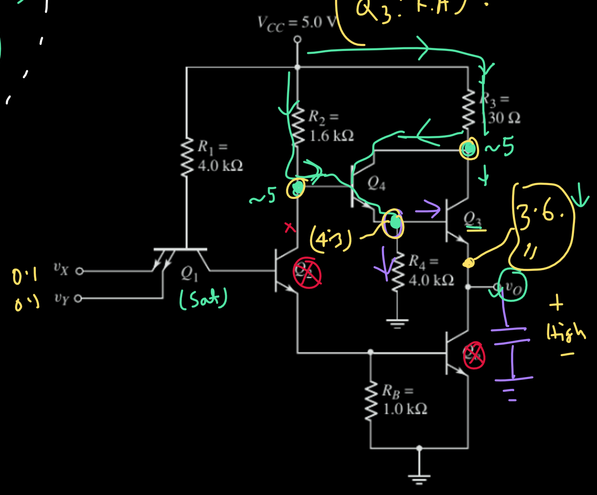



(Modified totem-pole)

Case 1 $V_X = V_Y = 5V$. $Q_3$: cut-off. $Q_4$: F.A. ($V_{CE} > 0.2$) ($V_{BC} < 0$)




Case 2 $V_X = V_Y = 0.1$ ($Q_4$: (BC: Reverse Bias)) ($Q_4$: F.A. $Q_3$: F.A).




# Recommended Practice Problems from

(DTL, TTL).

Neamen's *Microelectronics: Circuit Analysis and Design (4th Edition)*

**Chapter 17: 17.20, 17.21, 17.23, 17.25, 17.28, 17.32**