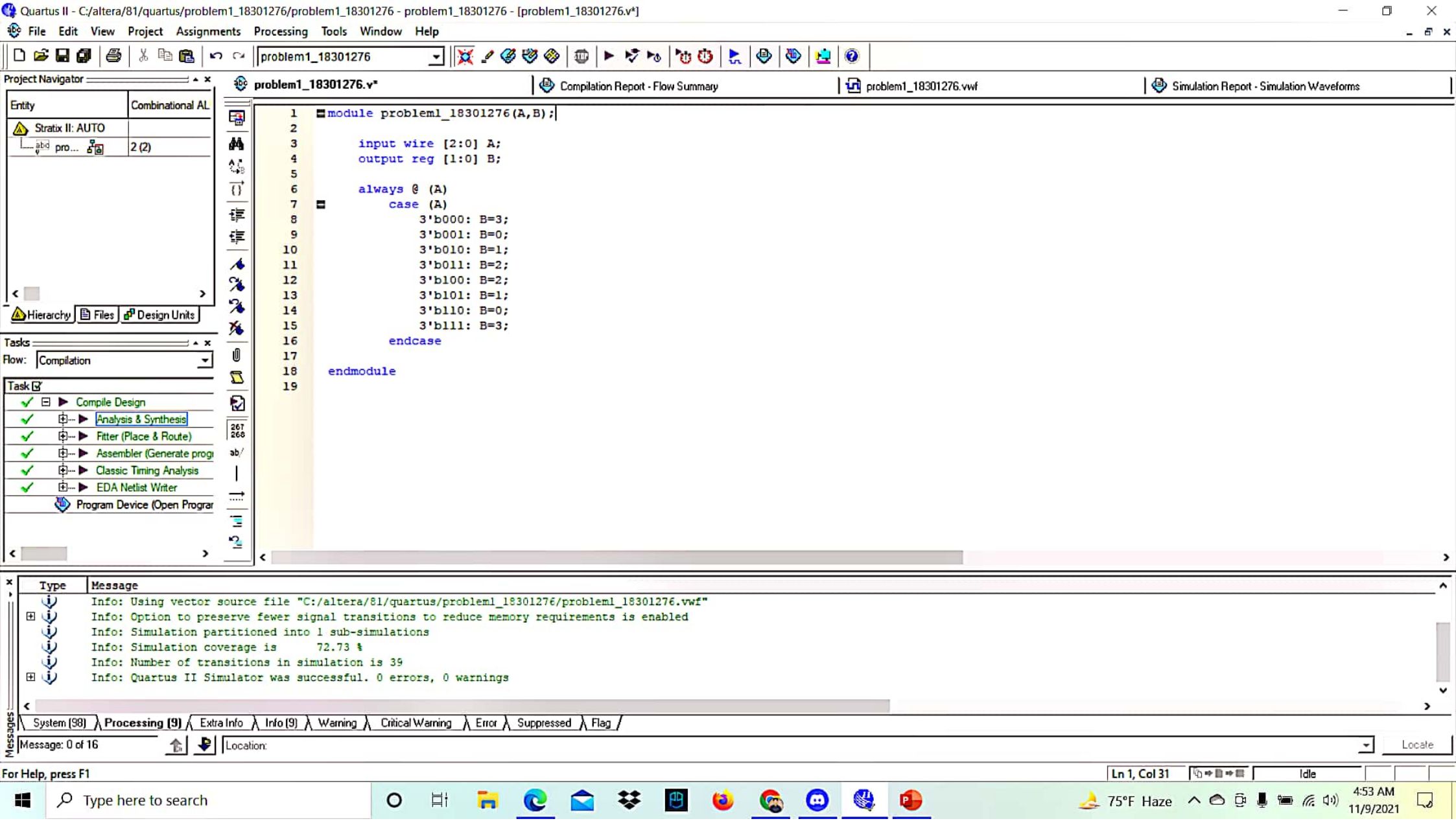

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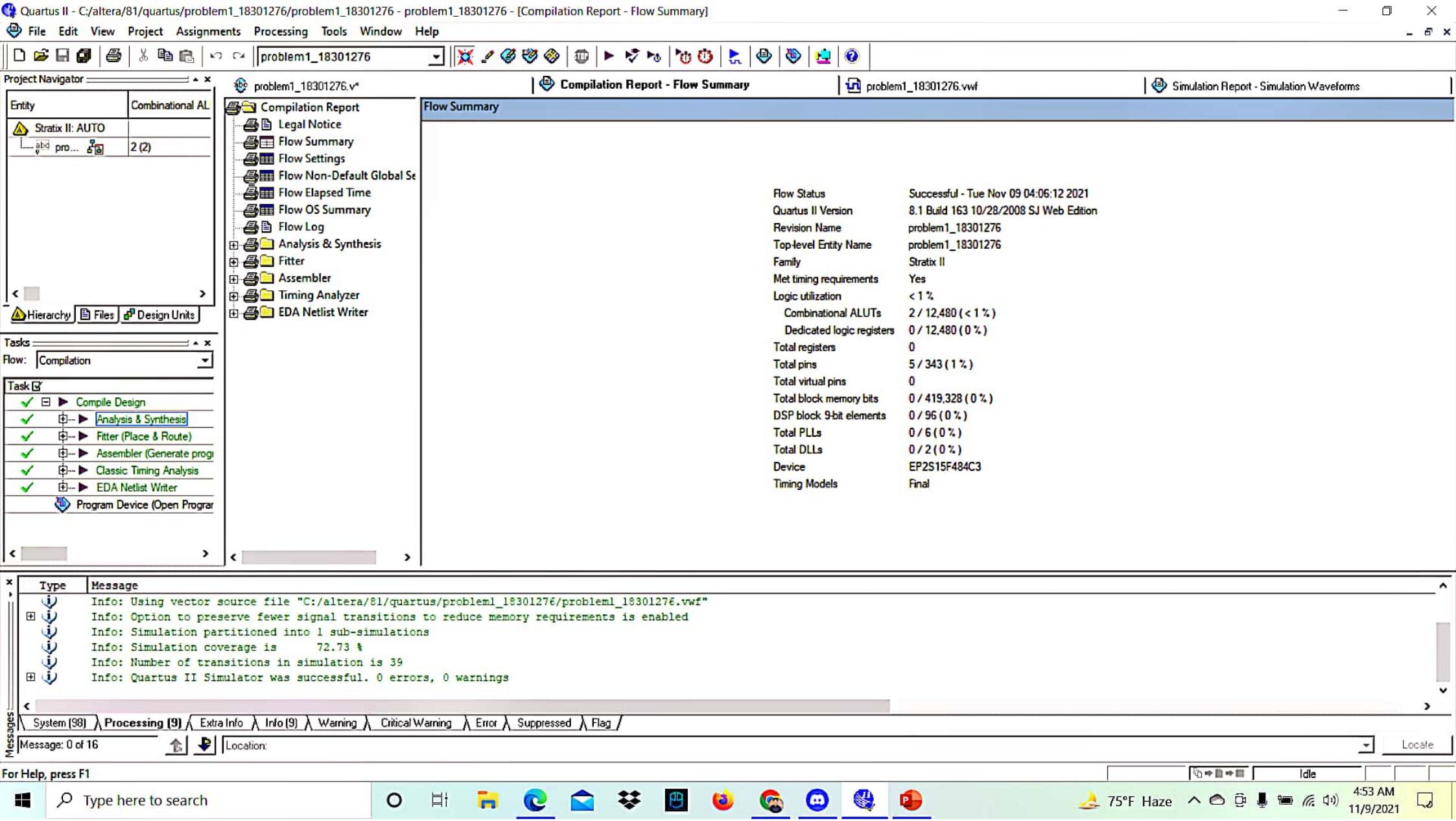

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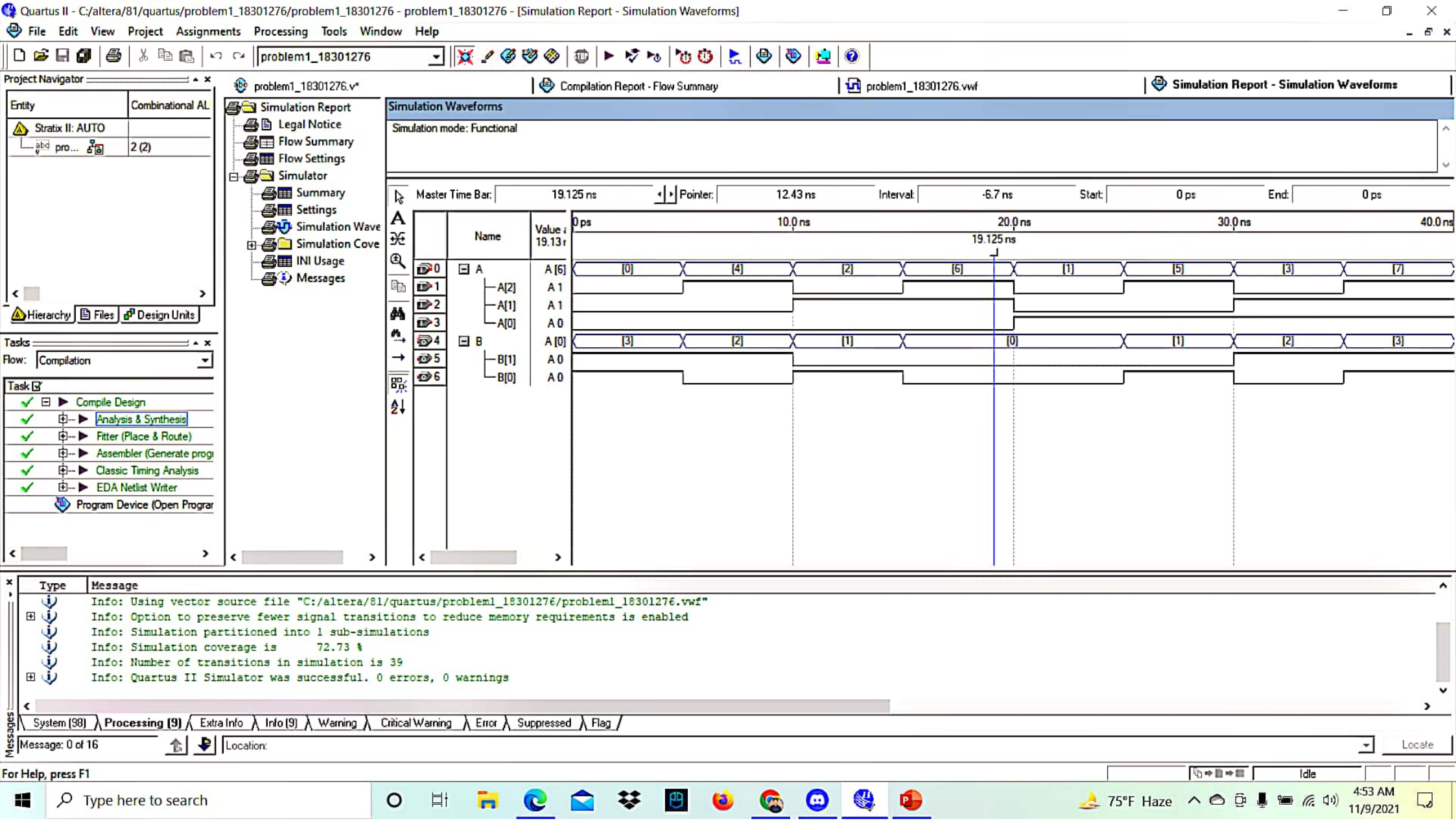

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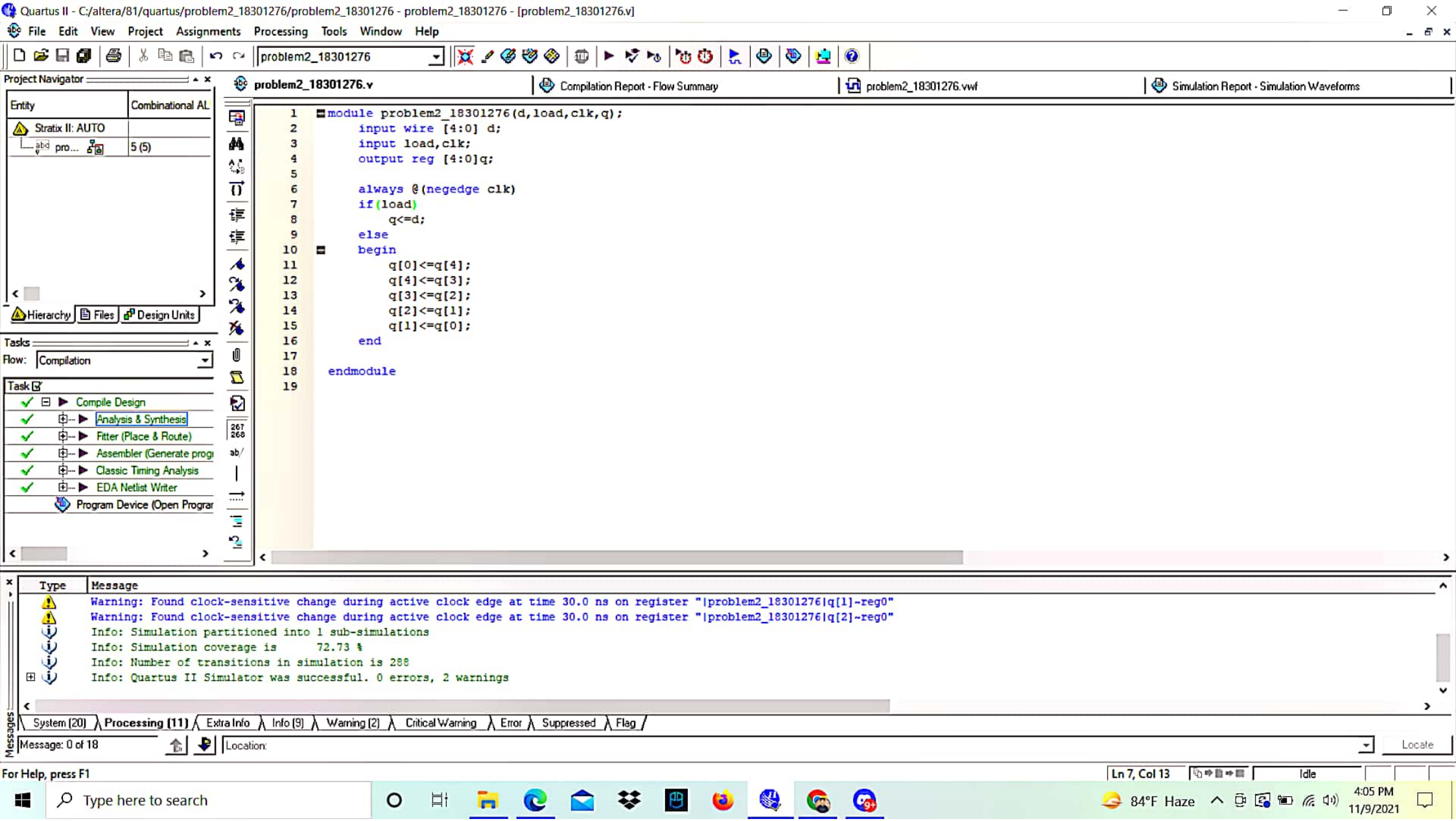

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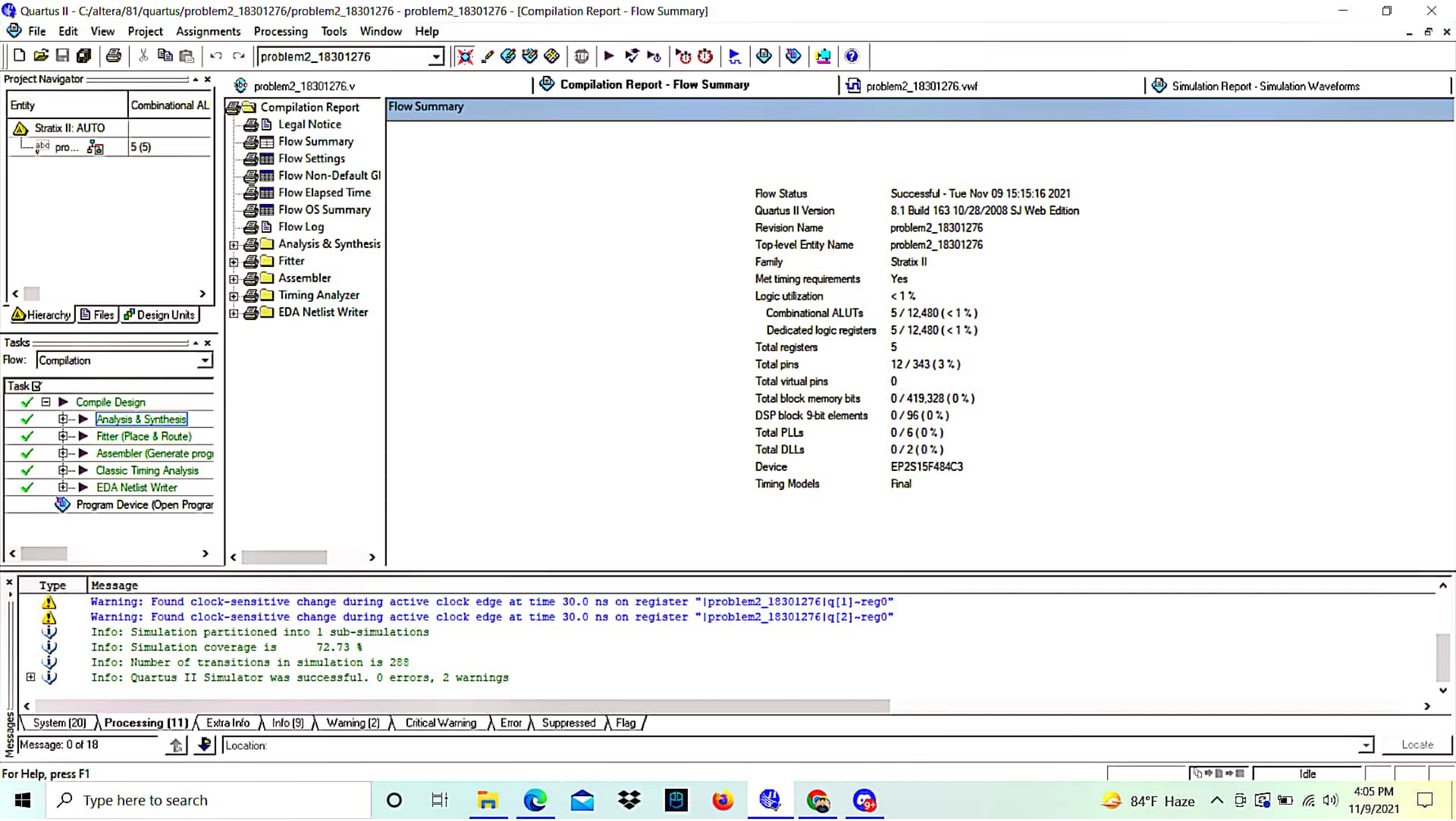

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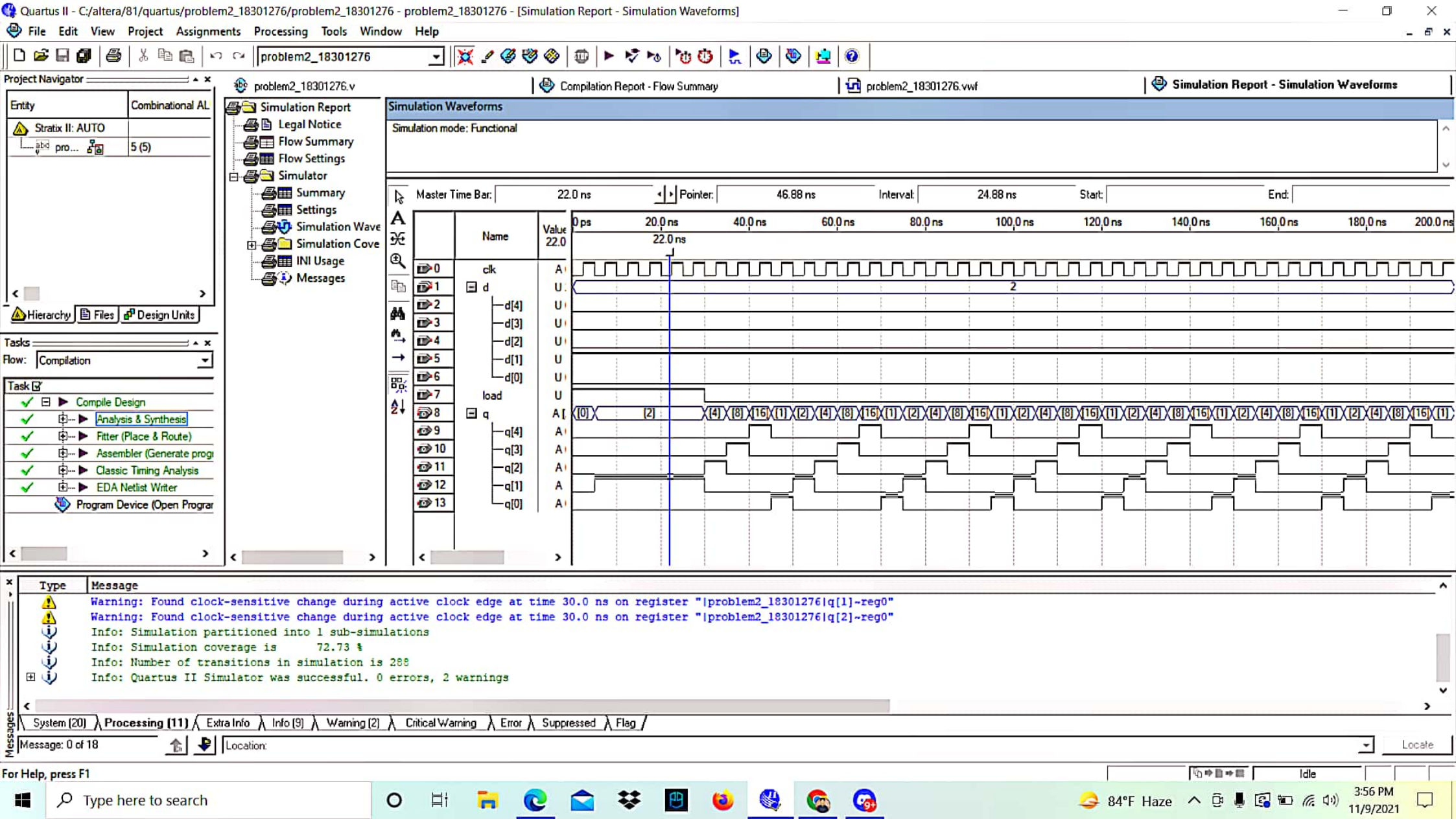

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#18301276

Problem 1:

Here in the code, A is a 3-bit width input and B is the 2-bit width output to show the unique bit position for every possible cases.

For 3 bit input, there will be 8 combination.

Input (A)	Output (B) indecimal	Output (B) in binary
000	3	11
001	0	00
010	1	01
011	2	10
100	2	10
101	1	01
110	0	00
111	3	11

Problem 2:

Here it is a 5-bit end around left shift register which operates at the negative edge of clk with load functional and qr is the output of the shift register.

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In the timing diagram we can clearly see that, ~~for every~~ after 5 clock cycles for every negative edge in the clk, there is a rise in the output q and after that repetitions is occur after every 5 clock cycles.

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