CSE460 VLSI Design
Final Exam

Date: 8 January, 2022
Time: **05.50 PM - 07.10 PM**
Duration: **1 hour 20 minutes**
PDF preparation & submission: Additional **15 minutes**

Last time to submit: 7.25 PM

Your name, ID, section, slot no. & signature should be at the beginning of your script

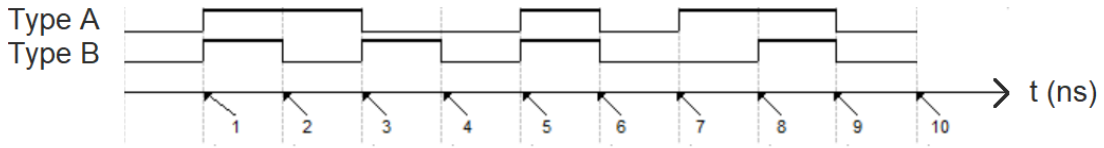
This page does not contain any question, the following page does.

*Answer any 3 questions. Each question is worth **10** points. Total marks: 3 x 10 = 30.*

1. Consider an nMOS transistor in a **0.8 µm** process with **W = 1.2 µm** and **L = 0.6 µm**. In this process, the gate oxide thickness is **100 Å** and the mobility of electrons is **350 $cm^2/V \cdot s$**. The threshold voltage is **0.7 V**. The permittivity of free space, **8.85×10^{-14} F/cm**, and the permittivity of SiO_2 is **k_{ox} = 3.9** times as great. **[10]**
    a. Plot I_{ds} vs. V_{ds} for V_{gs} **= 0.5 V** & **3.5 V**. The plot must be properly labeled.
    b. Repeat the previous question if the threshold voltage was increased to **4 V**.

2. Consider a CMOS inverter in a **0.8 µm** process, where the pMOS transistor is **8 times** wider than the nMOS transistor. Assume a mobility ratio of **2**. **[10]**
    a. What is the beta ratio of the inverter?
    b. Draw an approximate DC response curve of the inverter and determine the values of V_{IL}, V_{IH}, V_{OL} & V_{OH} from the DC response curve; such that the noise margins are maximized. (Assume $V_{tn} = |V_{tp}| = 0.2$ **V**; V_{DD} **= 1 V**.)
    c. Using your answer from Ques. No. 2(b), find the approximate values of NM_H & NM_L and comment on your result.

3. A digital system-on-chip in a **1 V**, **65 nm** process (with **50 nm** drawn channel lengths and **λ = 25 nm**) has **1 billion** transistors, of which **500 million** are used in type ***A*** logic gates and the remainder are used in type ***B*** logic gates. The average type ***A*** transistor width is **12 λ** and the average type ***B*** transistor width is **8 λ**. A typical behavior of the output signal of both type of logic gates for a single clock cycle is shown below: **[10]**



Assume each transistor contributes **1 fF/µm** of gate capacitance and **0.8 fF/µm** of diffusion capacitance. *Neglect* wire capacitance. The system is operating at **1 GHz**.
    a. Estimate the activity factor for type A & type B logic gates.
    b. Estimate the switching power of the system.

4. Answer the following questions: **[10]**
    a. Describe the CTS stage of physical design. Why is it required for chip design?
    b. Sketch a **3-input** NOR gate with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (***R***). Compute the rising and falling propagation delays of the NOR gate driving ***h*** identical NOR gates using the Elmore delay model. Assume shared diffusion terminal for series transistors, and that every source or drain has fully contacted diffusion.