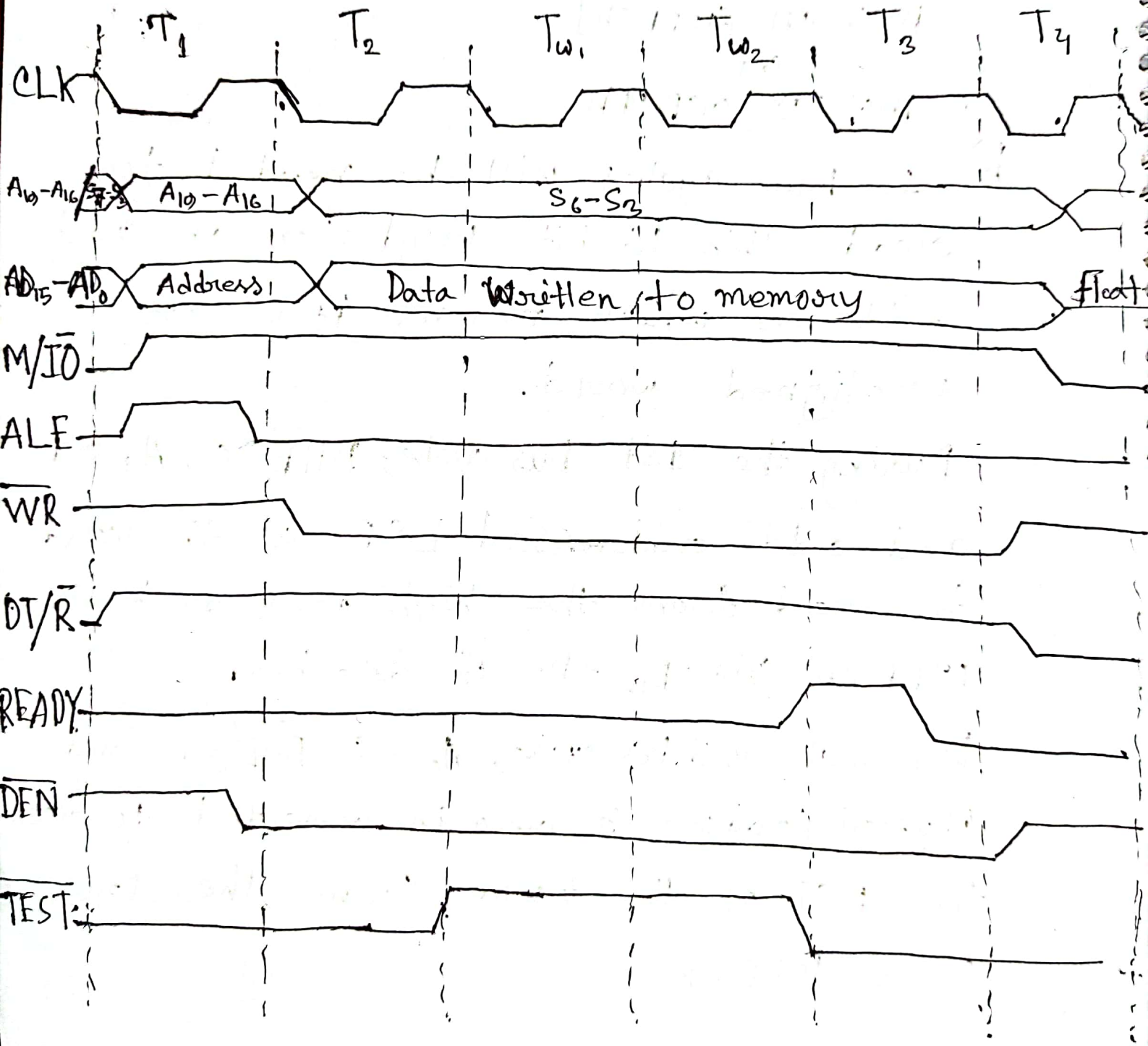
18301276

Question 1:



Here, During T_1 state, Address of memory is sent out by using control signal ALE. M/$\overline{IO}$ is high during the whole bus-cycle which signifies memory is accessed in this cycle. DT/$\overline{R}$ is high means data is transmitted out to memory. DEN is enabled at the end of T_1 which means transceiver on memory is connected. After that, Data to be written appear on data bus $AD_{15} - AD_0$. $\overline{WR}$ is low from that time which defines writing data to memory. At the end of T_2, when memory was not Ready, $\overline{TEST}$ pin appears high and cpu enters idle state. After two wait states, $\overline{TEST}$ becomes low and READY pin appears high which signifies completion of data transfer.

#1830127 6

Question 2:

a) MOV CX, [12BE7h]

or,

MOV CL, [12BE7h]

MOV CH, [12BE8h]

or,

MOV CX, 06BC1h

b) 2 bus-cycles will be needed to read this 16 bit word from an odd address which means it is an unaligned word.

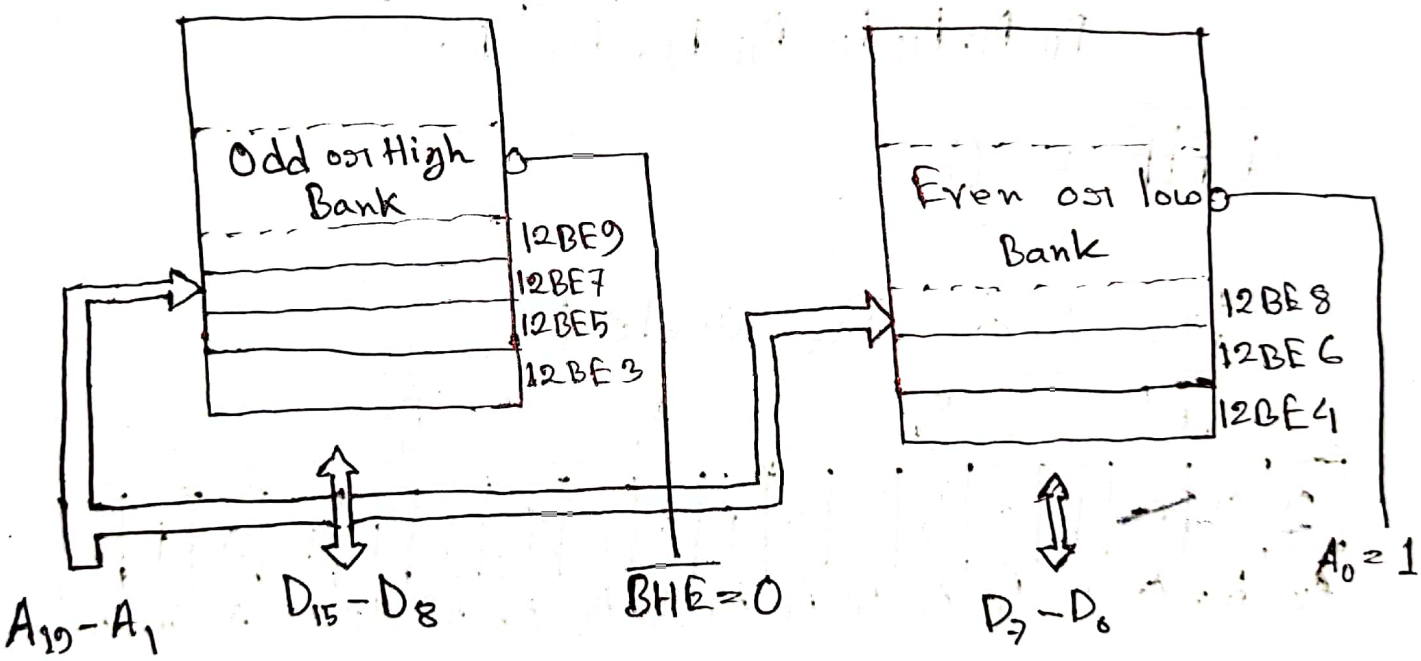
During the 1st bus-cycle, $\overline{BHE} = 0$, $A_0 = 1$ and odd addressed LSB of the word is read from the high memory bank 12BE7h via $D_{15} - D_8$ of data bus.

During the 2nd bus-cycle, $A_0 = 0$, $\overline{BHE} = 1$ and Physical address is auto incremented to read the MSB of the word from the low Bank 12BE8h.

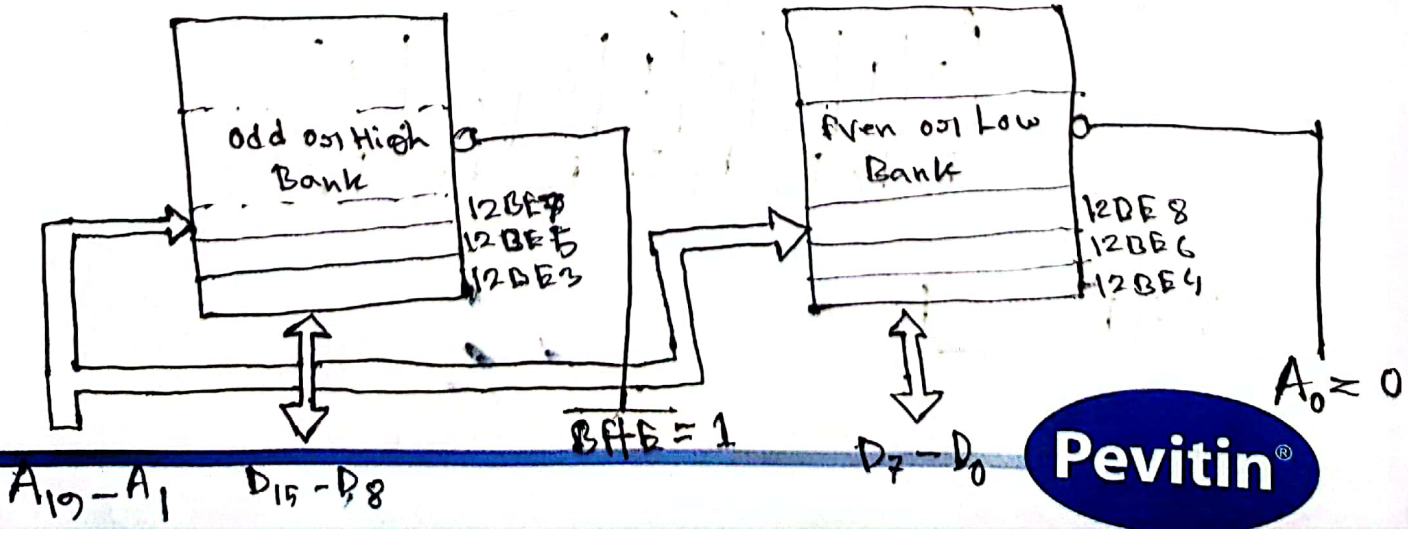
#18301276

c) The connection for data transfer between processor and memory for, 2 byte data is drawn below:

During 1st bus-cycle, LSB of the word in $D_{15}-D_8$



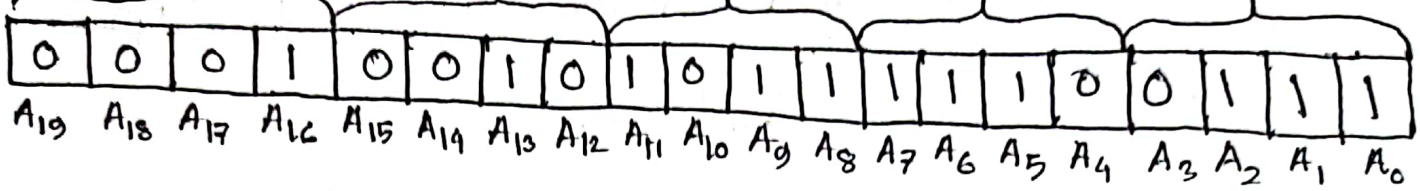
During 2nd bus-cycle; MSB of the word in D_7-D_0



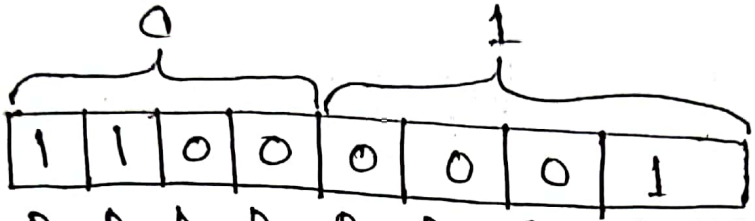
#18301276

d) For 1st Bus-Cycle:

Address = 1 2 B E 7

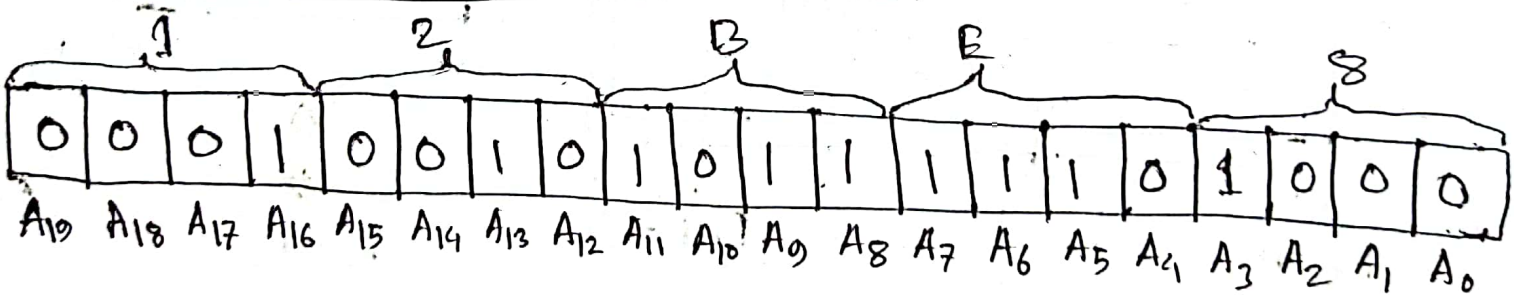


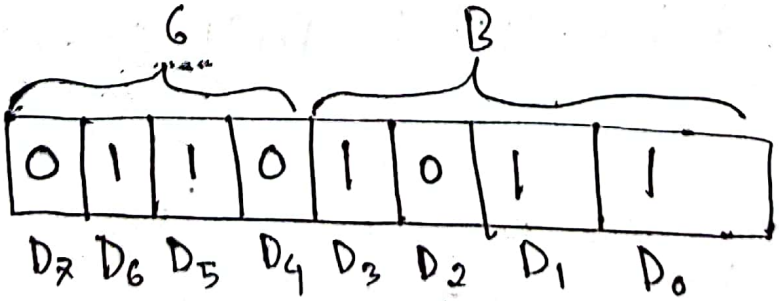
Data = C 1



$\overline{BHE} = 0$

For 2nd Bus-Cycle:





$\overline{BHE} = 1$