

Quartus II - C:/altera/81/quartus/problem1_18301276/problem1_18301276 - problem1_18301276 - [problem1_18301276.v*]

File Edit View Project Assignments Processing Tools Window Help

problem1_18301276

problem1_18301276.v* | Compilation Report - Flow Summary | problem1_18301276.vwf | Simulation Report - Simulation Waveforms

Entity: Combinational AL

Stratix II: AUTO

pro... 2 (2)

Hierarchy | Files | Design Units

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate progi)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Prograr)

```

1 module problem1_18301276 (A, B);
2
3     input wire [2:0] A;
4     output reg [1:0] B;
5
6     always @ (A)
7     case (A)
8         3'b000: B=3;
9         3'b001: B=0;
10        3'b010: B=1;
11        3'b011: B=2;
12        3'b100: B=2;
13        3'b101: B=1;
14        3'b110: B=0;
15        3'b111: B=3;
16    endcase
17
18 endmodule
19

```

267
268

ab/

Messages

Type	Message
Info	Info: Using vector source file "C:/altera/81/quartus/problem1_18301276/problem1_18301276.vwf"
Info	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Info: Simulation partitioned into 1 sub-simulations
Info	Info: Simulation coverage is 72.73 %
Info	Info: Number of transitions in simulation is 39
Info	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (98) | Processing (9) | Extra Info | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag

Message: 0 of 16

Location:

For Help, press F1

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Type here to search

75°F Haze 4:53 AM 11/9/2021

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Stratix II: AUTO	
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- Flow Non-Default Global Se
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
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- EDA Netlist Writer

Flow Summary

Flow Status	Successful - Tue Nov 09 04:06:12 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem1_18301276
Top-level Entity Name	problem1_18301276
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	2 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	5 / 343 (1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

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Hierarchy Files Design Units

Tasks

Flow: Compilation

Task

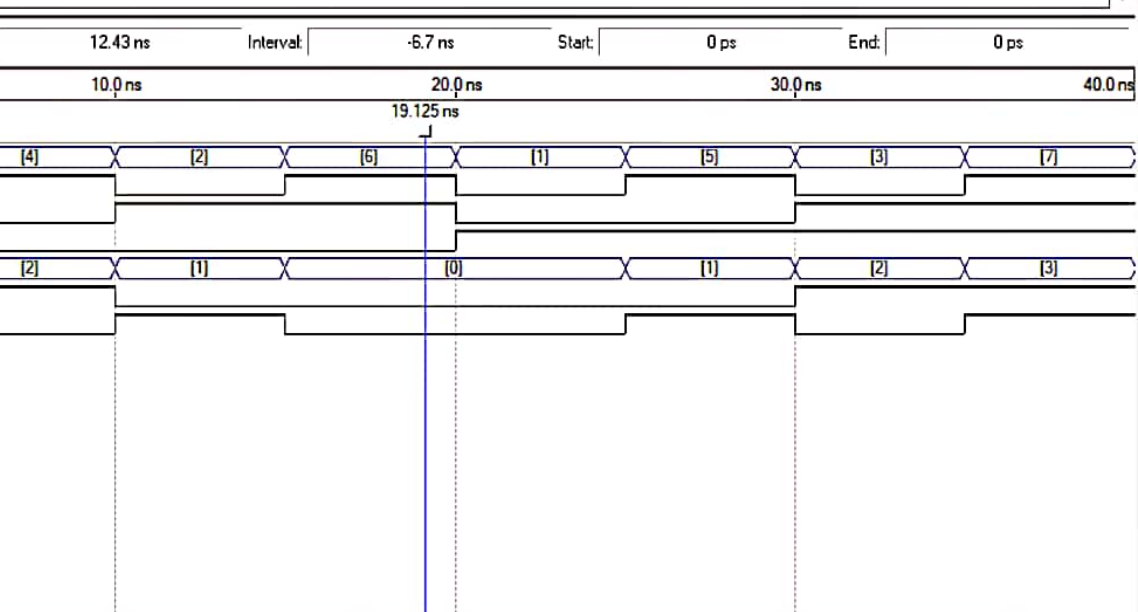
- Compile Design
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- Simulator
- Summary
- Settings
- Simulation Wave
- Simulation Cove
- INI Usage
- Messages

Simulation mode: Functional

Master Time Bar: 19.125 ns Pointer: 12.43 ns Interval: -6.7 ns Start: 0 ps End: 0 ps

Name	Value
A	A [6]
A[2]	A 1
A[1]	A 1
A[0]	A 0
B	A [0]
B[1]	A 0
B[0]	A 0



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```

1 module problem2_18301276 (d, load, clk, q);
2     input wire [4:0] d;
3     input load, clk;
4     output reg [4:0] q;
5
6     always @(negedge clk)
7     if (load)
8         q <= d;
9     else
10        begin
11            q[0] <= q[4];
12            q[4] <= q[3];
13            q[3] <= q[2];
14            q[2] <= q[1];
15            q[1] <= q[0];
16        end
17
18 endmodule
19

```

- Warning: Found clock-sensitive change during active clock edge at time 30.0 ns on register "|problem2_18301276|q[1]-reg0"
- Warning: Found clock-sensitive change during active clock edge at time 30.0 ns on register "|problem2_18301276|q[2]-reg0"
- Info: Simulation partitioned into 1 sub-simulations
- Info: Simulation coverage is 72.73 %
- Info: Number of transitions in simulation is 288
- Info: Quartus II Simulator was successful. 0 errors, 2 warnings

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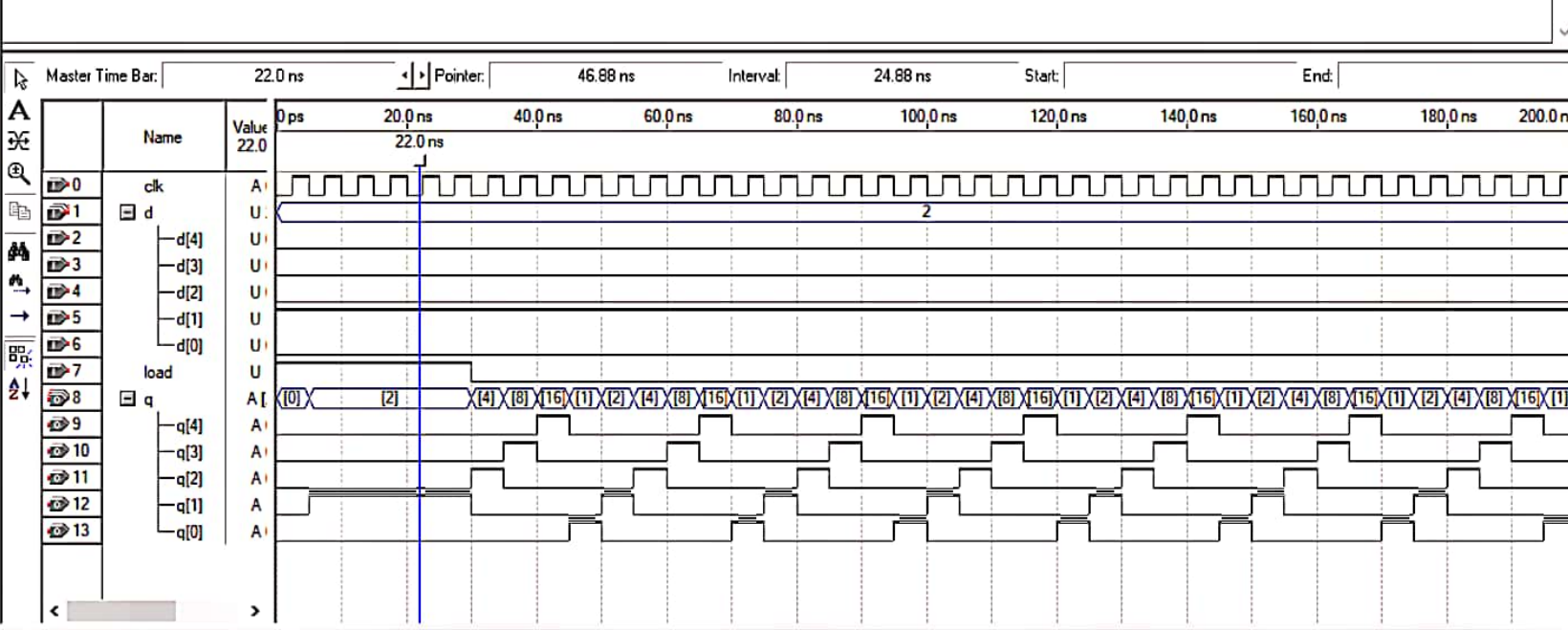
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Simulation Waveforms

Simulation mode: Functional



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Problem 1:

Here in the code, A is a 3-bit width input and B is the 2-bit width output to show the unique bit position for every possible cases. For 3 bit input, there will be 8 combinations.

Input (A)	Output (B) in decimal	Output (B) in binary
000	3	11
001	0	00
010	1	01
011	2	10
100	2	10
101	1	01
110	0	00
111	3	11

Problem 2:

Here it is a 5-bit end around left shift register which operates at the negative edge of clk with load function and q is the output of the shift register.

In the timing diagram we can clearly see that, ~~for every~~ after 5 clock cycles for every negative edge in the clk, there is a rise in the output q and after that repetitions occur after every 5 clock cycles.