#1830127G

Input A	Input B	Input (VA)	Input (VB)	V_0	V_1	V_2	V_3	V_4	V_6	V_5
0	0	0	0	4.61312	0.717354	0.007690	8.81×10^{-9}	5	5	4.80314
0	1	0	5	4.61312	0.755312	0.049408	8.89×10^{-9}	5	5	4.80314
1	0	5	0	4.61312	0.755312	0.049408	8.89×10^{-9}	5	5	4.80314
1	1	5	5	0.0005	2.68739	1.95768	1.05263	1.14492	4.9965	0.57797

Table:1

Report:

1) When One or both input is low, T_1 and T_2 transistors will go to saturation mode. It will result T_3 and T_4 in Cut-off mode because very small amount of current will flow from the base of T_3. For this, T5 transistor will be in active region

since it will have 5V at base and positive voltage at emitter. Thus, output will be high.

On the other hand, if both inputs are high T_1 and T_2 will go to reverse active mode which will make the T_3 in saturation mode and this will put the T_4 in saturation mode. As a result, T_5 will be is cut off mode and output will be logic low.

2) Totem pole stage is one output format of TTL circuits. In this stage, one transistor works as a pull-down structure and another works as pull-up structure.

Also, in totem pole structure, pull up resistance is low for this pull up stage takes way less time.

3)

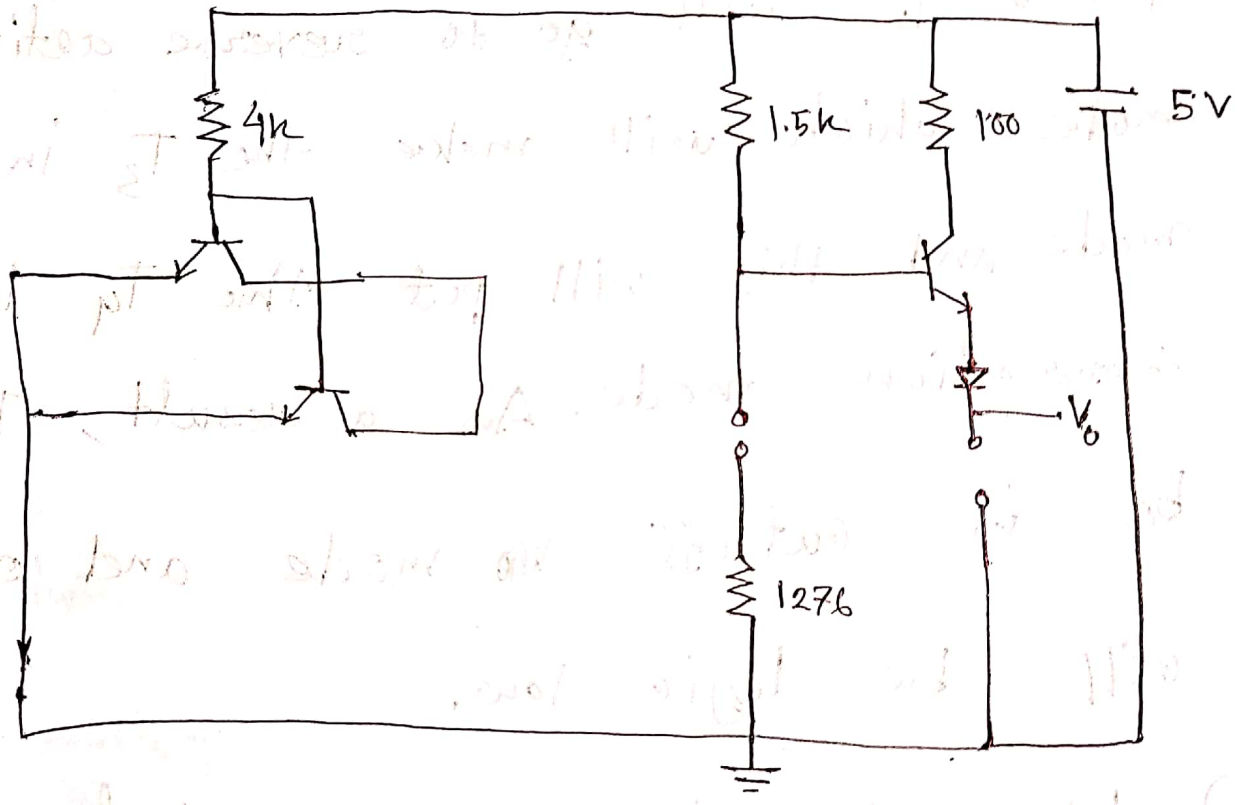

Fig: When both input are low

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4) Here, T_3 works as a phase splitter or a switch.

5) If Diode D_1 is not used, then output could be high when it is supposed to be low.

6) When at least one input is low, T5 transistor will be in forward active mode.

7)

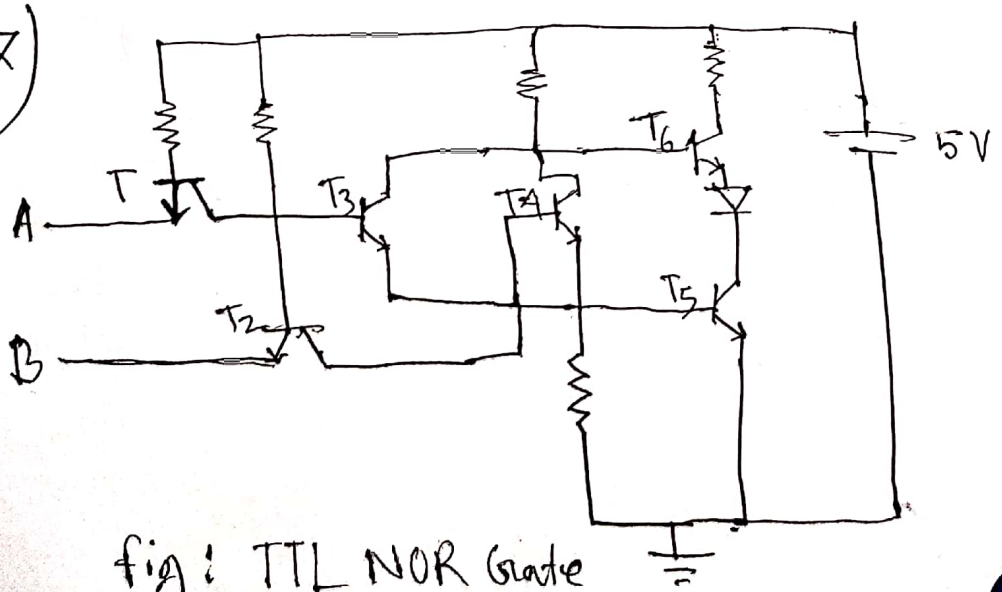

fig: TTL NOR Gate