CSE460: VLSI Design

Lecture 15

CMOS DC Characteristics

Contents

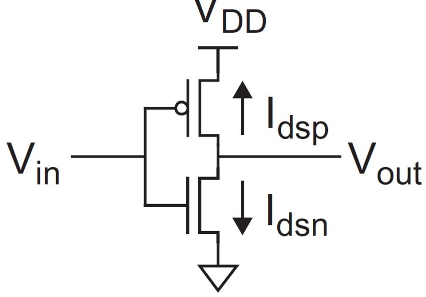
- CMOS Inverter DC Characteristics
- Noise Margin
- nMOS & pMOS Pass Transistor DC Characteristics

Static CMOS Inverter

A static CMOS inverter is built using a pMOS and an nMOS

DC Transfer function or DC response: V_{out} vs V_{in}

For the CMOS inverter shown:

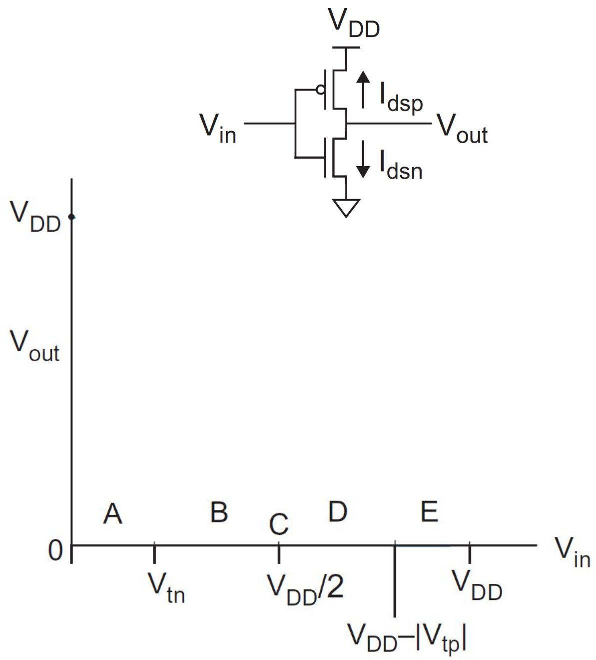


- $V_{in} = 0 \quad \Rightarrow \quad V_{out} = V_{DD}$
- $V_{in} = V_{DD} \quad \Rightarrow \quad V_{out} = 0$
- In between these 2 cases, V_{out} depends transistor current
- V_{out} vs V_{in} relationship can be found by setting $I_{dsn} = |I_{dsp}|$
- V_{out} vs V_{in} relationship can also be found via graphical solutions

CMOS Inverter DC Response

CMOS Inverter DC response can be determined as:

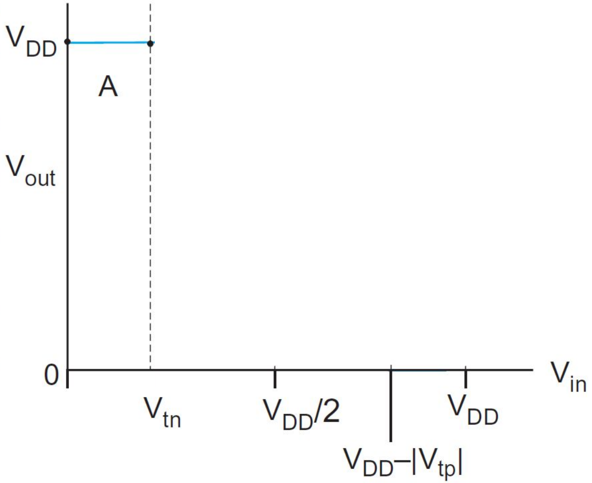
1. Divide the input into 5 different regions:
    a. **A**: $0 \leq \boldsymbol{V_{in}} < V_{tn}$
    b. **B**: $V_{tn} \leq \boldsymbol{V_{in}} < V_{DD}/2$
    c. **C**: $\boldsymbol{V_{in}} = V_{DD}/2$
    d. **D**: $V_{DD}/2 < \boldsymbol{V_{in}} \leq V_{DD} - |V_{tp}|$
    e. **E**: $\boldsymbol{V_{in}} > V_{DD} - |V_{tp}|$
2. Determine the operating regions of the devices
    a. Cutoff, Linear or Saturation?
3. Approximate $\boldsymbol{V_{out}}$ at **A**, **B**, **C**, **D** & **E** regions depending on the **pMOS** and **nMOS** *operating regions*



CMOS Inverter DC response

Region A

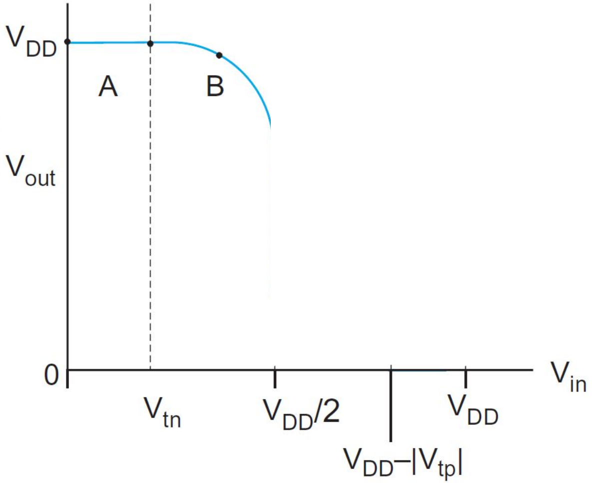
Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp} \rvert$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cutoff	linear	$V_{out} = 0$



CMOS Inverter DC response

Region B

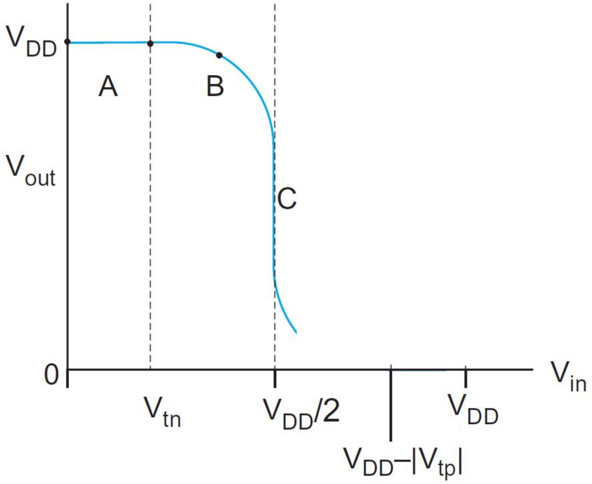
Region	Condition	p-device	n-device	Output
A	$0 \leq V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \leq V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \leq V_{DD} - \lvert V_{tp} \rvert$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cutoff	linear	$V_{out} = 0$



CMOS Inverter DC response

Region C

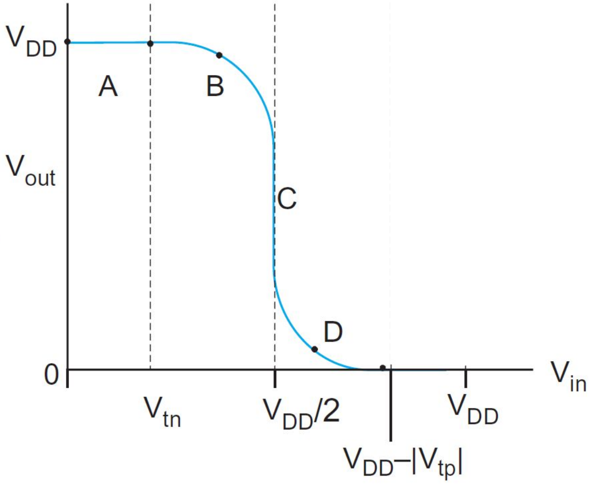
Region	Condition	p-device	n-device	Output
A	$0 \leq V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \leq V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \leq V_{DD} - \lvert V_{tp} \rvert$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cutoff	linear	$V_{out} = 0$



CMOS Inverter DC response

Region D

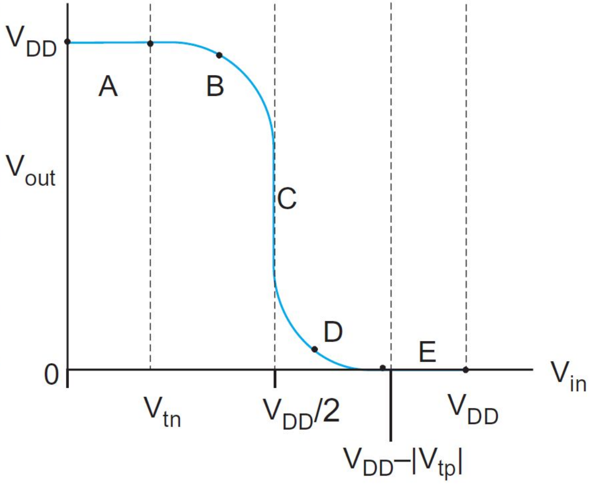
Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp} \rvert$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cutoff	linear	$V_{out} = 0$



CMOS Inverter DC response

Region E

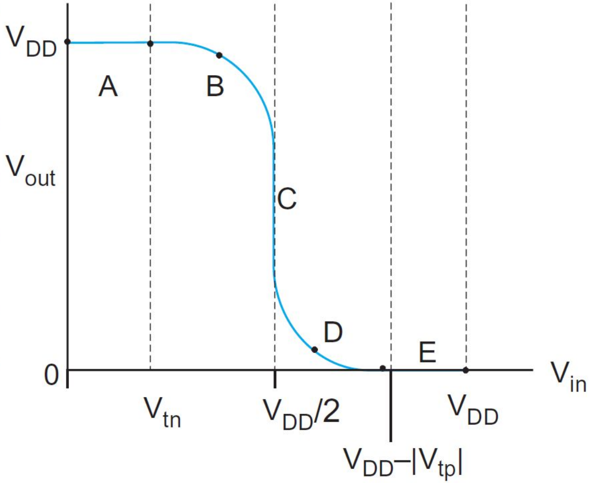
Region	Condition	p-device	n-device	Output
A	$0 \leq V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \leq V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \leq V_{DD} - \lvert V_{tp} \rvert$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cutoff	linear	$V_{out} = 0$



CMOS Inverter DC response

Complete $\boldsymbol{V_{out}}$ vs $\boldsymbol{V_{in}}$

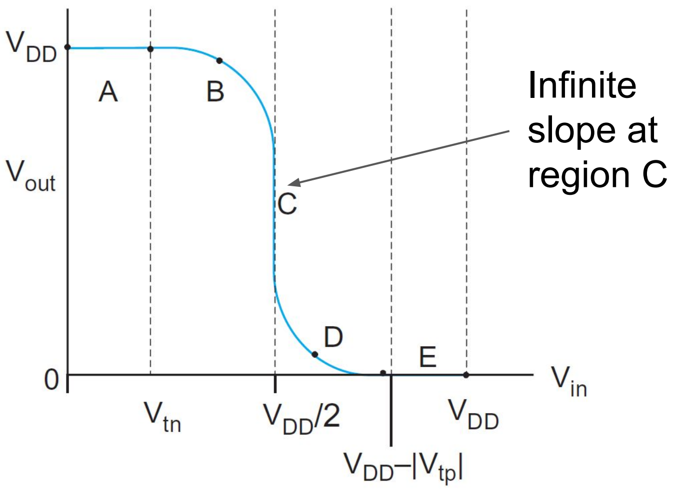
Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp} \rvert$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cutoff	linear	$V_{out} = 0$

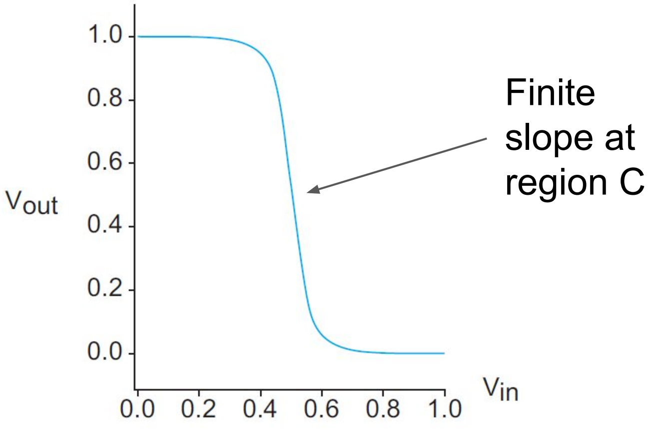


Practical CMOS Inverter DC response

In reality, the sharp change at region C is not that sharp and has finite slope

- Theoretical inverter DC response vs Practical inverter DC response

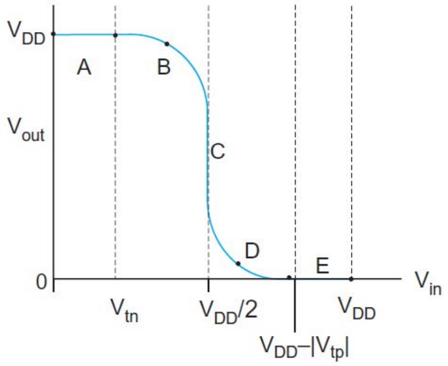




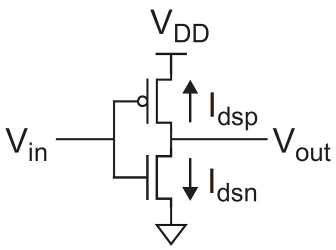
Supply Current

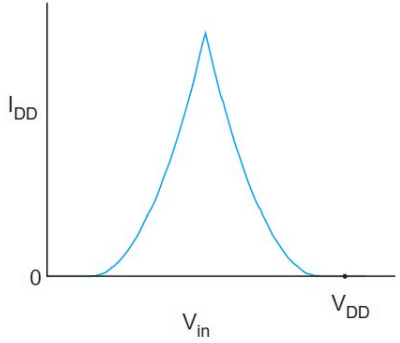
If $I_{DD} = I_{dsn} = |I_{dsp}|$ is the supply current drawn from V_{DD}

- I_{DD} is non-zero in regions B, C & D
- I_{DD} is zero in regions A & E



Region	Condition	p-device	n-device
A	$0 \le V_{in} < V_{tn}$	linear	cutoff
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated
C	$V_{in} = V_{DD}/2$	saturated	saturated
D	$V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp} \rvert$	saturated	linear
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cutoff	linear





Power Consumption

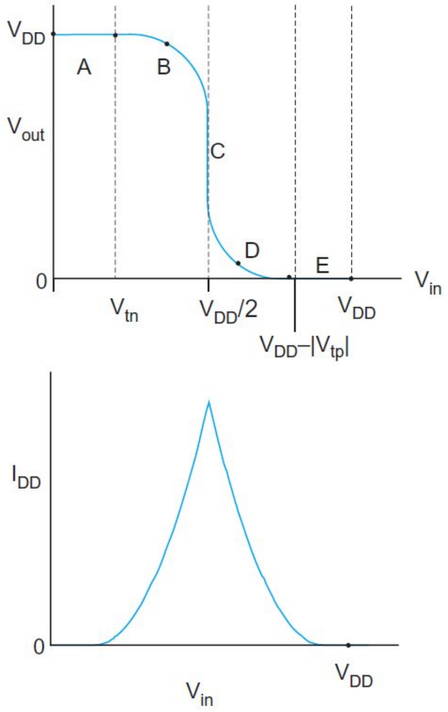
If $I_{DD} = I_{dsn} = |I_{dsp}|$ is the current drawn from supply V_{DD}

- I_{DD} is non-zero in regions B, C & D
- I_{DD} is zero in regions A & E

That is why we always try to work with strong signals

- A strong 0 falls in the region A where $I_{DD} \approx 0$
- A strong 1 falls in the region E where $I_{DD} \approx 0$

$I_{DD} \approx 0$ or low implies <u>low power consumption</u>!



Power Consumption

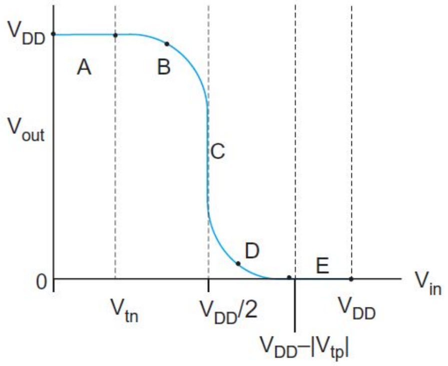
If $I_{DD} = I_{dsn} = |I_{dsp}|$ is the current drawn from supply V_{DD}

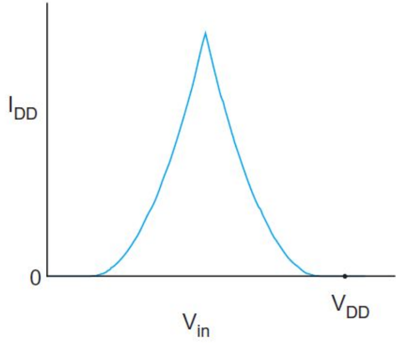
- I_{DD} is non-zero in regions B, C & D
- I_{DD} is zero in regions A & E

That is also why we try to avoid degraded signals

- A degraded 0 falls in the region B/C where $I_{DD} \neq 0$
- A degraded 1 falls in the region D/C where $I_{DD} \neq 0$

$I_{DD} \neq 0$ or high implies <u>high power consumption</u>!





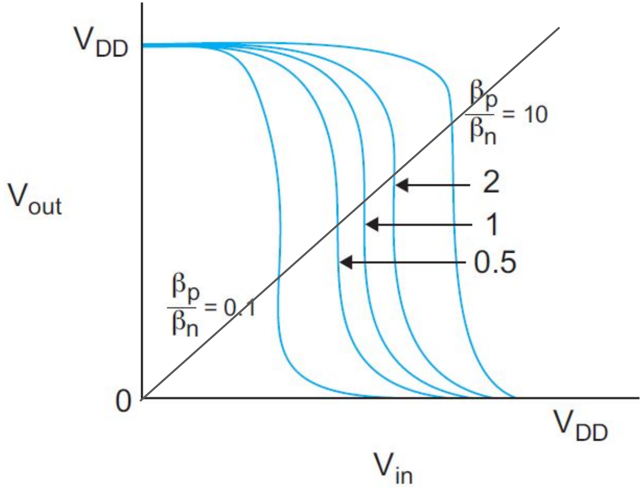
Beta Ratio Effects

The crossover point, where $\boldsymbol{V_{in} = V_{out}}$ is called the input threshold, $\boldsymbol{V_{inv}}$

For $\boldsymbol{\beta_p = \beta_n}$, the inverter threshold voltage, $\boldsymbol{V_{inv} = V_{DD}/2}$

$\boldsymbol{\beta_p / \beta_n}$ is called the beta ratio; $\boldsymbol{r = \beta_p / \beta_n}$

- $\boldsymbol{r = 1}$ ⇒ inverter is un-skewed
- $\boldsymbol{r > 1}$ ⇒ inverter is HI-skewed
- $\boldsymbol{r < 1}$ ⇒ inverter is LO-skewed



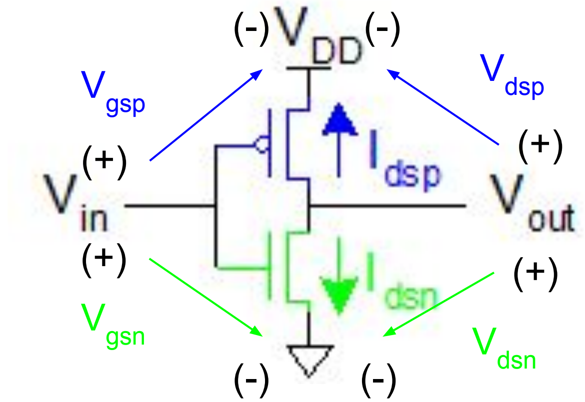
Thus, by changing $\boldsymbol{r}$ we can shift the response!

Beta Ratio Effects for a Static CMOS Inverter

We would like to know how V_{inv} changes for a CMOS inverter as we change r

For the CMOS inverter shown:

- $V_{gsp} = V_{in} - V_{DD}$
- $V_{dsp} = V_{out} - V_{DD}$
- $V_{gsn} = V_{in} - 0 = V_{in}$
- $V_{dsn} = V_{out} - 0 = V_{out}$



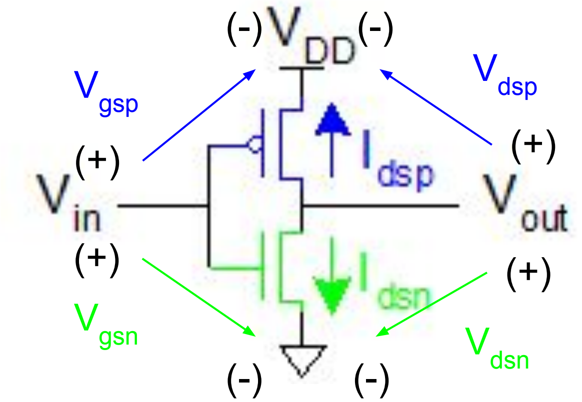
Assume: $V_{tp} = -V_{tn}$

Beta Ratio Effects for a Static CMOS Inverter

For βp ≠ βn, we can calculate the inverter threshold voltage by setting $\boldsymbol{V_{in} = V_{inv}}$

1. In region C, both pMOS & nMOS are saturated
2. So the nMOS and pMOS currents are:
- $\boldsymbol{I_{dsp} = \beta_p(V_{gsp} - V_{tp})^2/2 = \beta_p(V_{inv} - V_{DD} - V_{tp})^2/2}$
- $\boldsymbol{I_{dsn} = \beta_n(V_{gsn} - V_{tn})^2/2 = \beta_n(V_{inv} - V_{tn})^2/2}$
3. Set the currents $\boldsymbol{I_{dsp} = -I_{dsn}}$
4. Solve for $\boldsymbol{V_{inv}}$:

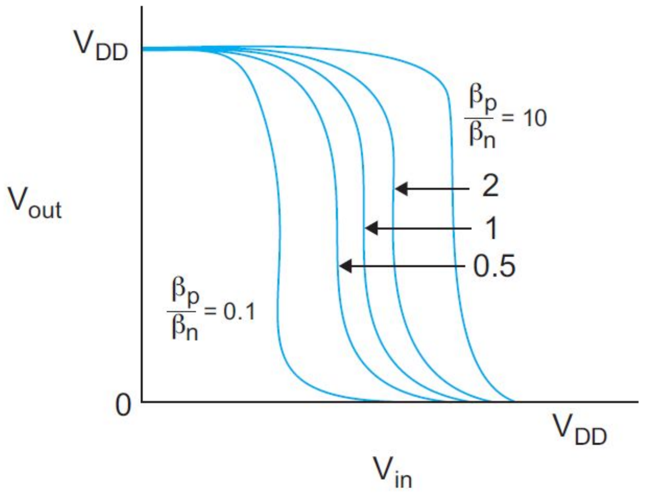
$$V_{\text{inv}} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{1}{r}}}{1 + \sqrt{\frac{1}{r}}}$$



Beta Ratio Effects

So thus for $\beta_p \neq \beta_n$, we can calculate the inverter threshold voltage as a function of "***r***", where ***r* = *β*$_p$ / *β*$_n$**

$$V_{\text{inv}} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{1}{r}}}{1 + \sqrt{\frac{1}{r}}}$$



Other CMOS Gates

DC transfer characteristics of other static CMOS gates can be understood by collapsing the gates into an equivalent inverter

- **Series transistors** can be viewed as a single transistor of greater length
- If only one of several **parallel transistors** is ON, the other transistors can be ignored
- If several **parallel transistors** are ON, the collection can be viewed as a single transistor of greater width

Noise Margin (Noise Immunity)

Noise margin is closely related to the DC voltage characteristics

Helps determine the allowable noise voltage on the input of a gate so that the output will not be corrupted

The specification most commonly used to describe noise margin uses two parameters:

1. The LOW noise margin, NM_L
2. The HIGH noise margin, NM_H

Noise Margin

Voltage definitions:

V_{IH} = minimum HIGH input voltage

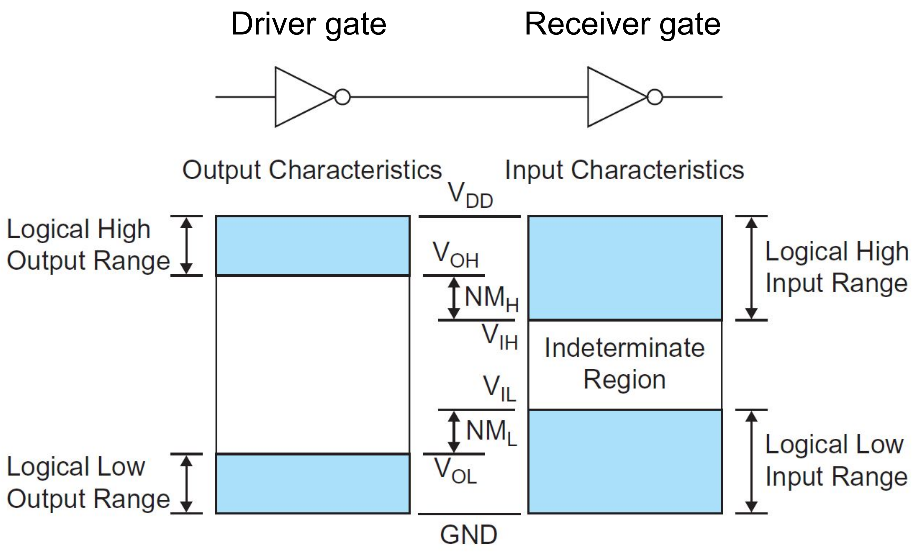
V_{IL} = maximum LOW input voltage

V_{OH} = minimum HIGH output voltage

V_{OL} = maximum LOW output voltage

NM_L = The LOW noise margin

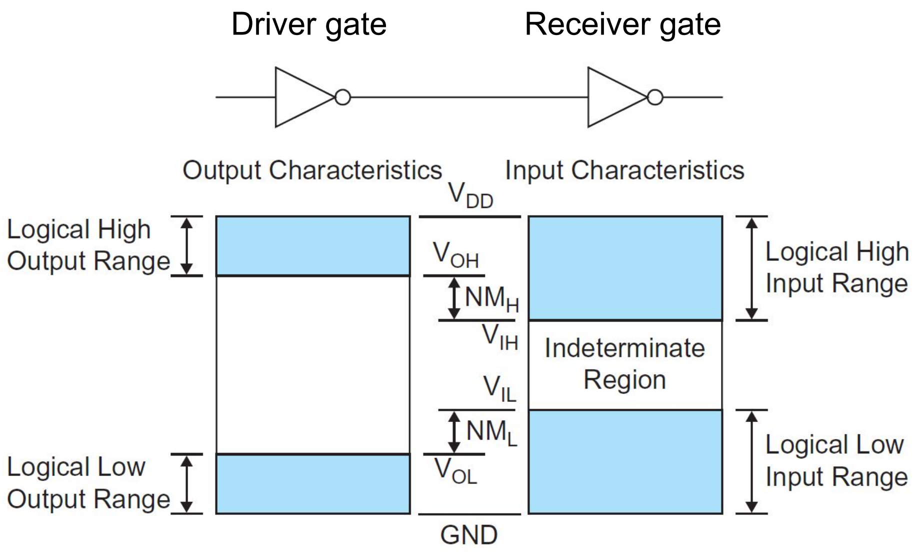
NM_H = The HIGH noise margin



Low Noise Margin

- **The LOW noise margin (*NM_L*)** is the difference in maximum LOW input voltage recognized by the receiving gate and the maximum LOW output voltage produced by the driving gate

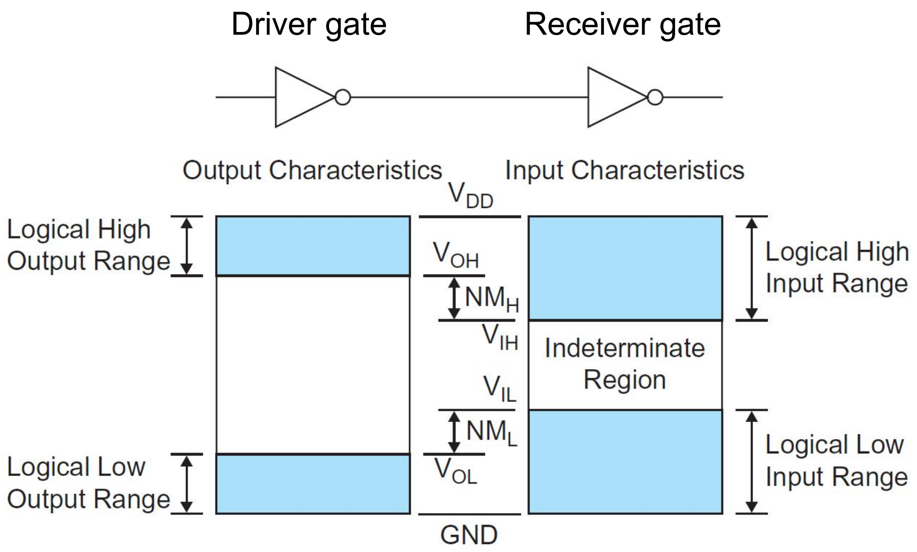
$$NM_L = V_{IL} - V_{OL}$$



High Noise Margin

- **The HIGH noise margin (NM_H)** is the difference between the minimum HIGH output voltage of the driving gate and the minimum HIGH input voltage recognized by the receiving gate

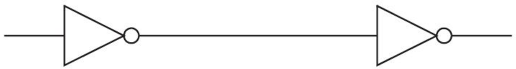
$$NM_H = V_{OH} - V_{IH}$$

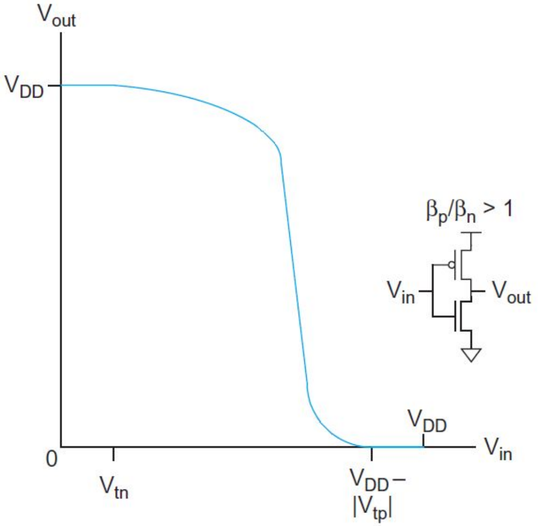


Selecting V_{IL}, V_{IH}, V_{OL} & V_{OH}

How to choose the logic levels $\boldsymbol{V_{IL}}$, $\boldsymbol{V_{IH}}$, $\boldsymbol{V_{OL}}$ **&** $\boldsymbol{V_{OH}}$ such that the noise margins $\boldsymbol{NM_L}$ **&** $\boldsymbol{NM_H}$ are maximized?

- Use the DC transfer characteristics!

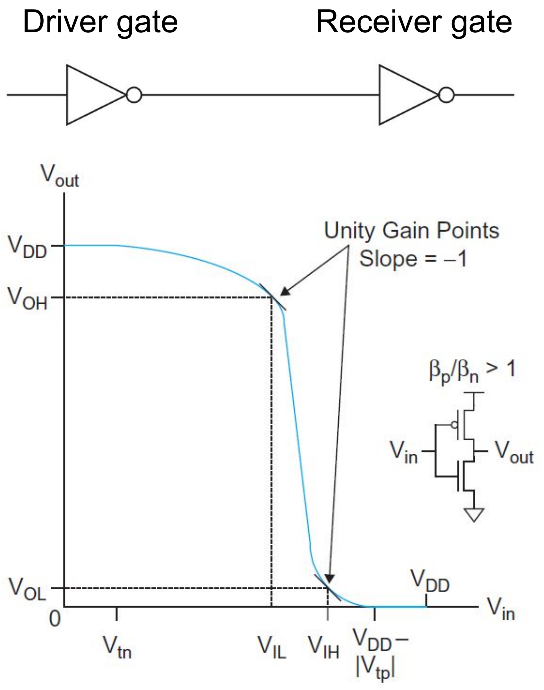




Selecting V_{IL}, V_{IH}, V_{OL} & V_{OH}

How to choose the logic levels $\boldsymbol{V_{IL}}$, $\boldsymbol{V_{IH}}$, $\boldsymbol{V_{OL}}$ **&** $\boldsymbol{V_{OH}}$ such that the noise margins $\boldsymbol{NM_L}$ **&** $\boldsymbol{NM_H}$ are maximized?

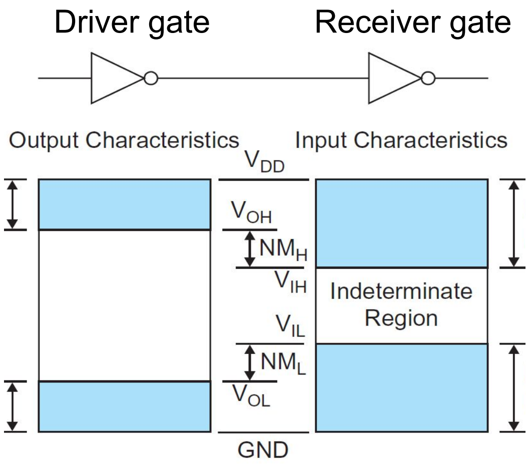
- Use the DC transfer characteristics!
- Logic levels are defined at the unity gain point where the slope is –1
- This gives a conservative bound on the worst case static noise margin



Selecting V_{IL}, V_{IH}, V_{OL} & V_{OH}

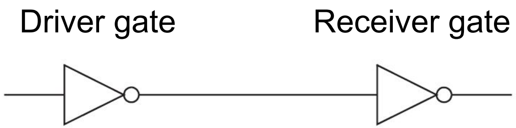
Logic levels of typical 5 V and 3.3 V logic families

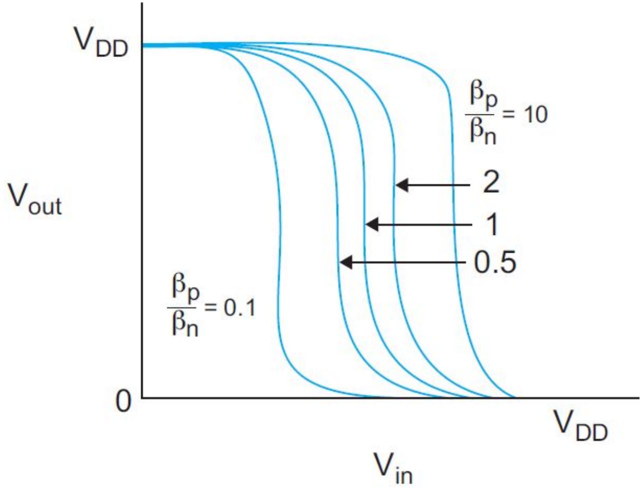
Logic Family	V_{DD}	V_{IL}	V_{IH}	V_{OL}	V_{OH}
TTL	5 (4.75–5.25)	0.8	2.0	0.4	2.4
CMOS	5 (4.5–6)	1.35	3.15	0.33	3.84
LVTTL	3.3 (3–3.6)	0.8	2.0	0.4	2.4
LVCMOS	3.3 (3–3.6)	0.9	1.8	0.36	2.7



Noise Margin: Summary

- **NM_L or NM_H too small**: the gate may be disturbed by noise that occurs on the inputs
- **An unskewed gate has equal noise margins**: which maximizes immunity to arbitrary noise sources
- **If a gate sees more noise in the high or low input state**: the gate can be skewed to improve that noise margin at the expense of the other

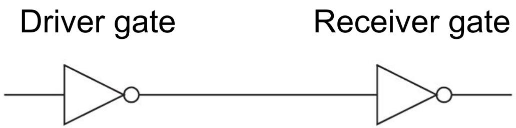


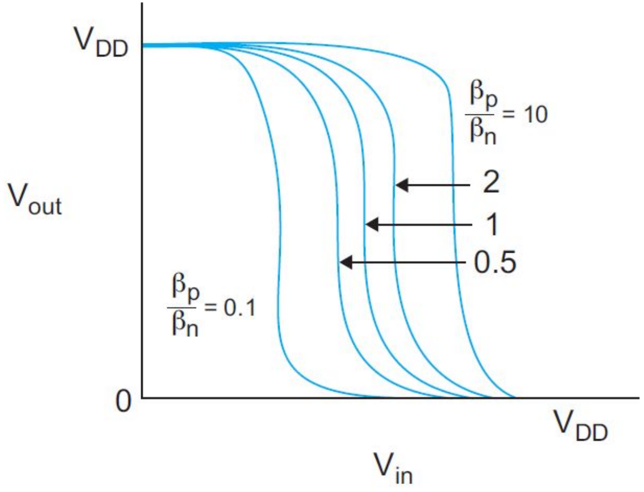


Noise Margin: Summary

- **Noise sources tend to scale with the supply voltage**: so noise margins are best given as a fraction of the supply voltage; for example $0.3V_{DD}$

  A noise margin of 0.4 V is quite comfortable in a 1.8 V process, but marginal in a 5 V process





Pass Transistor DC Characteristics

Recall from our previous lectures that

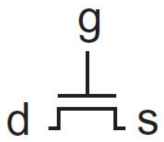
- **nMOS** transistors pass ‘0’s well but ‘1’s poorly
- **pMOS** transistors pass ‘1’s well but ‘0’s poorly

We are now better prepared to define how “poorly”

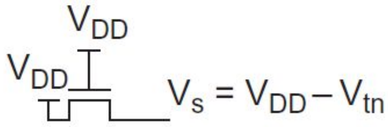
nMOS Pass Transistor DC Characteristics

To keep an nMOS transistor ON, we need

- $V_{gs} \geq V_{tn}$
- $\Rightarrow V_g - V_s \geq V_{tn}$
- $\Rightarrow V_s \leq V_g - V_{tn}$
- $\Rightarrow \mathbf{V_{s(max)} = V_g - V_{tn}}$



nMOS Pass Transistor DC Characteristics



To keep an nMOS transistor ON, we need

- $\mathbf{V_{s(max)} = V_g - V_{tn}}$

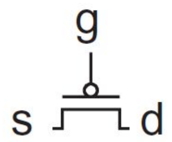
nMOS transistors passing '1' ($\mathbf{V_{in} = V_{DD}}$; $\mathbf{V_{out} = ?}$)

- Gate is connected to V_{DD}: $V_g = V_{DD}$
- Current flowing from drain to source
- $V_{in} = V_d = V_{DD}$; $V_{out} = V_s = ?$
- But we know $V_{s(max)} = V_g - V_{tn} \Rightarrow \mathbf{V_{out(max)} = V_{DD} - V_{tn}}$

nMOS transistors attempting to pass a '1' never pass above $\mathbf{V_{DD} - V_{tn}}$

pMOS Pass Transistor DC Characteristics

To keep a pMOS transistor ON, we need

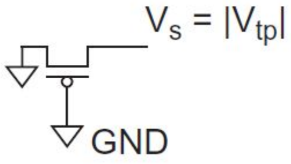


- $V_{sg} \geq |V_{tp}|$
- $\Rightarrow V_s - V_g \geq |V_{tp}|$
- $\Rightarrow V_s \geq V_g + |V_{tp}|$
- $\Rightarrow \mathbf{V_{s(min)} = V_g + |V_{tp}|}$

pMOS Pass Transistor DC Characteristics

To keep a pMOS transistor ON, we need

- $\mathbf{V_{s(min)} = V_g + |V_{tp}|}$



pMOS transistors passing ‘0’ (**V_{in} = 0; V_{out} = ?**)

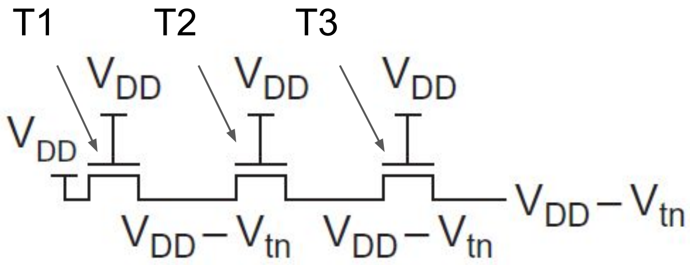
- Gate is connected to GND: $V_g = 0$
- Current flowing from source to drain
- $V_{in} = V_d = 0$; $V_{out} = V_s = ?$
- But we know $V_{s(min)} = V_g + |V_{tp}| \Rightarrow V_{out(min)} = |V_{tp}|$

pMOS transistors attempting to pass a ‘0’ never pass lower than $|V_{tp}|$

nMOS Pass Transistor DC Characteristics

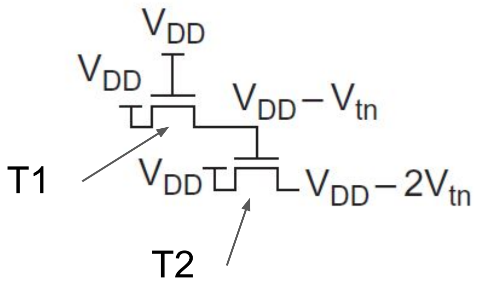
Series nMOS transistors passing '1' (V_{DD})

- If all of the transistors have gates tied to V_{DD}
- $V_{g(T1)} = V_{g(T2)} = V_{g(T3)} = V_{DD}$
- $V_{in(T1)} = V_{DD}$; $V_{out(T3)} = ?$



1. <u>Output of Transistor T1</u>: $V_{out(max),\,T1} = V_{g(T1)} - V_{tn(T1)} = V_{DD} - V_{tn}$
2. <u>Output of Transistor T2</u>: $V_{out(max),\,T2} = V_{g(T2)} - V_{tn(T2)} = V_{DD} - V_{tn}$
3. <u>Output of Transistor T3</u>: $V_{out(max),\,T3} = V_{g(T3)} - V_{tn(T3)} = V_{DD} - V_{tn}$

nMOS Pass Transistor DC Characteristics



nMOS transistor driven by degraded output

- If T1 transistor has gate tied to V_{DD}
- $V_{g(T1)} = V_{DD}$; $V_{in} = V_{DD}$; $V_{out} = ?$

Output of Transistor T1: $V_{out(max),\,T1} = V_{g(T1)} - V_{tn(T1)} = V_{DD} - V_{tn}$

- Output of transistor T1 is now driving the gate of transistor T2
- T2 transistor has gate tied to $V_{DD} - V_{tn}$
- $V_{g(T2)} = V_{DD} - V_{tn}$; $V_{in} = V_{DD}$; $V_{out} = ?$

Output of Transistor T2: $V_{out(max),\,T2} = V_{g(T2)} - V_{tn(T2)} = (V_{DD} - V_{tn}) - V_{tn} = V_{DD} - 2V_{tn}$

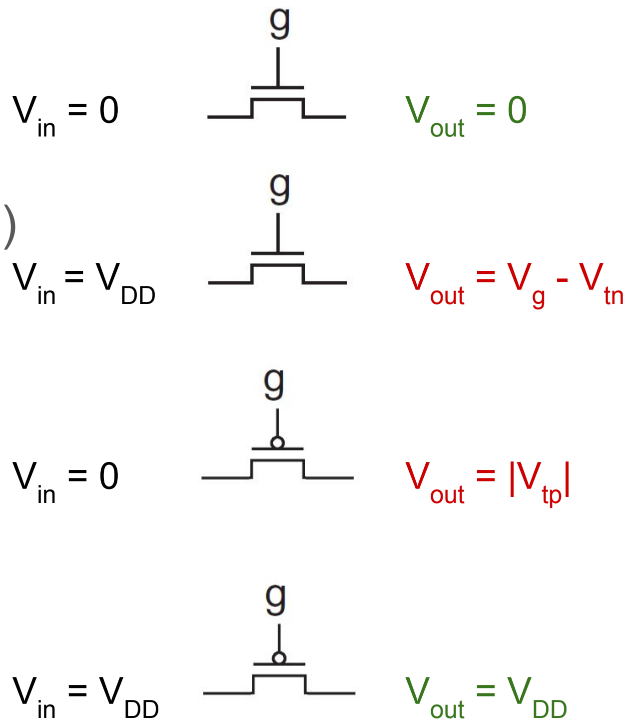
Pass Transistor DC Characteristics: Summary

nMOS pass transistor

- V_{in} = GND ⇒ V_{out} = GND (strong 0)
- $V_{in} = V_{DD}$ ⇒ $V_{out(max)} = V_g - V_{tn}$ (degraded 1)

pMOS pass transistor

- V_{in} = GND ⇒ $V_{out(min)} = |V_{tp}|$ (degraded 0)
- $V_{in} = V_{DD}$ ⇒ $V_{out} = V_{DD}$ (strong 1)



Pass Transistor DC Characteristics: Summary

- nMOS/pMOS pass transistors sometimes produce degraded outputs
- The loss is sometimes called a threshold drop
- In old processes where V_{DD} was high and Vt was a small fraction of V_{DD}, the threshold drop was tolerable
- In modern processes V_{DD} is significantly lower and Vt is almost ⅓ of V_{DD}, the threshold drop can produce an invalid or marginal logic at the output

To solve this problem we use CMOS transmission gates

Thank You!