

Quiz Solution

Saturday, May 22, 2021 8:29 PM

Slot 1

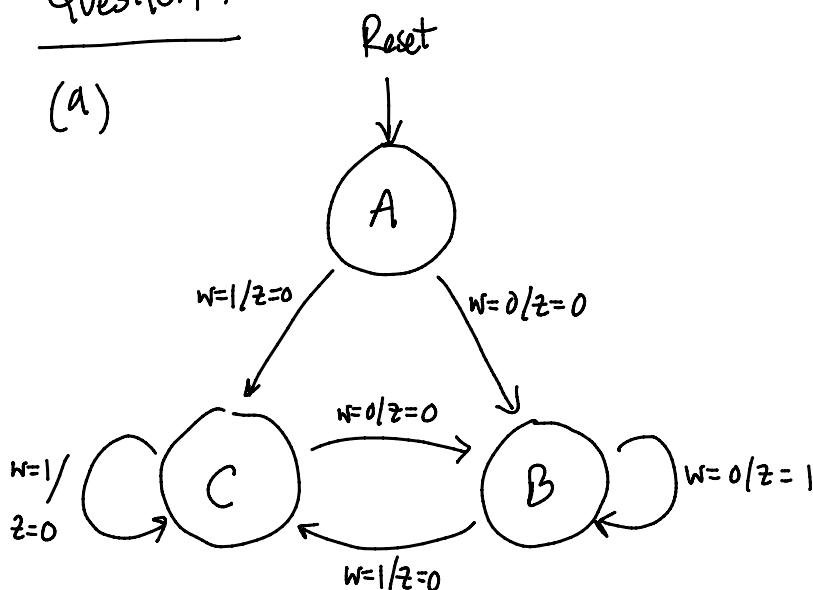
Time: 35 minutes for answering + 10 minutes for PDF preparation = 45 minutes

Full marks: 15

- A mealy-type FSM that has an input w and an output z. The machine is a sequence detector, that produces $z = 1$ when two consecutive values in w are either 00 or 11.
- a) Draw the state diagram (clearly mark your reset and transitions) [5]
- b) Derive the complete state assigned table using one hot encoding [5]
2. Why do we need to dope pure silicon? Briefly explain 2 methods for doping a pure silicon in the CMOS fabrication process. [5]

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Question 1



(b)

| Present state | Next state | | Output | |
|-------------------------------|-------------------------|-------------------------|--------|-----|
| | w=0 | w=1 | w=0 | w=1 |
| $\bar{Y}_3\bar{Y}_2\bar{Y}_1$ | $\bar{Y}_3\bar{Y}_2Y_1$ | $Y_3\bar{Y}_2\bar{Y}_1$ | z | z |
| (A) 001 | (B) 010 | (C) 100 | 0 | 0 |
| (B) 010 | (B) 010 | (C) 100 | 1 | 0 |
| (C) 100 | (B) 010 | (C) 100 | 0 | 1 |

state assigned table w/ one hot encoding.

(derive the next state and output equations; and compare the complexity of the comb. circuit with other encoding schemes.)

Question 2

Because pure silicon has very low conductivity at room temperature due to its electronic lattice structure.

2 ways to dope silicon: ① ion implantation

② diffusion

Slot 2

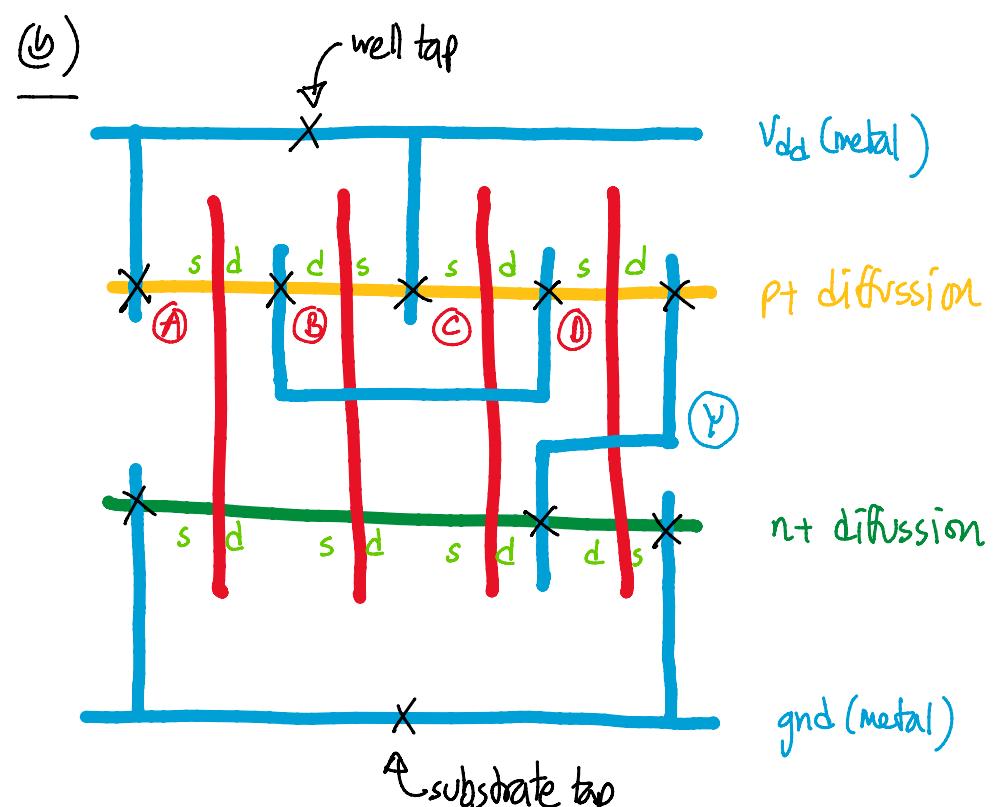
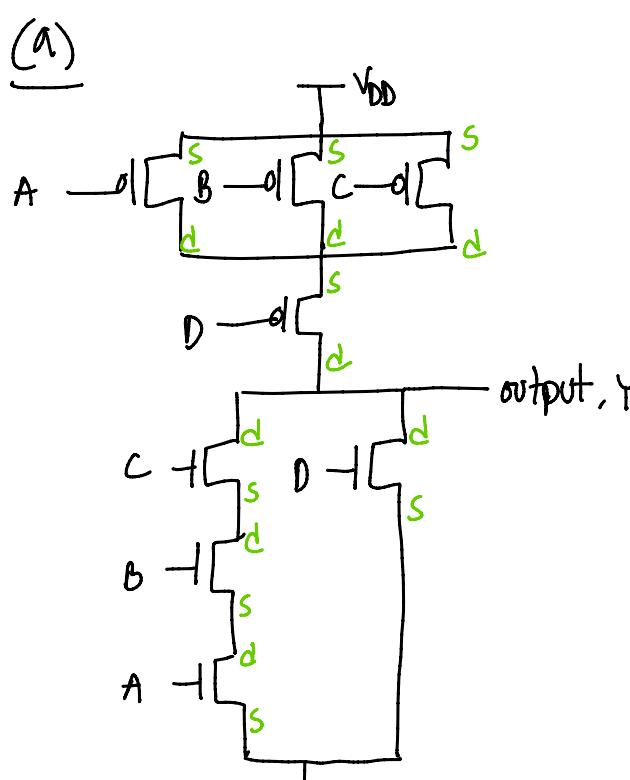
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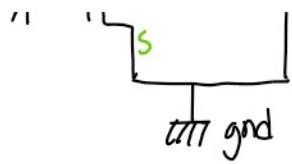
Full marks: 15

- Consider the design of a CMOS compound gate computing the function, $F = ABC + D$
 - sketch the transistor level schematic (clearly mark the source and drain terminals of each transistor) [3]
 - sketch a stick diagram of the circuit in (a) [5]
 - estimate the width, height and area from the stick diagram, for a 320nm process [2]
- Why are well and substrate taps necessary? For a CMOS inverter in p-well process (fill in the blanks) [5]
 - the well should be connected to _____
 - the substrate should be connected to _____

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Question 1





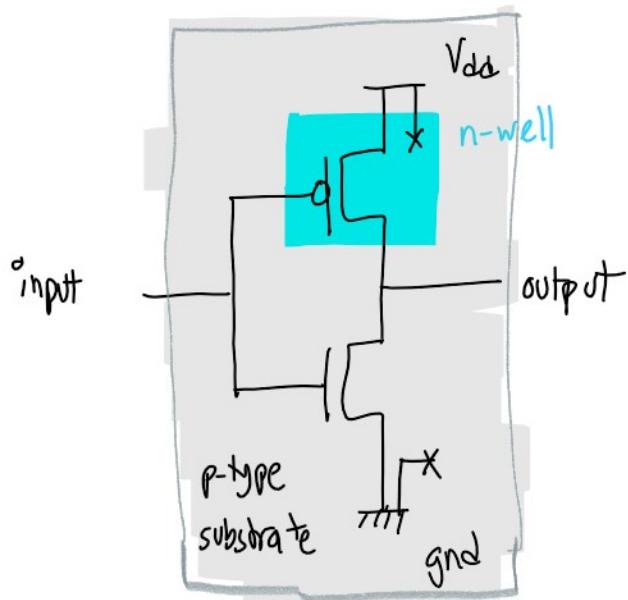
(c) 320 nm process. $\therefore f = 320 \text{ nm}$. $\lambda = f/2 = 160 \text{ nm}$.

height = 6 wiring tracks $\approx 6 \times 8\lambda$

width = 5 wiring tracks $\approx 5 \times 8\lambda$

area = height \times width $= 6 \times 8 \times 5 \times 8 \times \lambda^2$

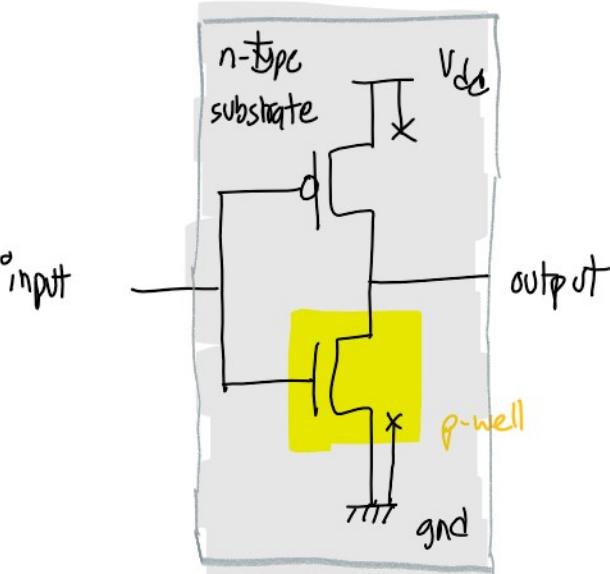
Question 2



CMOS inverter in n-well process

PMOS body \rightarrow n-well \rightarrow connected to V_{DD}

NMOS body \rightarrow p-substrate \rightarrow connected to gnd



CMOS inverter in p-well process

PMOS body \rightarrow n-substrate \rightarrow connected to V_{DD}

NMOS body \rightarrow p-well \rightarrow connected to gnd.

Why? Always keep the body-source/drain junction reverse biased.

If the body is n-type, connect it to the maximum voltage available (V_{DD})

If the body is p-type, connect it to the minimum voltage available (gnd)

Slot 3

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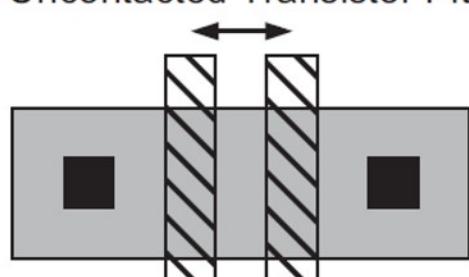
Full marks: 15

1. Briefly explain the following design rules for CMOS fabrication: [6]

- a) the poly-silicon width and spacing
- b) the metal width and spacing
- c) the dimensions of contact

2. The uncontacted transistor pitch is defined as the distance between the midpoints of two transistors when there are *no contacts in between them*, and the contacted transistor pitch is defined as the distance between the midpoints of two transistors when there is *a contact in between them*. For the following diagram below (legend: hatched white = pol-silicon, black filled = contacts, gray filled = diffusion):

Uncontacted Transistor Pitch

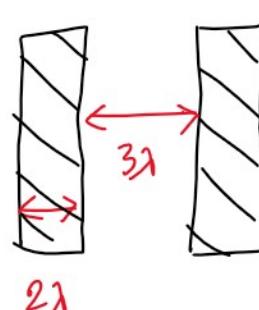


Contacted Transistor Pitch



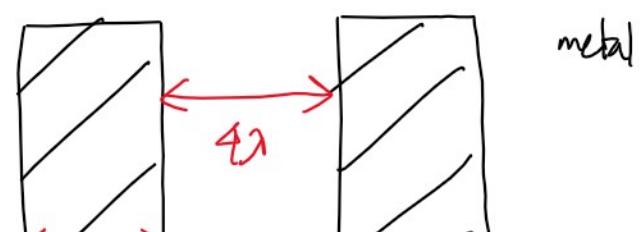
Question 1

(a)

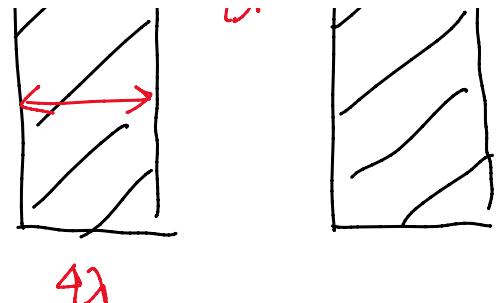
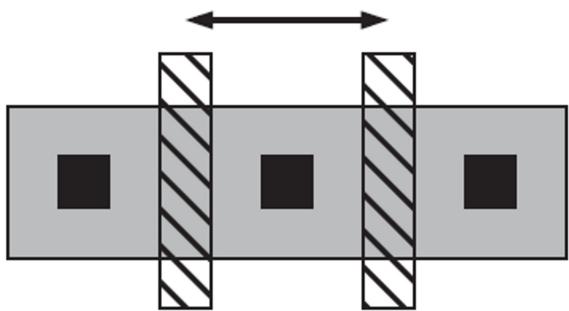


polysilicon

(b)



metal

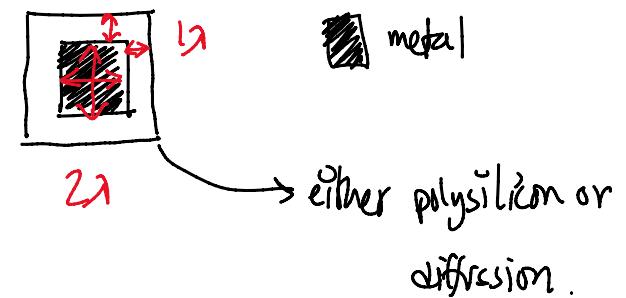


In addition to the design rules covered in class, 1 additional rule is that the minimum poly-silicon to contact spacing should be 2λ .

- a) calculate the minimum uncontacted transistor pitch [4]
- b) calculate the minimum contacted transistor pitch [5]

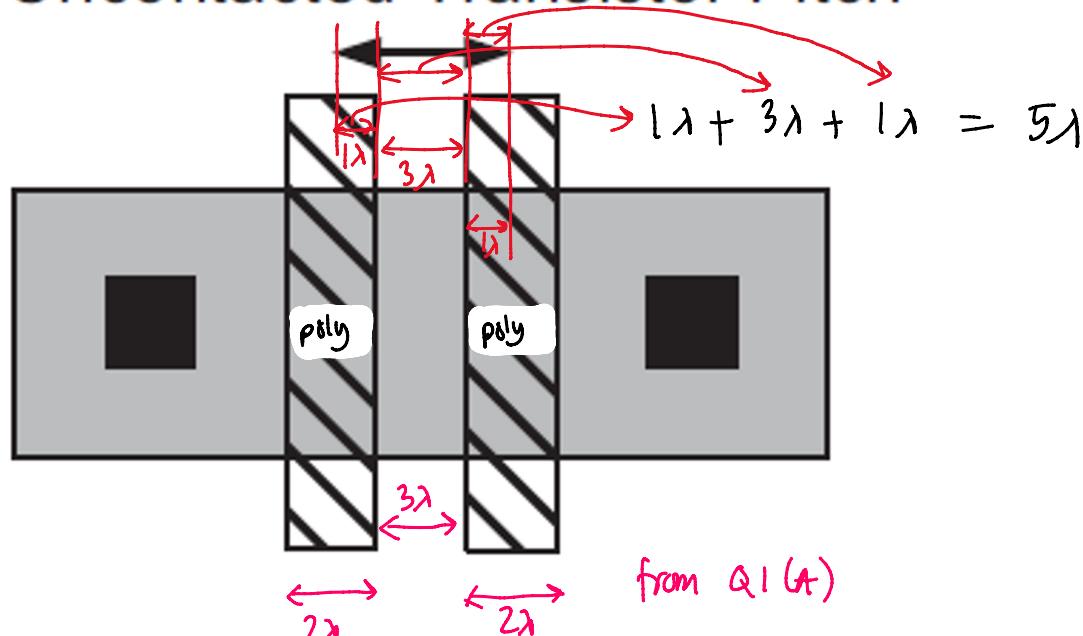
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(c)



(b)

Uncontacted Transistor Pitch



Contacted Transistor Pitch

