

Problem 1:

$$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

a)

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Here, AND, OR and NOT logic operations are performed in the circuit. So, the output Y.

b) I picked randomly 2 time instances
20 ns and 30 ns

For 20 ns and 30 ns,

Time Instances	A	B	C	Y
20	0	1	1	0
30	1	0	1	0

After crosschecking, it is clearly seen that outputs matched with truth table.

c) After assigning random values to input pins, I picked two time instances 10 ns and 20 ns.

Time Instances	A	B	C	Y
10	0	0	1	1
20	1	0	0	1

We can see, outputs matched with fourth table.

d) If we modify the equation for only NAND gates, then it will be

$$\overline{(\overline{A} \cdot \overline{A} \cdot \overline{B} \cdot \overline{B} \cdot C)} \cdot \overline{(\overline{A} \cdot \overline{A} \cdot B \cdot \overline{C} \cdot \overline{C})} \cdot \overline{(A \cdot \overline{B} \cdot \overline{B} \cdot \overline{C} \cdot C)} \cdot \overline{(A \cdot B \cdot C)}$$

Now, the logic circuit of this equation can be made using only NAND gates.

Entity	Combinational ALUTs	ALMs	Dedicated
Stratix II: AUTO			
pro...	1 (1)	1 (1)	0 (0)

Hierarchy Files Design Units

Tasks

Flow: Compilation

Task	Time
Compile Design	00:00:34
Analysis & Synthesis	00:00:05
Fitter (Place & Route)	00:00:13
Assembler (Generate programming files)	00:00:10
Classic Timing Analysis	00:00:03
EDA Netlist Writer	00:00:03
Program Device (Open Programmer)	

```

1 module problem1_18301276 (y,a,b,c);
2     input a,b,c;
3     output y;
4
5     assign anot = ~a;
6     assign bnot = ~b;
7     assign cnot = ~c;
8
9     assign p1 = anot & bnot & c;
10    assign p2 = anot & b & cnot;
11    assign p3 = a & bnot & cnot;
12    assign p4 = a & b & c;
13
14    assign y = p1 | p2 | p3 | p4;
15 endmodule
    
```

Type	Message
Info	Info: Using vector source file "E:/CSE460 Labs/Lab1/problem1_18301276/problem1_18301276.vwf"
Info	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Info: Simulation partitioned into 1 sub-simulations
Info	Info: Simulation coverage is 100.00 %
Info	Info: Number of transitions in simulation is 1840
Info	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (19) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

Message: 0 of 16 Location: Locate

For Help, press F1 Ln 1, Col 28 Idle NUM

Type here to search 30°C Mostly cloudy 12:50 PM 10/21/2021

Entity	Combinational ALUTs	ALMs	Dedicated
Stratix II: AUTO			
1 (1)	1 (1)	1 (1)	0 (0)

Task	Time
Compile Design	00:00:34
Analysis & Synthesis	00:00:05
Fitter (Place & Route)	00:00:13
Assembler (Generate programming files)	00:00:10
Classic Timing Analysis	00:00:03
EDA Netlist Writer	00:00:03
Program Device (Open Programmer)	

Compilation Report
Legal Notice
Flow Summary
Flow Settings
Flow Non-Default Global Se
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
EDA Netlist Writer

Flow Status	Successful - Thu Oct 21 12:38:39 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem1_18301276
Top-level Entity Name	problem1_18301276
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	1 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	4 / 343 (1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

Type	Message
Info	Info: Using vector source file "E:/CSE460 Labs/Lab1/problem1_18301276/problem1_18301276.vwf"
Info	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Info: Simulation partitioned into 1 sub-simulations
Info	Info: Simulation coverage is 100.00 %
Info	Info: Number of transitions in simulation is 1840
Info	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

Entity	Combinational ALUTs	ALMs	Dedicated
Stratix II: AUTO			
pro...	1 (1)	1 (1)	0 (0)

Task	Time
Compile Design	00:00:34
Analysis & Synthesis	00:00:05
Fitter (Place & Route)	00:00:13
Assembler (Generate programming files)	00:00:10
Classic Timing Analysis	00:00:03
EDA Netlist Writer	00:00:03
Program Device (Open Programmer)	

Simulation Report
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Flow Summary
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Simulator
Summary
Settings
Simulation Waveforms
Simulation Coverage
INI Usage
Messages

Info	Using vector source file "E:/CSE460 Labs/Lab1/problem1_18301276/problem1_18301276.vwf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 100.00 %
Info	Number of transitions in simulation is 81
Info	Quartus II Simulator was successful. 0 errors, 0 warnings

Entity	Combinational ALUTs	ALMs	Dedicated
Stratix II: AUTO	1 (1)	1 (1)	0 (0)

Hierarchy	Files	Design Units
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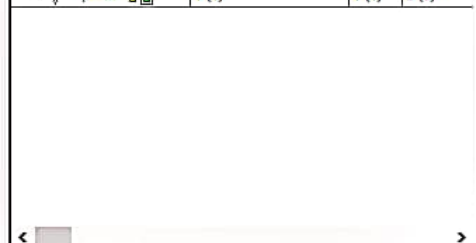
Tasks

Flow: Compilation

Task	Time
Compile Design	00:00:00
Analysis & Synthesis	00:00:00
Edit Settings	
View Report	
Analysis & Elaboration	
Partition Merge	
Netlist Viewers	
Design Assistant (Post-Mapping)	
I/O Assignment Analysis	
Early Timing Estimate	

Simulation Report
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Flow Summary
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Simulator
Summary
Settings
Simulation Waveforms
Simulation Coverage
INI Usage
Messages

Entity	Combinational ALUTs	ALMs	Dedicated
Stratix II: AUTO			
pro...	1 (1)	1 (1)	0 (0)



Task	Time
Compile Design	00:00:00
Analysis & Synthesis	00:00:00
Edit Settings	
View Report	
Analysis & Elaboration	
Partition Merge	
Netlist Viewers	
Design Assistant (Post-Mapping)	
I/O Assignment Analysis	
Early Timing Estimate	

```

1 module problem1_18301276 (y,a,b,c);
2     input a,b,c;
3     output y;
4
5     assign y = ~(~(a&a) & ~(b&b) & c) & ~(~(a&a) & b & ~(c&c)) & ~(a & ~(b&b) & ~(c&c)) & ~(a&b&c);
6 endmodule
    
```

Type	Message
Info	Info: Using vector source file "E:/CSE460 Labs/Lab1/problem1_18301276/problem1_18301276.vwf"
Info	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Info: Simulation partitioned into 1 sub-simulations
Info	Info: Simulation coverage is 93.33 %
Info	Info: Number of transitions in simulation is 75
Info	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

Entity	Combinational ALUTs	ALMs	Dedicated
Stratix II: AUTO	1 (1)	1 (1)	0 (0)

Task	Time
Compile Design	00:00:00
Analysis & Synthesis	00:00:00
Edit Settings	
View Report	
Analysis & Elaboration	
Partition Merge	
Netlist Viewers	
RTL Viewer	
State Machine Viewer	
Technology Map Viewer (Post)	

Compilation Report
Legal Notice
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
EDA Netlist Writer

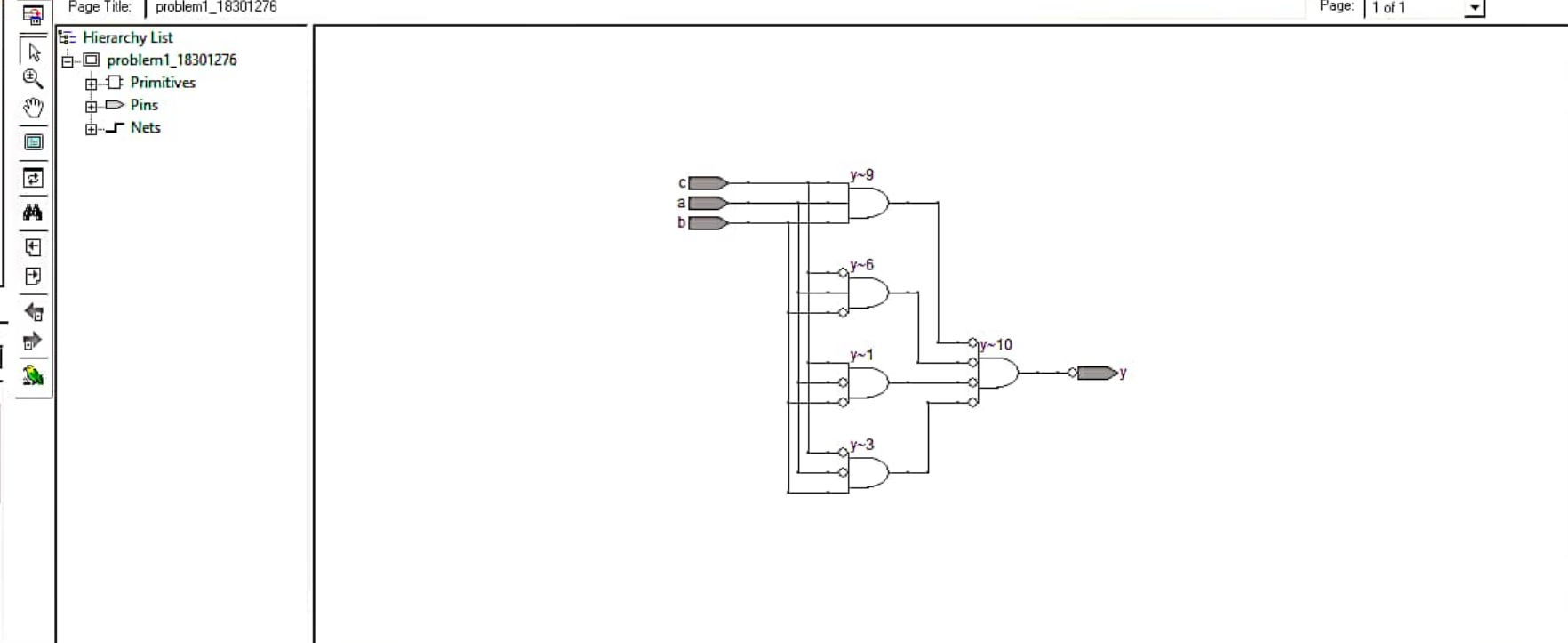
Flow Summary

Flow Status	Successful - Thu Oct 21 14:02:48 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem1_18301276
Top-level Entity Name	problem1_18301276
Family	Stratix II
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	1 / 12,480 (< 1 %)
Dedicated logic registers	0 / 12,480 (0 %)
Total registers	0
Total pins	4 / 343 (1 %)
Total virtual pins	0
Total block memory bits	0 / 419,328 (0 %)
DSP block 9-bit elements	0 / 96 (0 %)
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 2 (0 %)
Device	EP2S15F484C3
Timing Models	Final

Type	Message
Info	Number of transitions in simulation is 75
Info	Quartus II Simulator was successful. 0 errors, 0 warnings
Info	*****
Info	Running Quartus II Netlist Viewers Preprocess
Info	Command: quartus_rpp problem1_18301276 -c problem1_18301276 --netlist_type=sgate
Info	Quartus II Netlist Viewers Preprocess was successful. 0 errors, 0 warnings

Entity	Combinational ALUTs	ALMs	Dedicated
Stratix II: AUTO			
pro...	1 (1)	1 (1)	0 (0)

Task	Time
Compile Design	00:00
Analysis & Synthesis	00:00
Edit Settings	
View Report	
Analysis & Elaboration	
Partition Merge	
Netlist Viewers	
RTL Viewer	
State Machine Viewer	
Technology Map Viewer (Post)	



Type	Message
Info	Number of transitions in simulation is 75
Info	Quartus II Simulator was successful. 0 errors, 0 warnings
Info	*****
Info	Running Quartus II Netlist Viewers Preprocess
Info	Command: quartus_rpp problem1_18301276 -c problem1_18301276 --netlist_type=sgate
Info	Quartus II Netlist Viewers Preprocess was successful. 0 errors, 0 warnings