CS125 Digital Design

Tutorial #4
Basic Computer Complete Design

1) Consider the basic computer whose instruction set is described by Table (1) below. If the initial content of the AC is $(1234)_{16}$ and that of PC is $(52B)_{16}$ and the memory contents in hexadecimal are as follow:

Address	52B	A11	C54
Content	9A11	C54	4321

Show the content of each register (in hexadecimal) to fetch and execute the given instruction by completing the following table:

Micro instructions	Phase	Time	Hexadecimal content of the registers					
			PC	AC	AR	DR	IR	SC
initial values								
	Fetch	**T0**						
		T1						
	Decode	**T2**						
	Address	**T3**						
	Execute	**T4**						
		T5						

2) Consider the basic computer whose instruction set is described by Table (1) below. If the initial content of the AC is AD2F and that of PC is B3C and the memory contents are as follow:

Address	B3C	E23	E3F
Content	AE23	0E3F	ABCD

Show the content of each register (in hexadecimal) to fetch and execute the given instruction by completing the following table:

Instruction	Phase	Time	Hexadecimal content of the register					
			PC	AC	AR	DR	IR	SC
initial values								
	Fetch	T0						
		T1						
	Decode	T2						
	Address	T3						
	Execute	T4						
		T5						

3) Consider the basic computer memory size is changed from 4096x16 to 8Mx32 words where ($M = 2^{20}$). The instruction format has three parts: an Indirect address bit (I), the op-code part and the address part.

a) What is the number of bits of the registers: DR, AR, AC, IR, PC, TR, INPR and OUTR?

b) What is the max number of memory, register reference and input-output instructions?

4) Consider the following register transfers.

By using the table below, for each transfer, specify:

1. The binary value that must be applied to bus select inputs S2, S1, and S0 (if any) ;
2. The register control signals LD, INR, and CLR that must be active (if any);
3. A memory read or write operation (if needed); and
4. The operation in the ALU (if any).

Register transfers	S2	S1	S0	Register Control signal	Memory	Adder
a) PC ← DR						
b) AC ←AC+ 1						
c) AC ← AC+DR, DR ← AC						
d) DR ← 0						
e) M[AR] ← TR						
f) OUTR ← M[AR]						

5) Using the basic computer instruction set, write an assembly program that implements the followings:

a) Logic AND between two 16-bits stored in two memory locations 100 and 101.

b) Arithmetic subtraction of two integers stored in two memory locations 100 and 101.

6) Briefly explain the main function of the following special purpose registers: AR, PC, IR, TR

7) The following control inputs are active in the bus system shown in Fig. 1 below. For each case, specify the register transfer that will be executed during the next dock transition

	S_2	S_1	S_0	LD of register	Memory	Adder
a)	1	1	1	IR	Read	-
b)	1	1	0	PC	-	-
c)	1	0	0	DR	Write	-
d)	0	0	0	AC	-	Add

8) An instruction at address 021 in the basic computer has I = 0, an operation code of the AND instruction, and an address part equal to 083 (all numbers are in hexadecimal). The memory word at address 083 contains the operand B8F2 and the content of AC is A937. Go over the instruction cycle and determine the contents of the following registers at the end of the execute phase: PC, AR, DR, AC, and IR.

9) Explain why each of the following microoperations cannot be executed during a single clock pulse. Specify a sequence of microoperations that will perform the operation.

a) IR ← M[PC]

b) AC ← AC + TR

c) DR ← DR + AC (AC does not change)