```
# Reading C:/modeltech_10.0c/tcl/vsim/pref.tcl
# //  ModelSim SE 10.0c Jul 21 2011
# //
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# //
# Loading project ReadFile
#
# Compile of header.v was successful.
# Compile of jaa.v was successful.
# Compile of jaa_tb.v was successful.
# Compile of file_reader.v was successful.
# Compile of file_reader_tb.v was successful.
# Compile of file_readmemh.v was successful.
# Compile of file_writer.v was successful.
# Compile of file_writer_tb.v was successful.
# Compile of ram_writer.v was successful.
# Compile of memory_writer.v was successful.
# 10 compiles, 0 failed with no errors.
       vsim -novopt work.jaa_tb
# vsim -novopt work.jaa_tb
# Refreshing C:\Users\Alireza Fatemi\Desktop\Verilog\work.jaa_tb
# Loading work.jaa_tb
# Refreshing C:\Users\Alireza Fatemi\Desktop\Verilog\work.jaa
# Loading work.jaa
# Refreshing C:\Users\Alireza Fatemi\Desktop\Verilog\work.memory_writer
# Loading work.memory_writer
      run -all
# Break in Module jaa_tb at C:/Users/Alireza Fatemi/Desktop/Innocence Lost/JAA/Verilogs/jaa_tb.v line 18
      run -all
# Break key hit
# Break in Module jaa_tb at C:/Users/Alireza Fatemi/Desktop/Innocence Lost/JAA/Verilogs/jaa_tb.v line 7
# Break key hit
# Break key hit
      quit -sim
        vsim -novopt work.jaa_tb
# vsim -novopt work.jaa_tb
# Loading work.jaa_tb
# Loading work.jaa
# Loading work.memory_writer
      run -all
# Break in Module jaa_tb at C:/Users/Alireza Fatemi/Desktop/Innocence Lost/JAA/Verilogs/jaa_tb.v line 18
      quit -sim
# Compile of header.v was successful.
# Compile of jaa.v was successful.
# Compile of jaa_tb.v was successful.
# Compile of file_reader.v was successful.
# Compile of file_reader_tb.v was successful.
# Compile of file_readmemh.v was successful.
# Compile of file_writer.v was successful.
# Compile of file_writer_tb.v was successful.
# Compile of ram_writer.v was successful.
# Compile of memory_writer.v was successful.
# 10 compiles, 0 failed with no errors.
       vsim -novopt work.jaa_tb
# vsim -novopt work.jaa_tb
# Refreshing C:\Users\Alireza Fatemi\Desktop\Verilog\work.jaa_tb
# Loading work.jaa_tb
# Refreshing C:\Users\Alireza Fatemi\Desktop\Verilog\work.jaa
# Loading work.jaa
# Refreshing C:\Users\Alireza Fatemi\Desktop\Verilog\work.memory_writer
# Loading work.memory_writer
      run -all
# Opcode : 03    1
# 11100011101000000001000000000000
# 11101001001011010000000000000010
```

```
# Opcode : 04    2
# 11100011101000000001000000000001
# 11101001001011010000000000000010
# Opcode : 05    3
# 11100011101000000001000000000010
# 11101001001011010000000000000010
# Opcode : 06    4
# 11100011101000000001000000000011
# 11101001001011010000000000000010
# Opcode : 07    5
# 11100011101000000001000000000100
# 11101001001011010000000000000010
# Opcode : 08    6
# 11100011101000000001000000000101
# 11101001001011010000000000000010
# Opcode : 3b    7
# 11101000101111010000000000000001
# 11100101100000010011000000000000
# Opcode : 3c    8
# 11101000101111010000000000000001
# 11100101100000010011000000000001
# Opcode : 3d    9
# 11101000101111010000000000000001
# 11100101100000010011000000000010
# Opcode : 3e   10
# 11101000101111010000000000000001
# 11100101100000010011000000000011
# Opcode : 1a   11
# 11100101100100010011000000000000
# 11101001001011010000000000000010
# Opcode : 1b   12
# 11100101100100010011000000000001
# 11101001001011010000000000000010
# Opcode : 1c   13
# 11100101100100010011000000000010
# 11101001001011010000000000000010
# Opcode : 1d   14
# 11100101100100010011000000000011
# 11101001001011010000000000000010
# Opcode : 60   15
# 11101000101111010000000000000110
# 11100000100000010000000000000010
# Opcode : 59   16
# 11101000101111010000000000000001
# 11101001001011010000000000000001
# 11101001001011010000000000000010
# Opcode : 5a   17
# 11101000101111010000000000000011
# 11101001001011010000000000000010
# 11101001001011010000000000000011
# Opcode : 5b   18
# 11101000101111010000000000000111
# 11101001001011010000000000000100
# 11101001001011010000000000000010
# 11101001001011010000000000000101
# Opcode : 5c   19
# 11101000101111010000000000000011
# 11101001001011010000000000000010
# 11101001001011010000000000000011
# 11101001001011010000000000000001
# Opcode : 5d   20
# 11101000101111010000000000000111
# 11101001001011010000000000000100
# 11101001001011010000000000000010
# 11101001001011010000000000000101
# 11101001001011010000000000000010
# Opcode : 5e   21
# 11101000101111010000000000001111
# 11101001001011010000000000001000
# 11101001001011010000000000000100
```

```
# 11101001001011010000000000000010
# 11101001001011010000000000001001
# 11101001001011010000000000000100
# Opcode : 36   23
# 11101000101111010000000000000010
# 11100101100000010011000000000000
# Opcode : 5f   24
# 11101000101111010000000000000011
# 11101001001011010000000000000011
# Opcode : 15   26
# 11100101100100010011000000000000
# 11101001001011010000000000000010
# Not supported. xxxxxxxx   27
# Break in Module jaa_tb at C:/Users/Alireza Fatemi/Desktop/Innocence Lost/JAA/Verilogs/jaa_tb.v line 18
```