Sharif University of Technology
Department of Computer Engineering

Digital System Design
Static Timing Analysis (STA)

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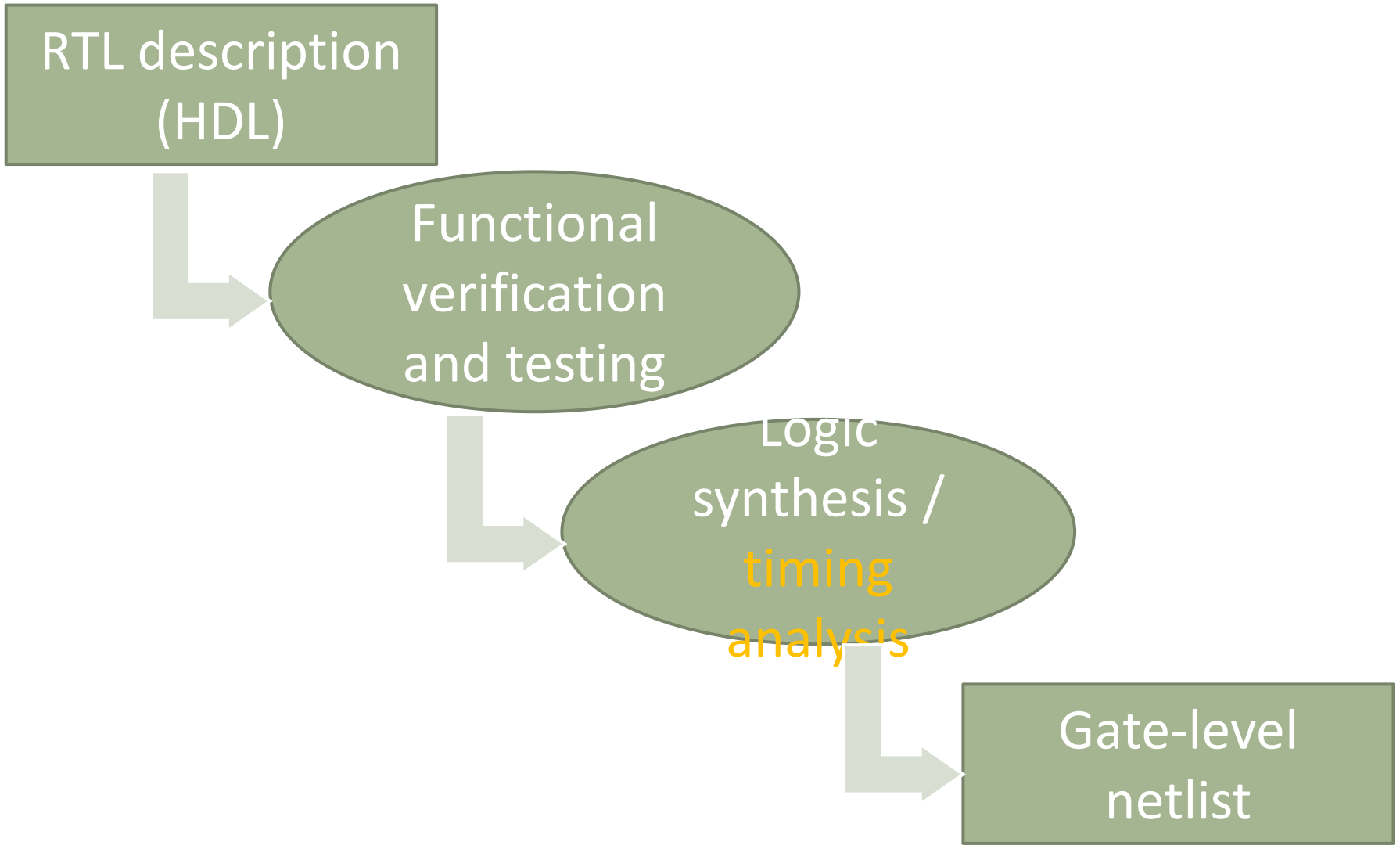
Timing Analysis

- To check if the circuit meets timing constraints
  - Timing the most important among all constraints
    - Design not working if not met
    - Compared with area, power, etc.
  - Timing constraints
    - Setup time
    - Hold time
    - Maximum clock frequency

Timing Analysis (Cont.)



Timing Analysis (Cont.)

Static

- Checks every path
- Fast
- Timing only
- Synchronous only
- No input/output vectors

Dynamic

- Difficult to cover all paths
- Time and computation intensive
- Functionality and timing
- Both syn. and async.
- Uses input/output vectors

STA Outline

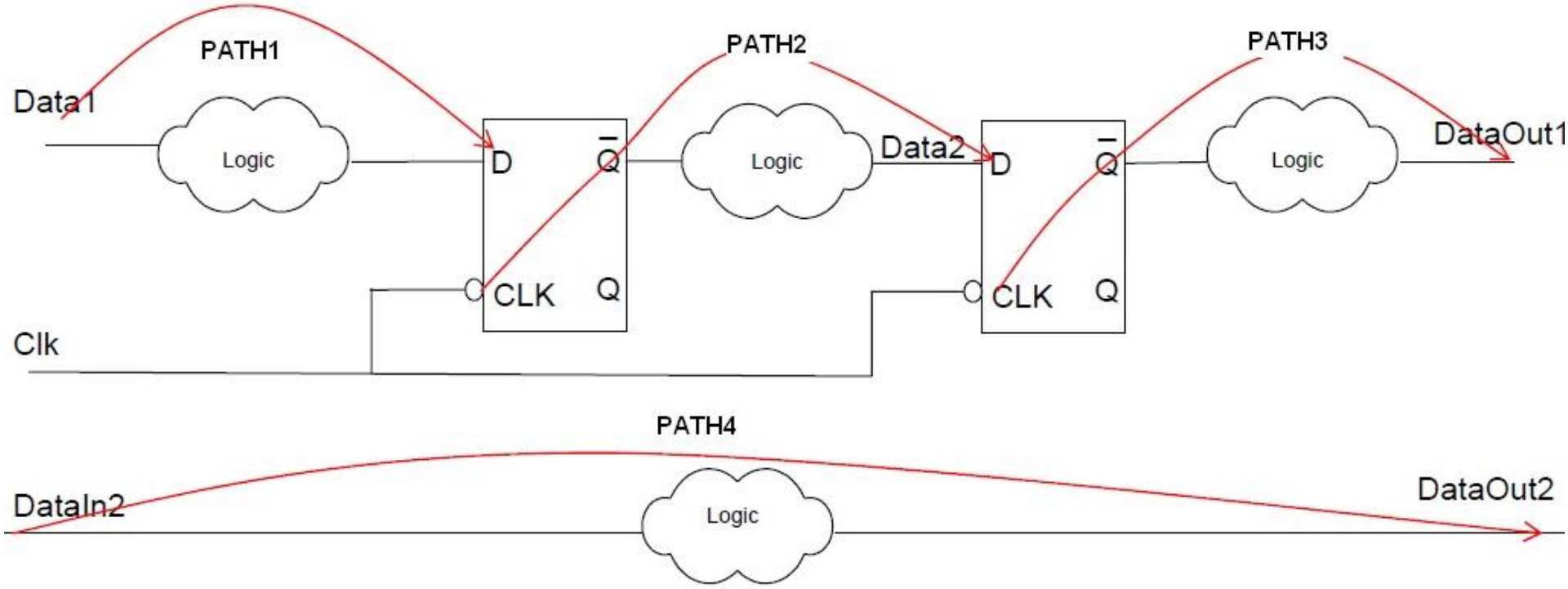
- Timing paths
- Calculating setup and hold times
- Checking setup and hold violations
- Calculating maximum frequency
- Fixing setup and hold violations

Timing Paths

- Data path
  - Start point
    - Input port of the design
    - Clock pin of the sequential cell (flip-flop, etc.)
  - End point
    - Output port of the design
    - Data input pin of the sequential cell
  - Four different combinations

Timing Path (Cont.)

- Data path

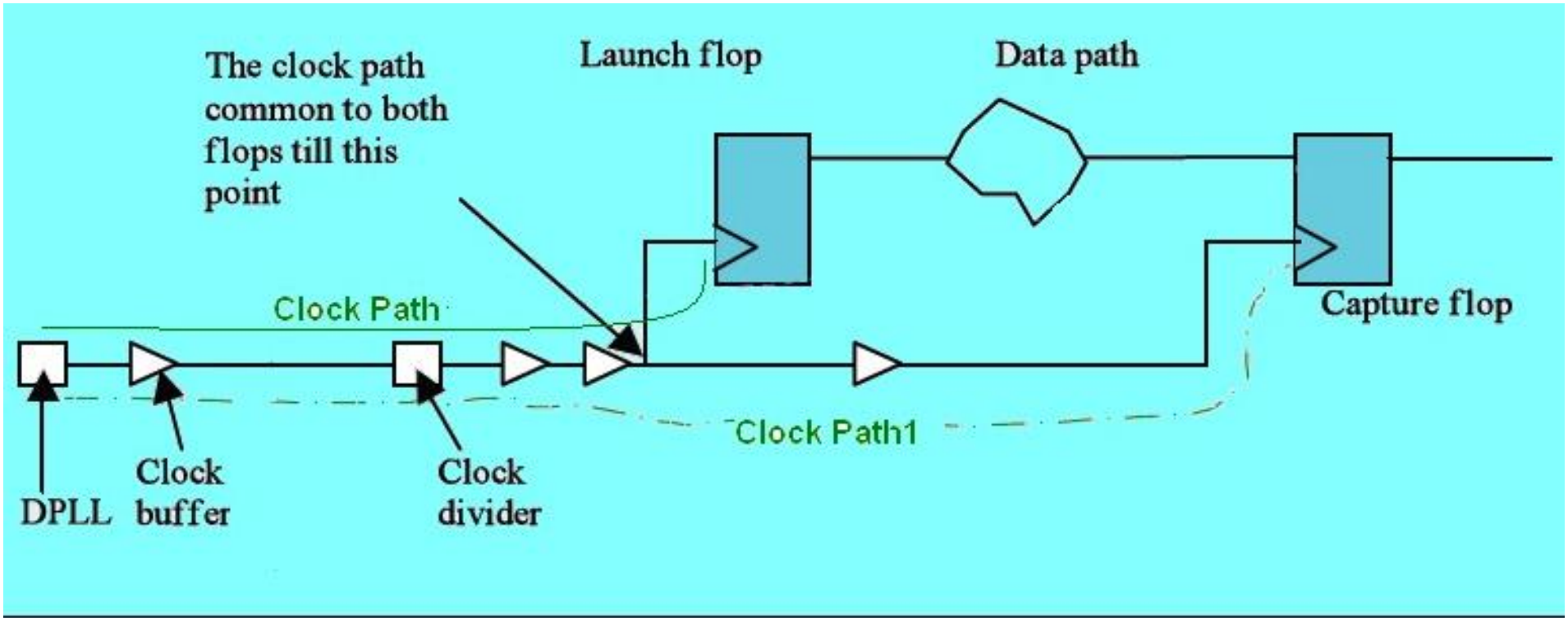


Timing Path (Cont.)

- Clock path
  - Start point
    - Clock input port
  - End point
    - Clock pin of the sequential cell

Timing Path (Cont.)

- Clock path

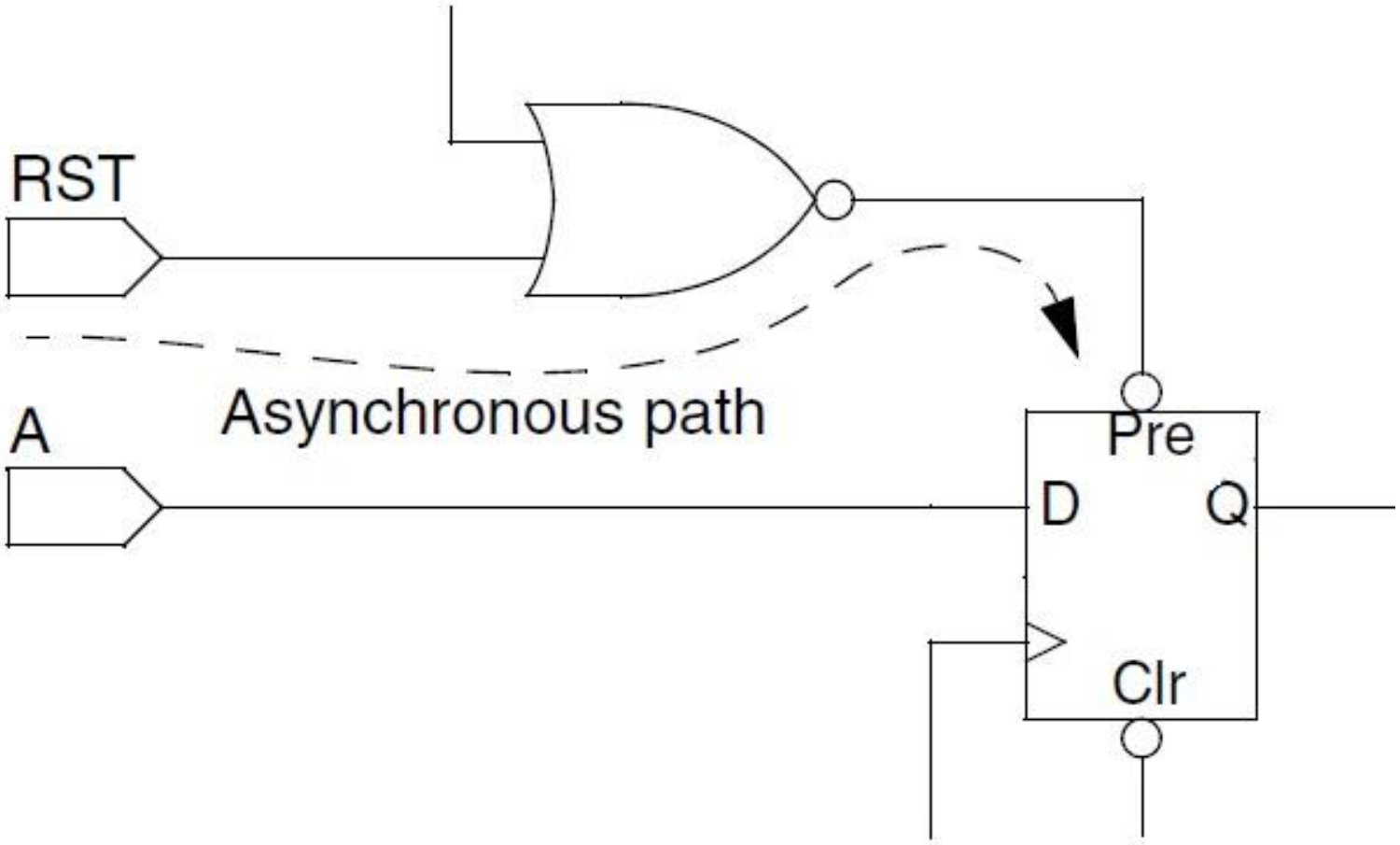


Timing Path (Cont.)

- Asynchronous path
  - Start point
    - Input port of the design
  - End point
    - Asynchronous set/reset/clear pin of the sequential cell

Timing Path (Cont.)

- Asynchronous path

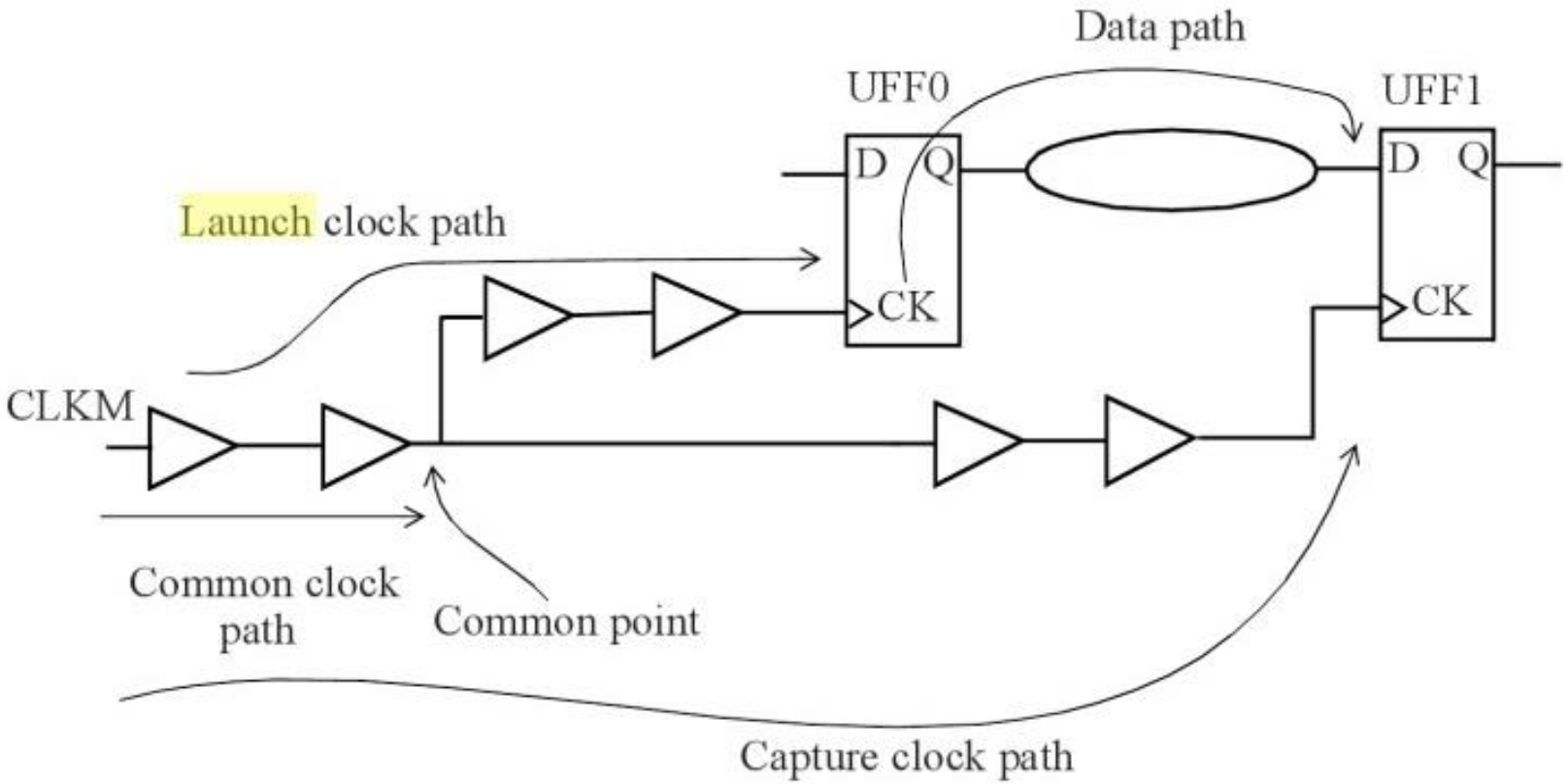


Timing Path (Cont.)

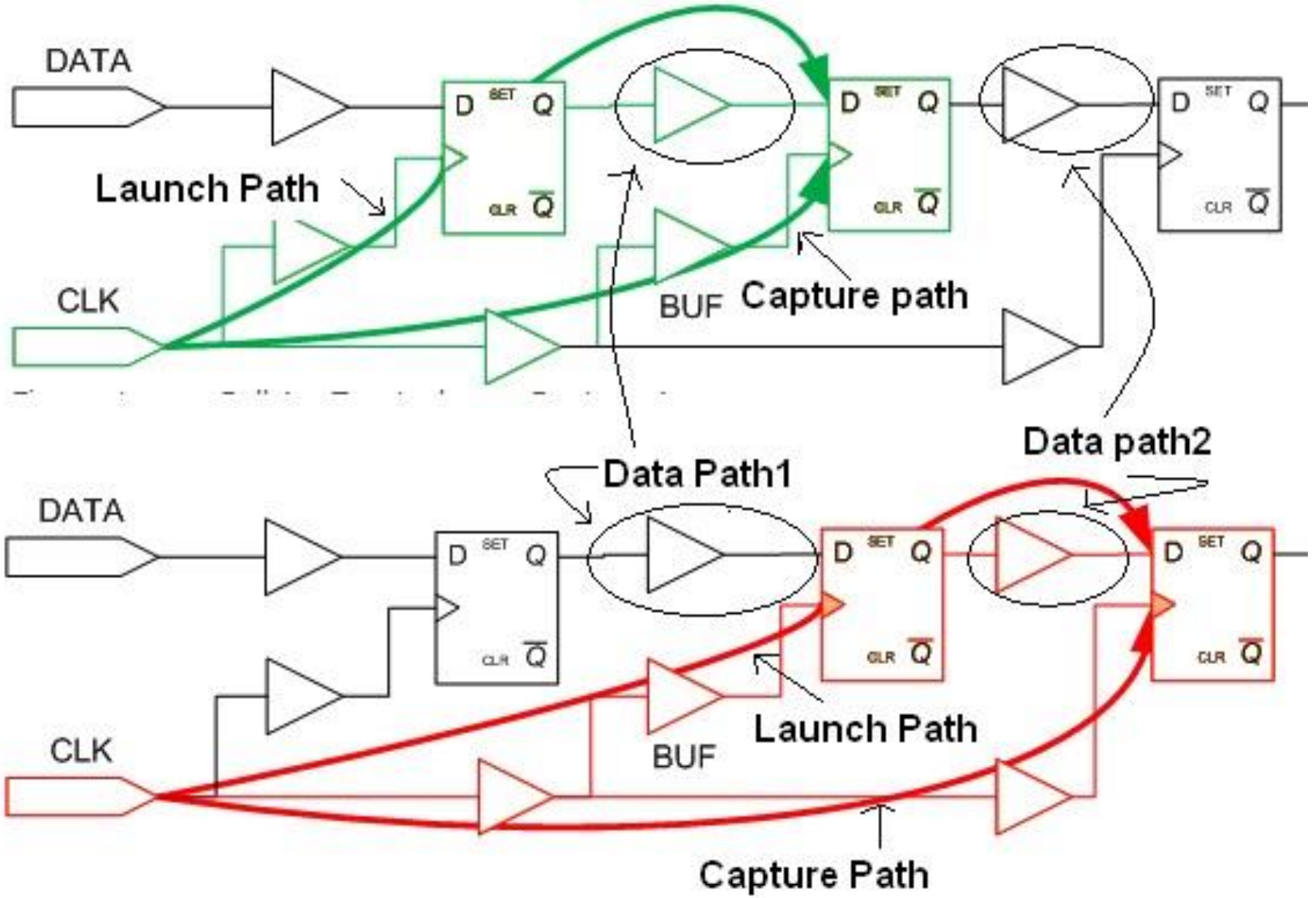
- Critical path
  - Path with the longest delay in a design
  - Limits maximum clock frequency
- Launch path
  - Clock path of launch flip-flop
  - Responsible for launching the data
- Capture path
  - Clock path of capture flip-flop
  - Responsible for capturing the data
- Data path

Timing Path (Cont.)

- Launch flip-flop: UFF0
- Capture flip-flop: UFF1



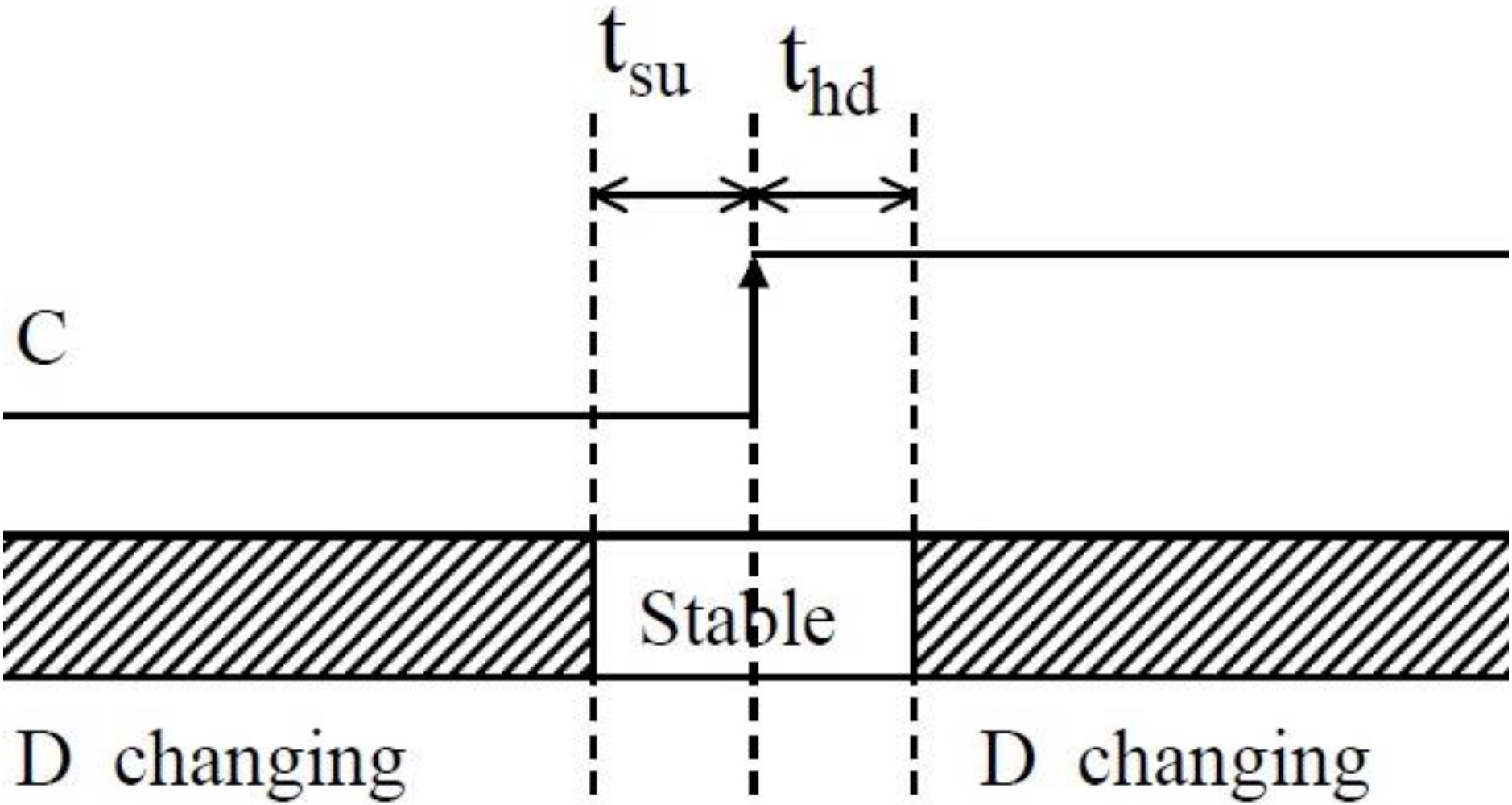
Timing Path (Cont.)



Setup and Hold Time

- Setup time
  - Minimum amount of time that the synchronous data signal must be stable before the active edge of the clock
- Hold time
  - Minimum amount of time that the synchronous data signal must be stable after the active edge of the clock
- Dependent on the internal circuitry of the flip-flop

Setup and Hold Time (Cont.)

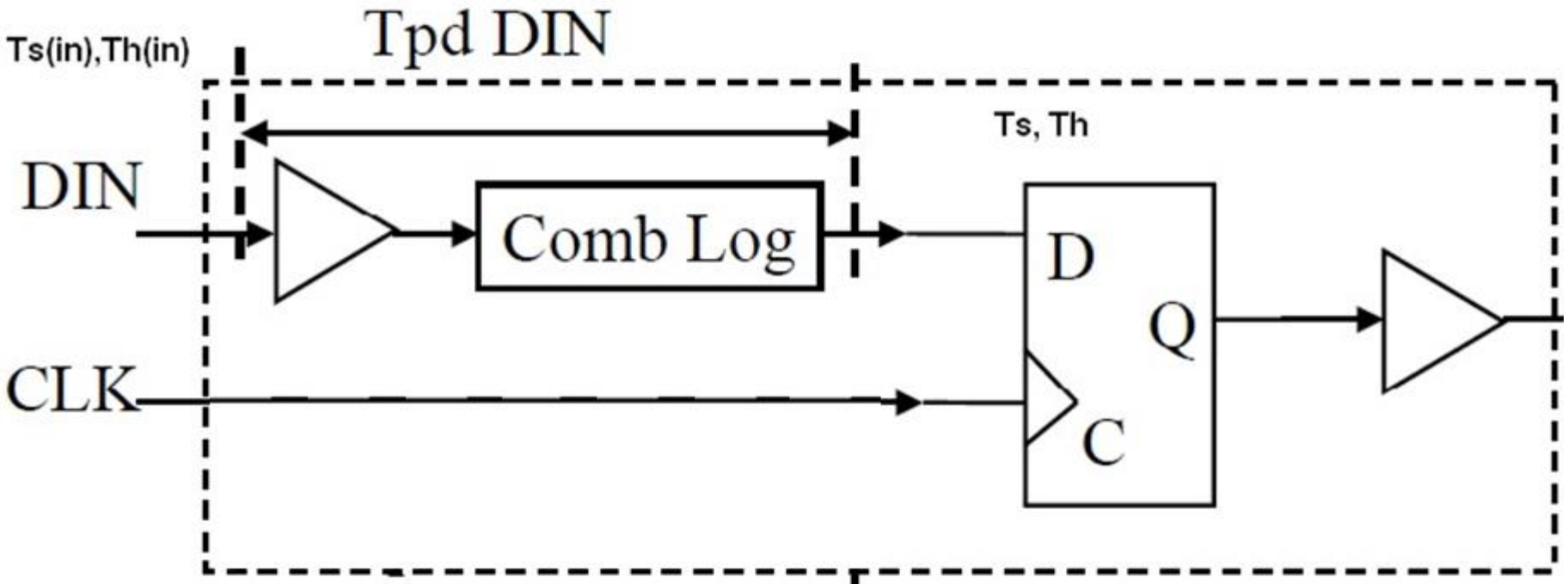


Setup and Hold Time (Cont.)

- Setup violation
  - If the data is not stable T_{su} time before the active clock edge
- Hold violation
  - If the data is not stable T_{hd} time after the active clock edge

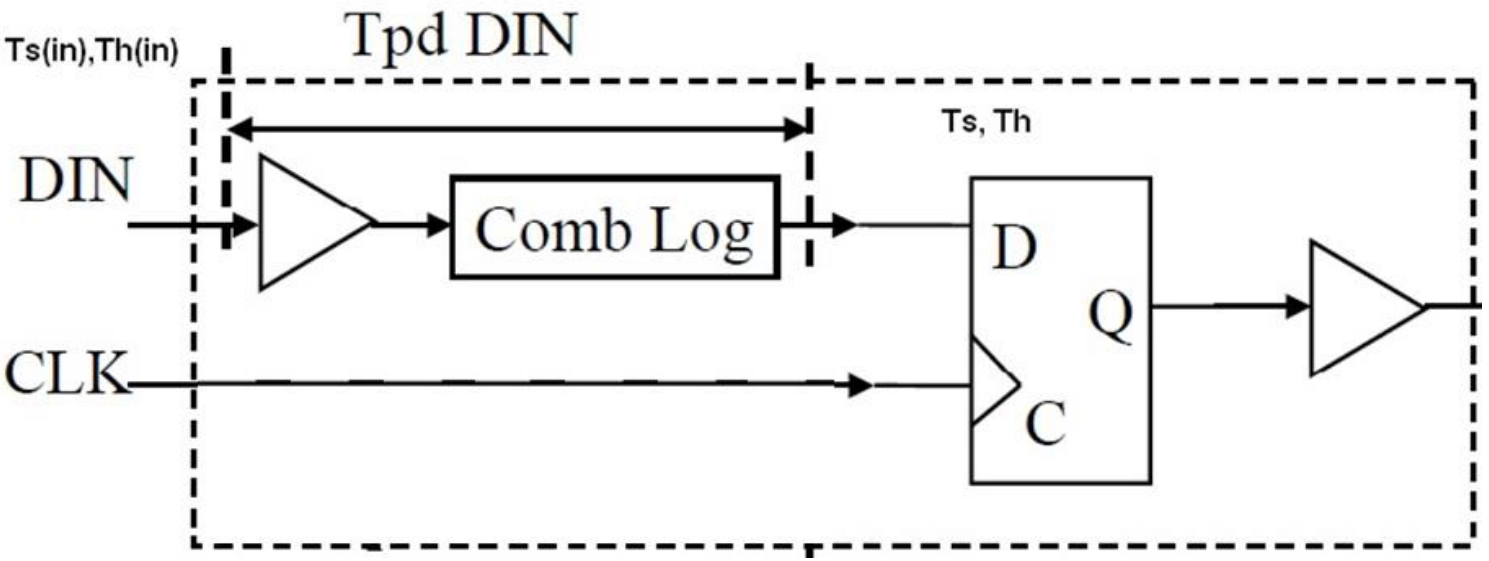
Setup and Hold Time (Cont.)

1. What is the minimum time DIN must be stable before/after the active clock edge so that there's no violations?



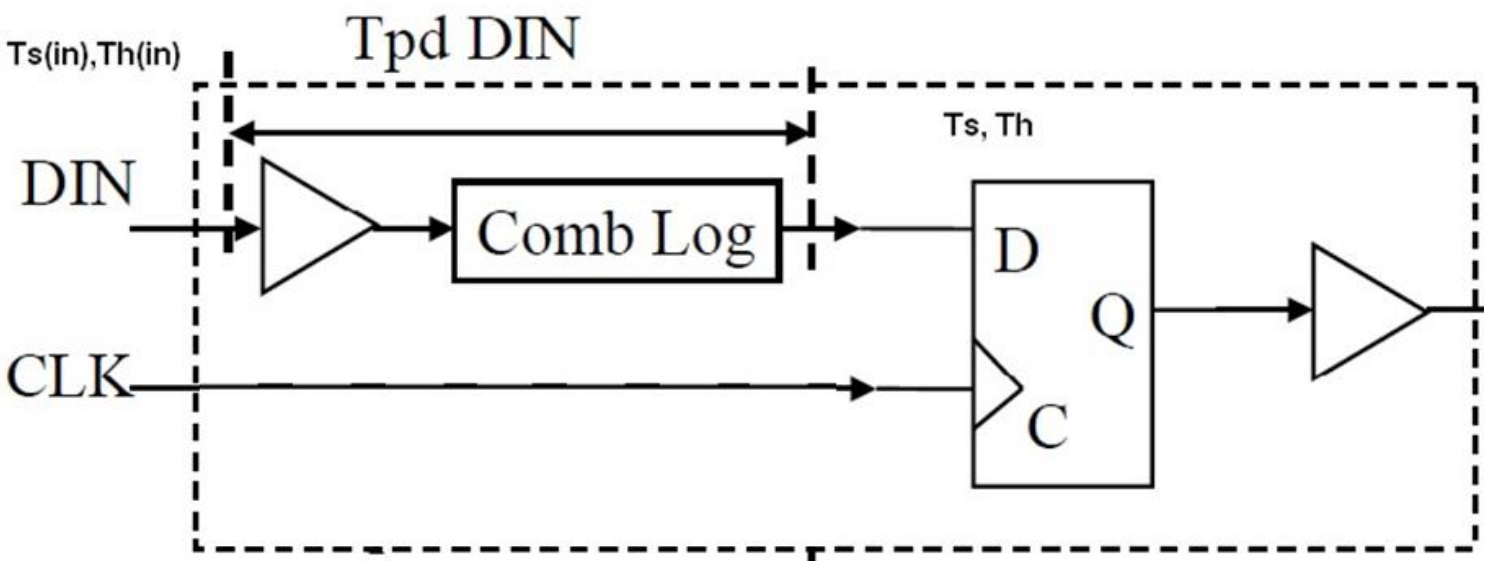
Setup and Hold Time (Cont.)

- Setup analysis
  - It takes DIN signal T_{pd} (DIN) time to reach D input
  - Must be there T_{su} (D) time before the CLK edge
    - T_{su} (DIN) = T_{pd} (DIN) + T_{su} (D)



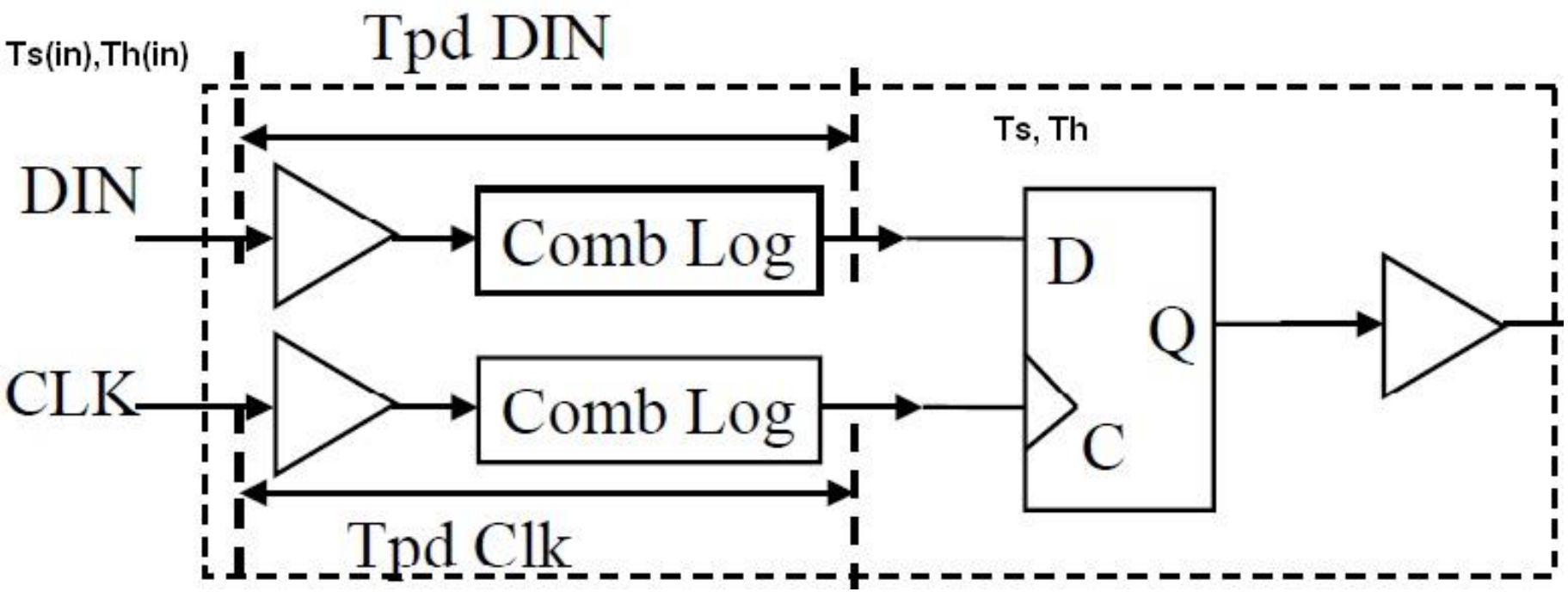
Setup and Hold Time (Cont.)

- Hold analysis
  - DIN must be stable at D input T_{hd} (D) time after the CLK edge
  - It means that the next DIN must not reach DIN till then
    - T_{hd} (DIN) = T_{hd} (D) - T_{pd} (DIN)



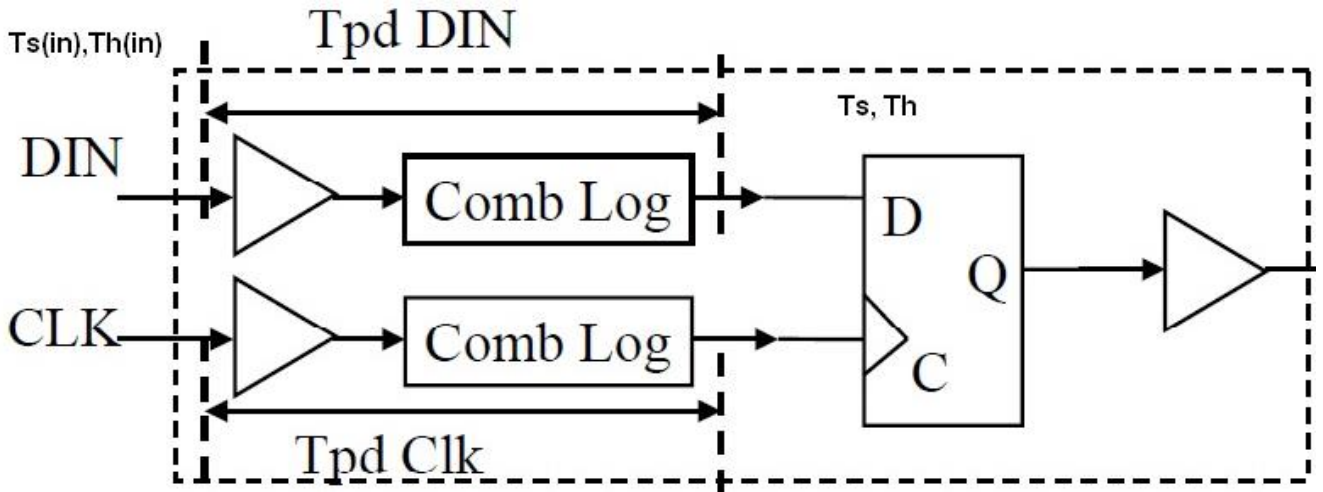
Setup and Hold Time (Cont.)

2. How about this one?



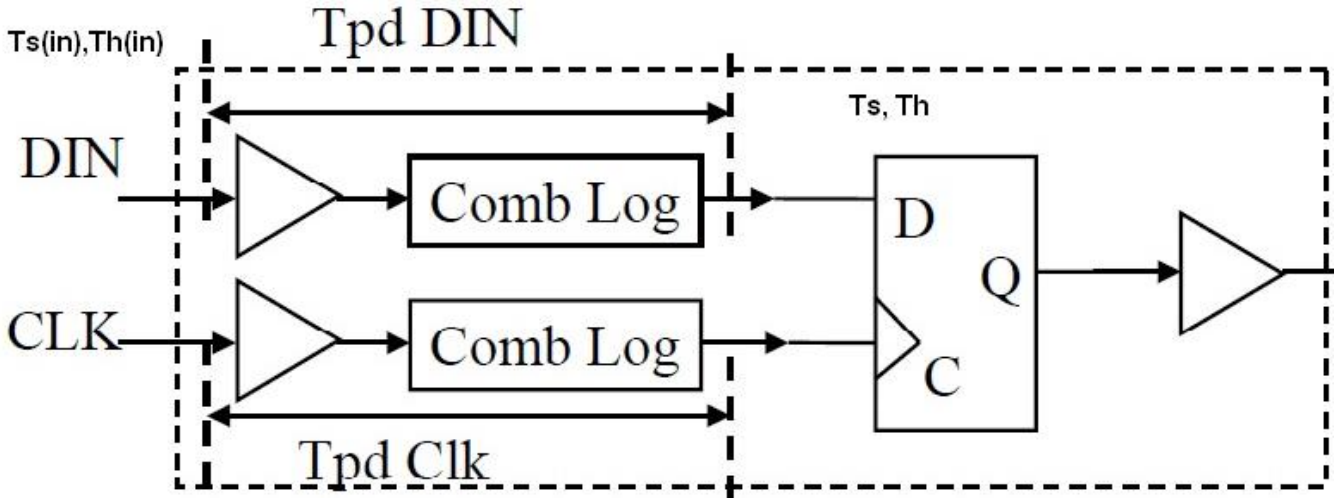
Setup and Hold Time (Cont.)

- Setup analysis
  - Same as previous
  - But clock edge arrives a little later
  - So DIN has a bit more time to reach D
  - T_{su} (DIN) = T_{pd} (DIN) + T_{su} (D) – T_{pd} (CLK)



Setup and Hold Time (Cont.)

- Hold analysis
  - Clock edge arrives a little later at C input
  - So DIN must be at D a bit more time to meet its edge
  - T_{hd} (DIN) = T_{hd} (D) - T_{pd} (DIN) + T_{pd} (CLK)

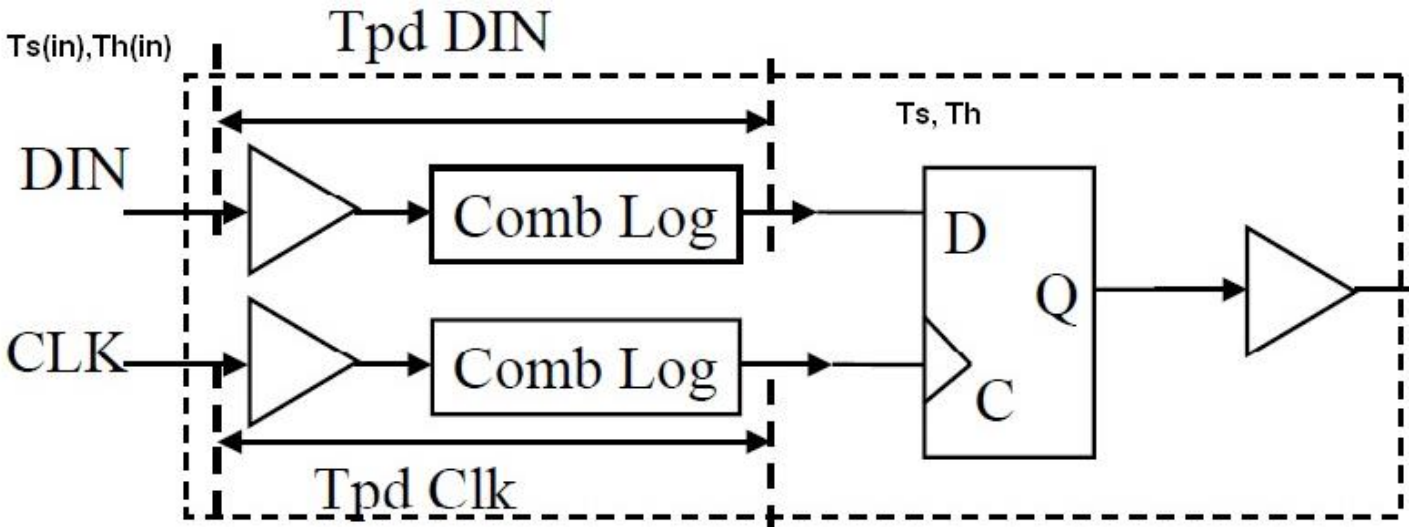


Setup and Hold Time (Cont.)

- Cell and wire delays
  - Not constant under
    - Environmental variations
    - PVT (process, voltage and temperature) variations
- In setup analysis, consider
  - Data path maximum delay
  - Clock path minimum delay
- In Hold analysis, consider
  - Data path minimum delay
  - Clock path maximum delay

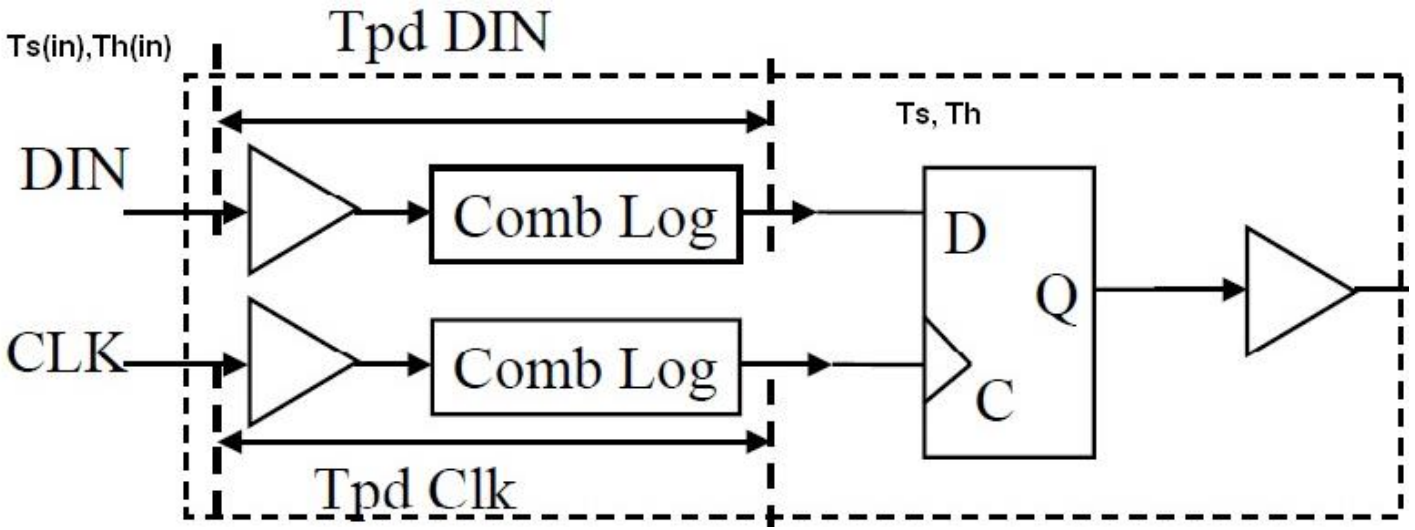
Setup and Hold Time (Cont.)

- Setup analysis
  - T_{su} (DIN) = Max T_{pd} (DIN) + T_{su} (D) – Min T_{pd} (Clk)
    - If Max T_{pd} (DIN) + T_{su} (D) > Min T_{pd} (Clk), otherwise 0



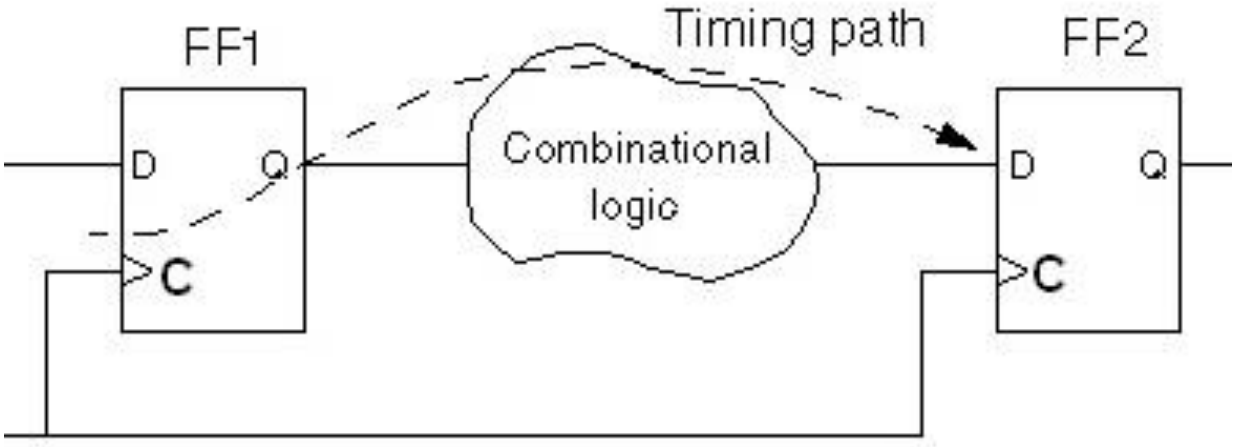
Setup and Hold Time (Cont.)

- Hold analysis
  - T_{hd} (DIN) = T_{hd} (D) - Min T_{pd} (DIN) + Max T_{pd} (Clk)
    - If T_{hd} (D) + Max T_{pd} (Clk) > Min T_{pd} (DIN), otherwise 0



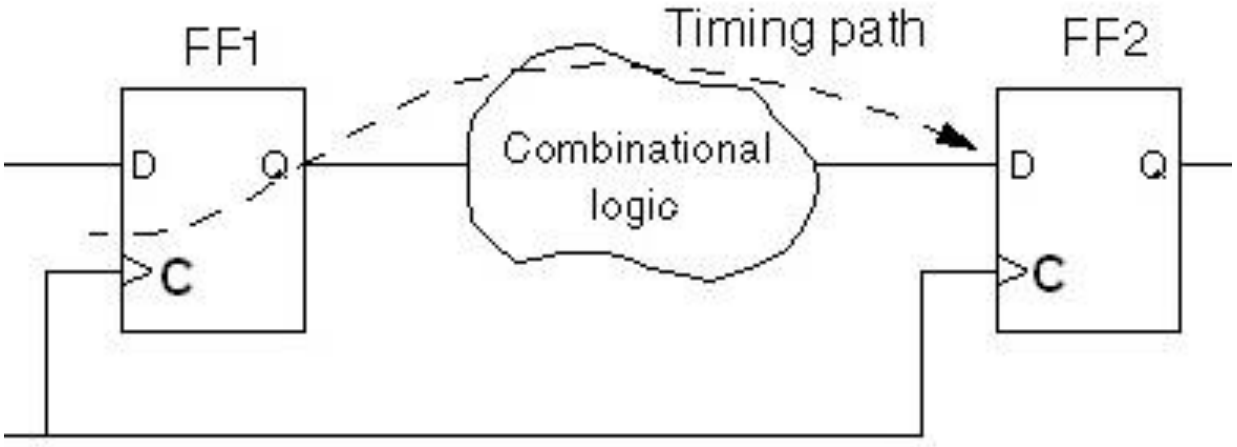
Setup and Hold Time (Cont.)

- The case for two flip-flops with same delay in launch and capture paths
  - Data path
    - FF1.C→FF1.Q→Combinational logic→FF2.D
  - Launch flip-flop: FF1
  - Capture flip-flop: FF2



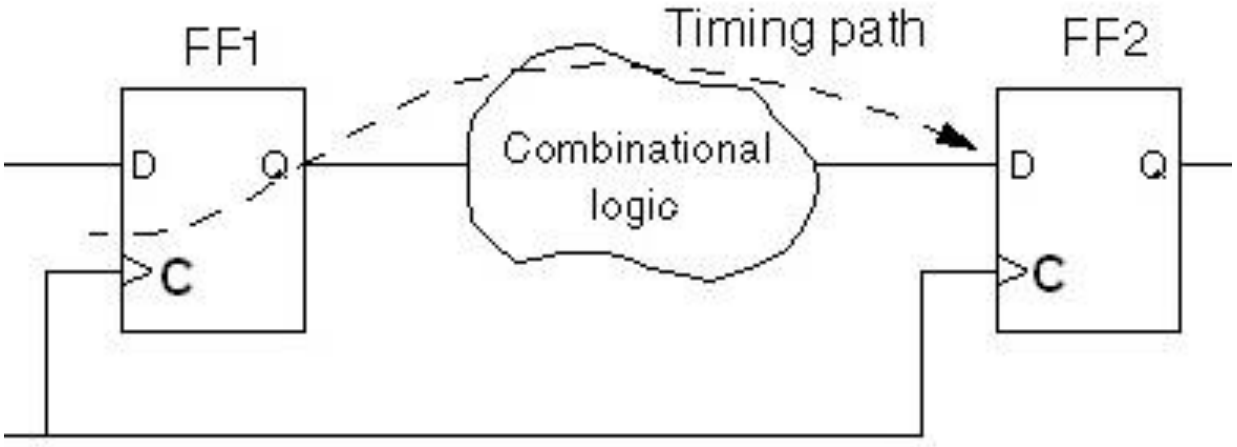
Setup and Hold Time (Cont.)

- To have no setup violation
  - Data launched at FF1 should arrive at FF2.D T_{su} time before the active edge of FF2.C
  - $T_{clk\text{-}to\text{-}q} + T_{pd} <=$ clock period - T_{su}

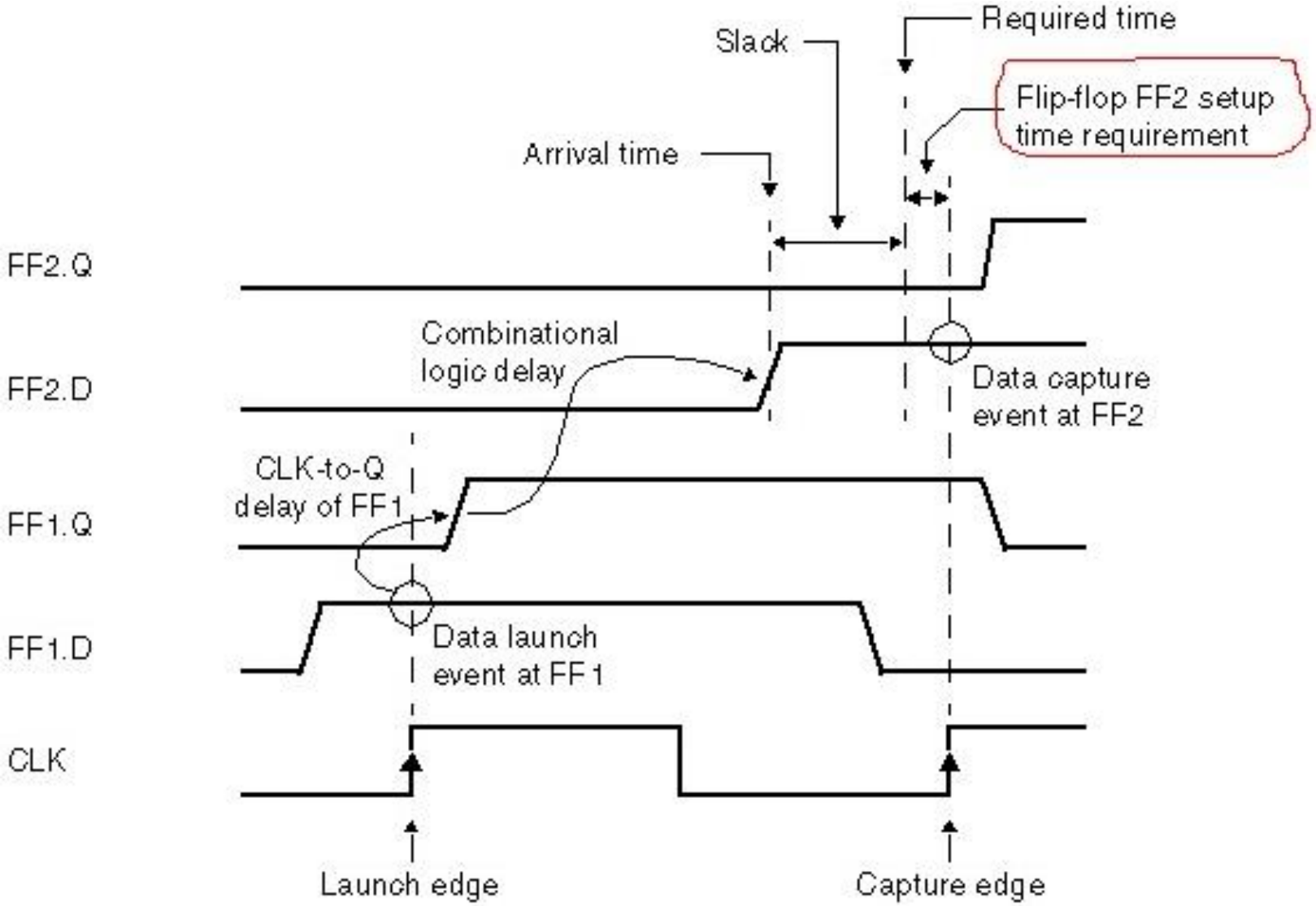


Setup and Hold Time (Cont.)

- To have no hold violation
  - Data must be stable T_{hd} after the active edge of FF2.C
  - It means that the next data launched at FF1 must not reach FF2.D till then
  - $T_{clk\text{-}to\text{-}q} + T_{pd} >= T_{hd}$

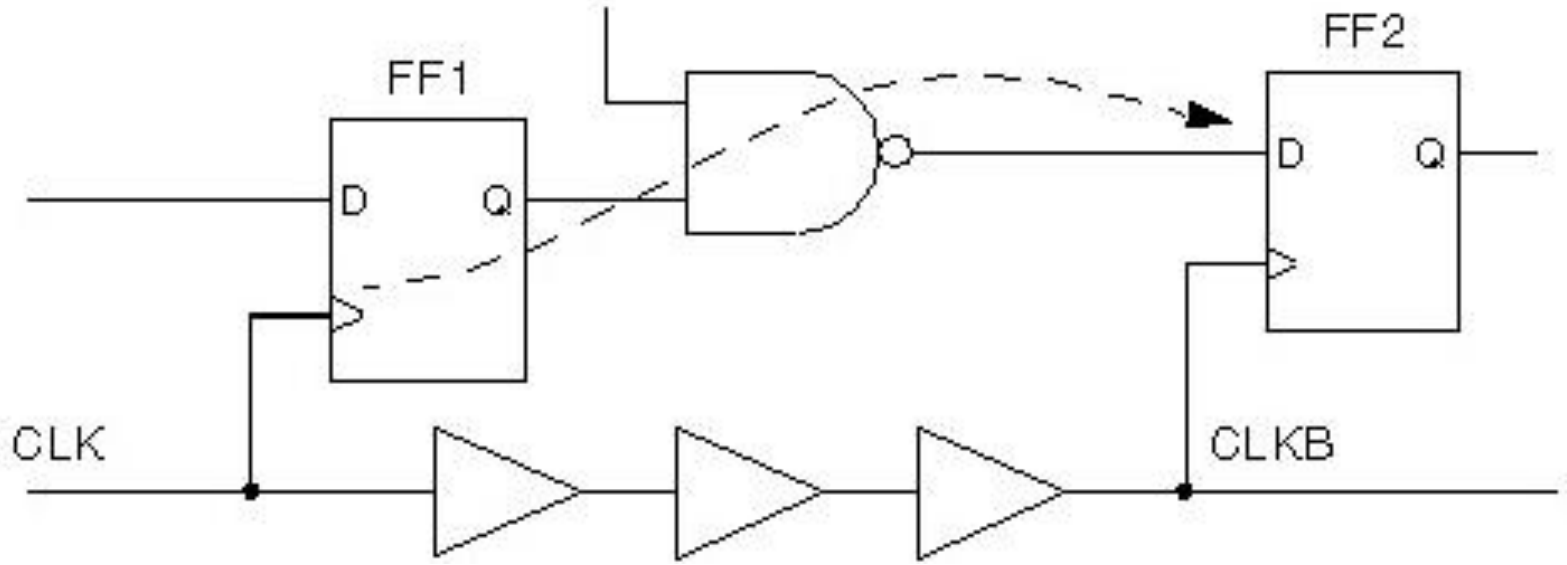


Setup and Hold Time (Cont.)



Setup and Hold Time (Cont.)

4. The case for two FFs with different delays in launch and capture paths
   - There's skew on the clock signal of FF2



Setup and Hold Time (Cont.)

- To have no setup violation
  - Data launched at FF1 must become stable T_{su} time before the active edge of CLKB

$$T_{pd}(CLK) = T_{pd}(\text{capture path}) - T_{pd}(\text{launch path})$$

$$T_{clk\text{-}to\text{-}q} + T_{pd} <= \text{clock period} + T_{pd}(CLK) + -T_{su}$$

  - Remember to check the worst case
  - Setup slack = RHS – LHS of the above inequality
    - Positive when no violation

Setup and Hold Time (Cont.)

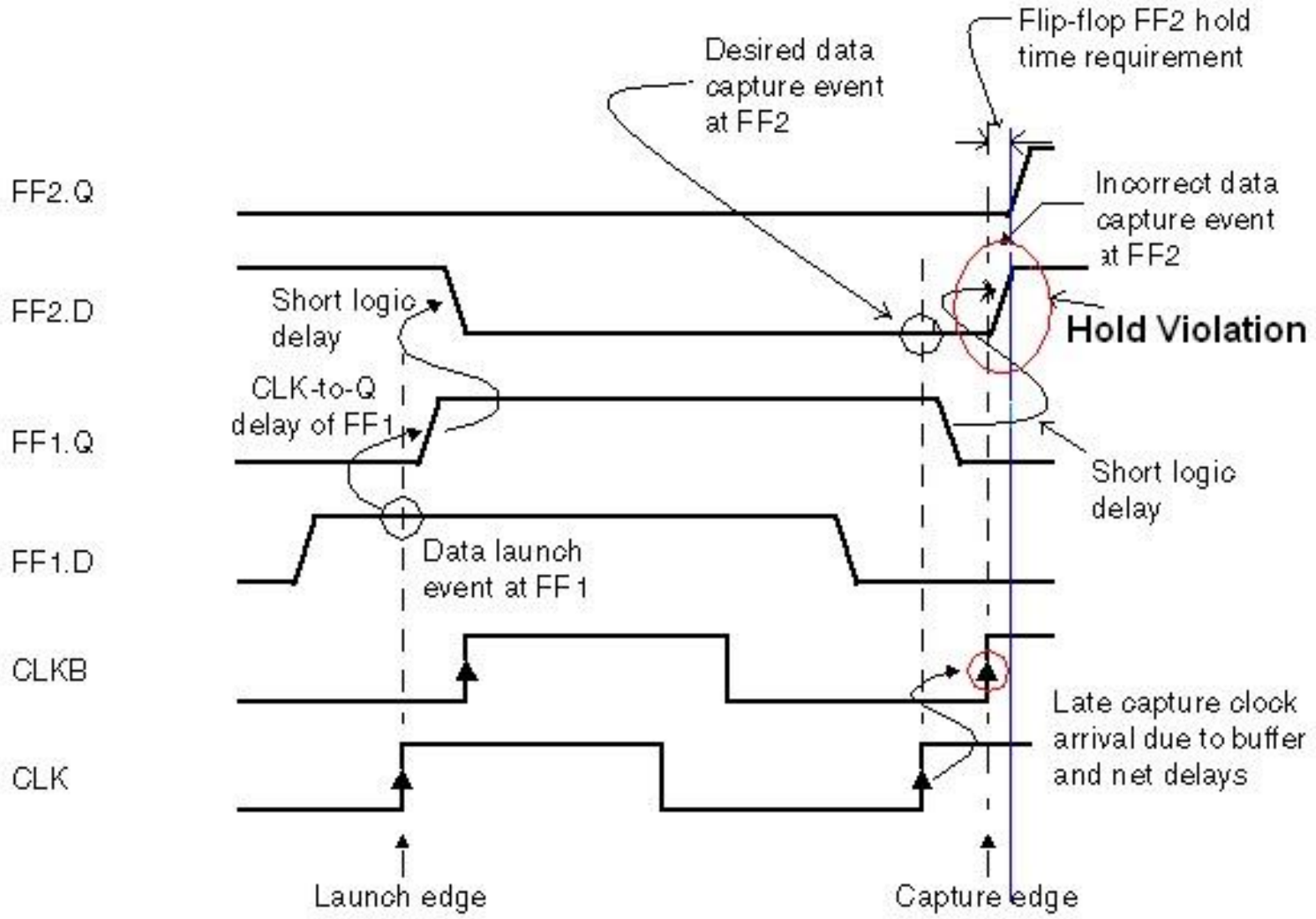
- To have no hold violation
  - Data must be stable T_{hd} after the active edge of CLKB
  - It means the data launched at the next active edge of CLK at FF1must not reach FF2.D till then

$$T_{pd}(CLK) = T_{pd}(\text{capture path}) - T_{pd}(\text{launch path})$$

$$T_{clk\text{-}to\text{-}q} + T_{pd} >= T_{hd} + T_{pd}(CLK)$$

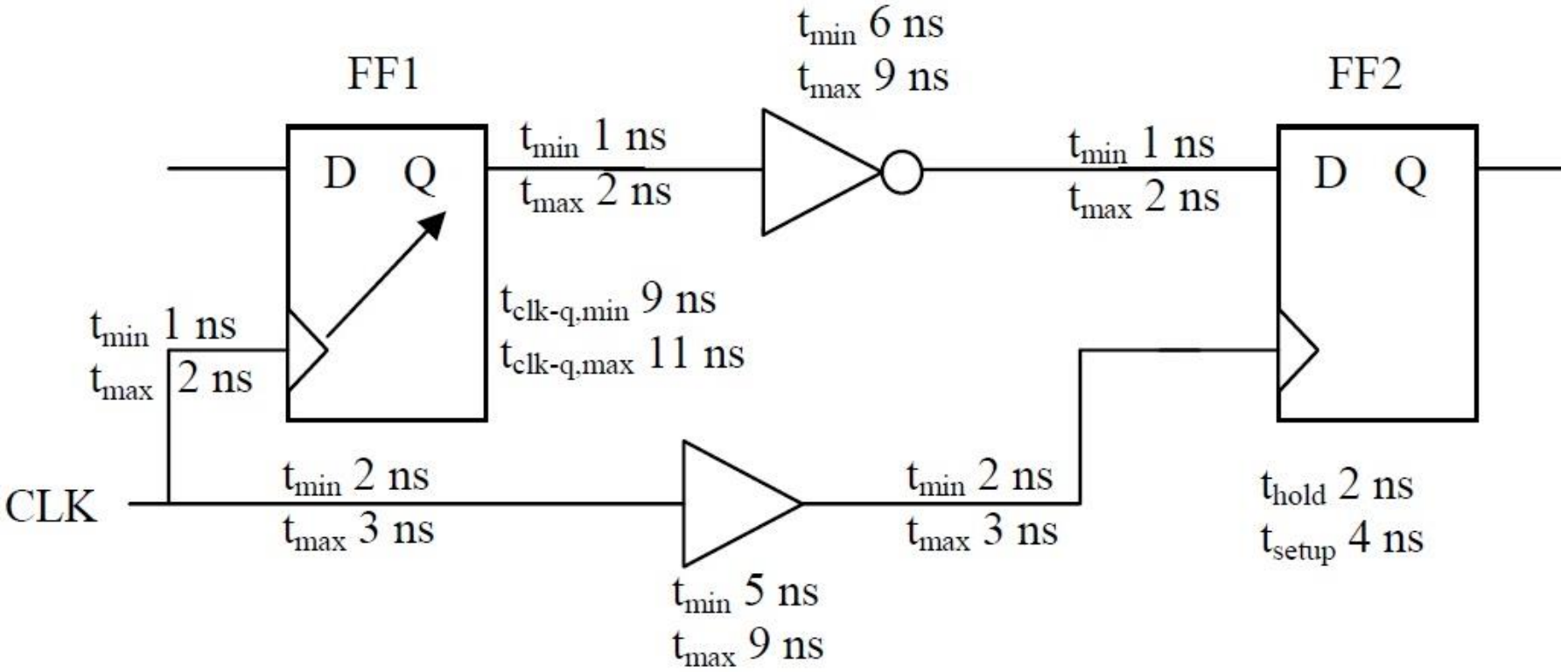
  - Always check the worst possible case
  - Hold slack = LHS – RHS of the above inequality
    - Positive when no violation

Setup and Hold Time (Cont.)



Example 1

- Check if there's any violation.
  - Clock period: 15 ns



Example 1 (Cont.)

Max $T_{clk\text{-}to\text{-}q}$	11
Max T_{pd}	2+9+2

Clock period	15
Min T_{pd} (capture)	2+5+2
Max T_{pd} (launch)	2
FF setup time	4

$$T_{clk\text{-}to\text{-}q} + T_{pd}$$
$$<=$$
$$\text{clock period} + T_{pd}\,(\text{capture path}) - T_{pd}\,(\text{launch path}) - T_{su}$$

Not satisfied → Setup violation

Example 1 (Cont.)

Min $T_{clk\text{-}to\text{-}q}$	9
Min T_{pd}	1+6+1

FF hold time	2
Max T_{pd} (capture)	3+9+3
Min T_{pd} (launch)	1

$$T_{clk\text{-}to\text{-}q} + T_{pd}$$
$$>=$$
$$T_{hd} + T_{pd} \text{ (capture path)} - T_{pd} \text{ (launch path)}$$

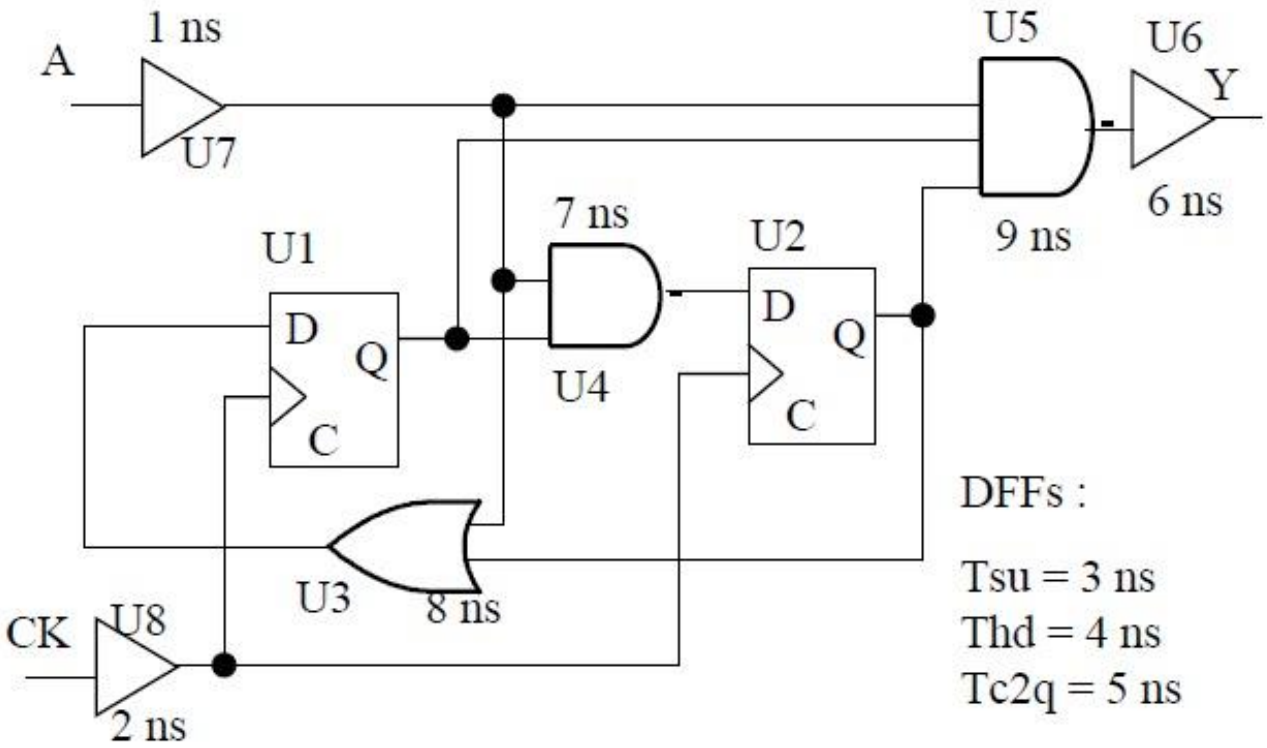
Satisfied → No hold violation

Calculating Max Frequency

- To calculate maximum operating frequency (minimum clock period)
  - Calculate path delays
    - Flop to flop
    - Input to clock
    - Clock to output
    - Input Pin to output pin
  - Min clock period is equal to the max delay

Example 2

- Calculate
  - setup and hold times at input A.
  - minimum clock period (maximum operating freq.).



Example 2 (Cont.)

- Setup time at A
  - List all paths from A to FFs
    - A→U7→U4→U2
      - T_{pd}= 1+7 = 8
    - A→U7→U3→U1
      - T_{pd}= 1+8 = 9
    - Use the longest paths for setup analysis
  - T_{su} (A) = Max T_{pd} (A) + T_{su} – Min T_{pd} (Clk)
    - 9 + 3 – 2 = 10 ns

Example 2 (Cont.)

- Hold time at A
  - List all paths from A to FFs
    - A→U7→U4→U2
      - T_{pd}= 1+7 = 8
    - A→U7→U3→U1
      - T_{pd}= 1+8 = 9
    - Use the shortest paths for hold analysis
  - T_{hd} (A) = T_{hd} - Min T_{pd} (A) + Max T_{pd} (Clk)
    - 4 – 8 + 2 = -2 < 0 → T_{hd} (A) = 0 ns

Example 2 (Cont.)

- Calculating max freq.
  - List all flop to flop paths
    - U1→U4→U2
      - 5 + 7 + 3 = 15 ns
    - U2→U3→U1
      - 5 + 8 + 3 = 16 ns

Example 2 (Cont.)

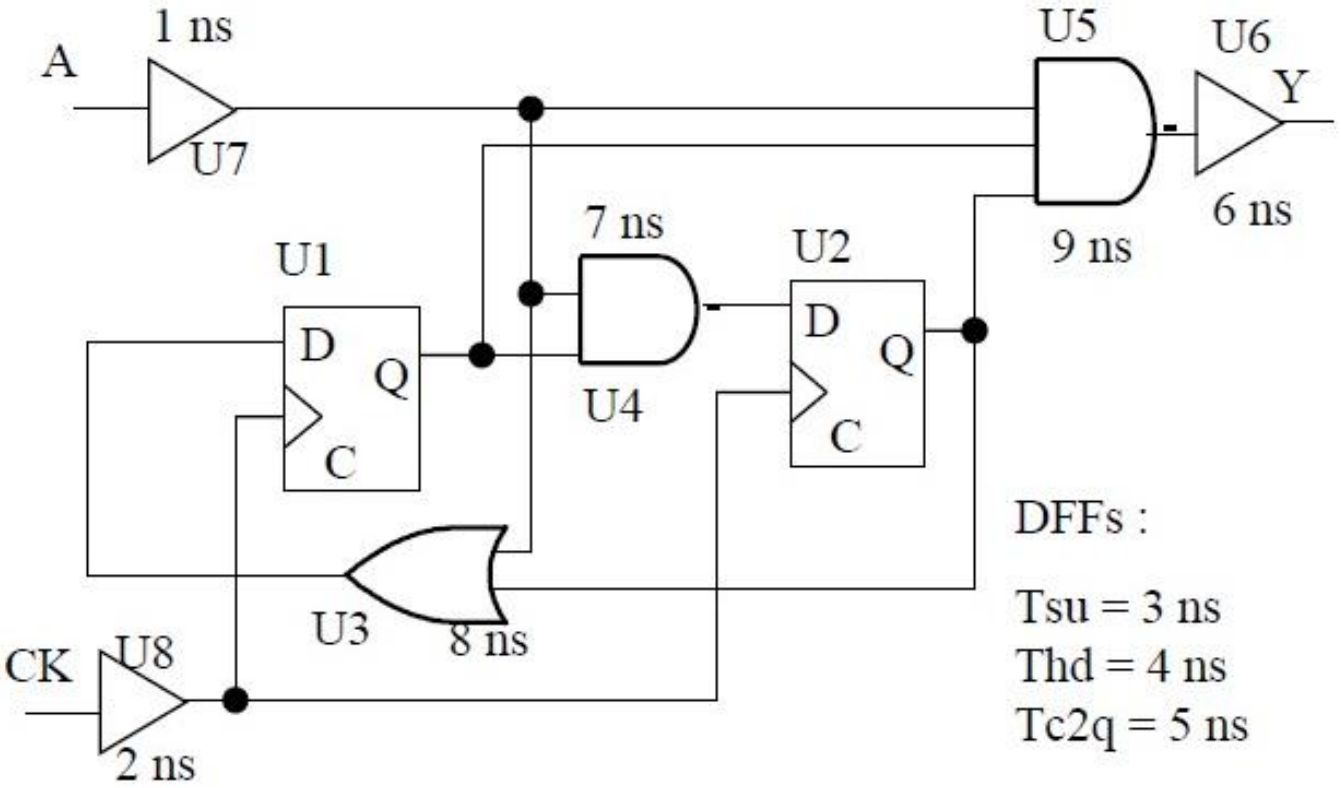
- Calculating max freq.
  - List all flop to output paths
    - U1→U5→U6
      - 2 + 5 + 9 + 6 = 22 ns
    - U2→U5→U6
      - 2 + 5 + 9 + 6= 22 ns
  - List all input to flop paths
    - A→U7→U4→U2
      - 1+7+3-2 = 9 ns
    - A→U7→U3→U1
      - 1+8+3-2 = 10 ns

Example 2 (Cont.)

- Calculating max freq.
  - List all input to output path
    - A→U7→U5→U6
      - 1 + 9 + 6 = 16 ns
  - Minimum period=max(15,16,22,22,16,9,10) = 22 ns
  - Maximum frequency = 1/22 = 45.45 MHz

Example 3

- Increase the operating frequency by using only two flip-flops
  - FF specifications are given



Example 3 (Cont.)

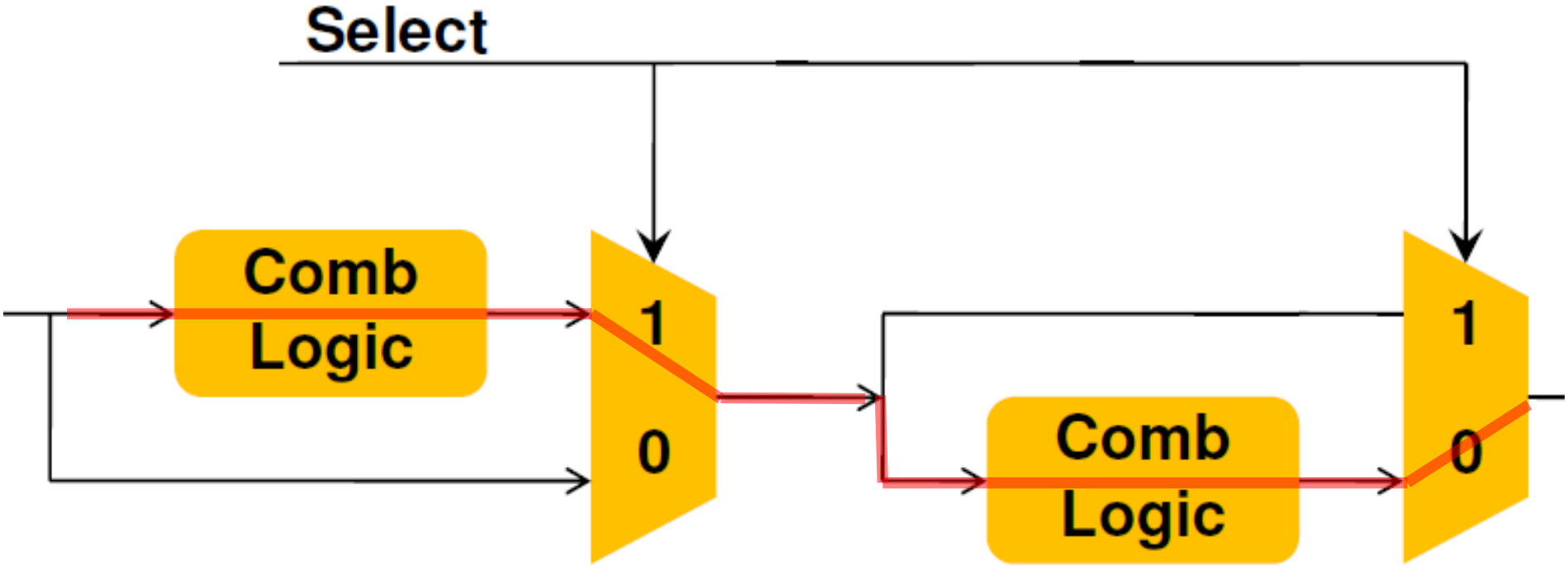
- Insert the FF into the critical path
  - U1→U5→U6
  - U2→U5→U6
  - Best choice is to place it between U5 and U6
- All delays must be re-computed
  - Flop to flop
  - Flop to output
  - Input to output
  - Input to flop
- Insert the 2nd FF in the new critical path

Exceptions

- False path
  - A path that is never activated
  - Must be excluded from timing analysis
  - When using EDA tools
    - Must be introduced to the tool by the designer
    - The tool neither tries to meet timing in this path nor optimizes it

Exceptions (Cont.)

- False path examples



Exceptions (Cont.)

- False path examples
  - Configuration inputs tied to Vcc/Gnd
  - Test inputs tied to Vcc/Gnd
  - Asynchronous inputs to the chip that have some sort of synchronizing circuit
- Multi-cycle path
  - A path through which multiple cycles are allowed for the data to propagate

Fixing Setup and Hold Violations

- Hold violations are more serious.
  - A chip
    - with setup violation operates in a lower frequency.
    - doesn’t operate at all with hold violation.

Fixing Setup and Hold Violations (Cont.)

1. Increasing data path delay
   - For hold violation
   - Example

Setup	Hold	Clock period	$T_{clk\text{-}to\text{-}q}$	Net delay	Combo. delay
2 ns	1 ns	10 ns	0 ns	0 ns	0.5 ns

- T_{pd} <=clock period – setup → No setup violation
- T_{pd} < Hold → Hold violation
  - Min acceptable combo. delay = 1 ns
    - Add buffers to the data path
    - No setup or hold violations

Fixing Setup and Hold Violations (Cont.)

2. Increasing clock period
   - For setup violations
   - Example

Setup	Hold	Clock period	$T_{clk\text{-}to\text{-}q}$	Net delay	Combo. delay
6 ns	5 ns	10 ns	0 ns	0 ns	0.5 ns

- T_{pd} <=clock period – setup → No setup violation
- T_{pd} < Hold → Hold violation
  - Min acceptable combo. delay = 5 ns
    - Causes setup violation

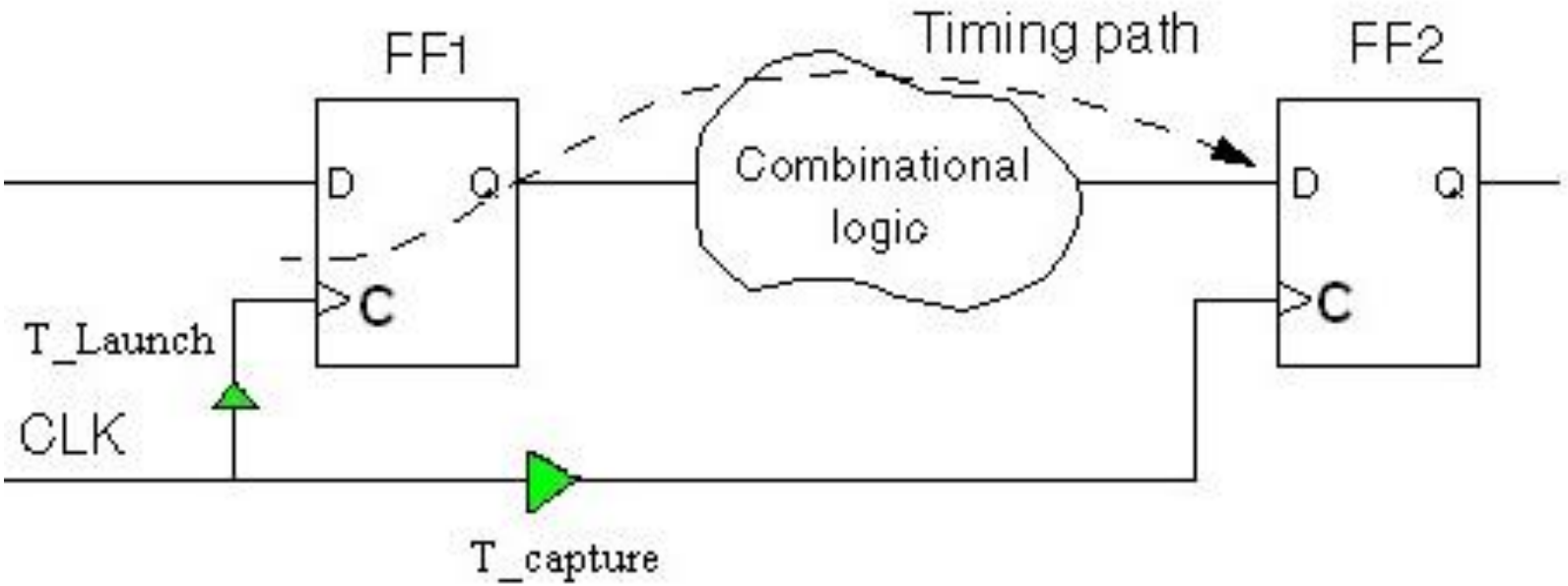
Fixing Setup and Hold Violations (Cont.)

- Example (cont.)
  - Increasing data path delay doesn't work alone
    - 5 ns = Hold <= T_{pd} <= period – setup = 10 -6 = 4 ns
      - Not satisfiable
      - Min clock period = 11 ns
- For violations to be fixable
  - Clock period >= setup + hold

Fixing Setup and Hold Violations (Cont.)

3. Manipulating clock paths
   - Example

Setup	Hold	Clock period	$T_{clk\text{-}to\text{-}q}$	Net delay	Combo. delay
4 ns	3 ns	10 ns	0 ns	0 ns	8 ns



Fixing Setup and Hold Violations (Cont.)

- Example (cont.)

Setup	Hold	Clock period	$T_{clk\text{-}to\text{-}q}$	Net delay	Combo. delay
4 ns	3 ns	10 ns	0 ns	0 ns	8 ns

- T_{pd} > clock period – setup → Setup violation
- T_{pd} >= Hold → No hold violation
- Remember?

$$T_{clk\text{-}to\text{-}q} + T_{pd} <= \text{clock period} + T_{pd}\,(\text{capture path}) - T_{pd}\,(\text{launch path}) - T_{su}$$

- Setup violation solved if capture path delay += 2

Fixing Setup and Hold Violations (Cont.)

- Example (cont.)

Setup	Hold	Clock period	$T_{clk\text{-}to\text{-}q}$	Net delay	Combo. delay	Capture delay
4 ns	3 ns	10 ns	0 ns	0 ns	8 ns	2 ns

- Neither setup nor hold violation

$$T_{clk\text{-}to\text{-}q} + T_{pd} <= \text{clock period} + T_{pd}\,(\text{capture path}) - T_{pd}\,(\text{launch path}) - T_{su}$$

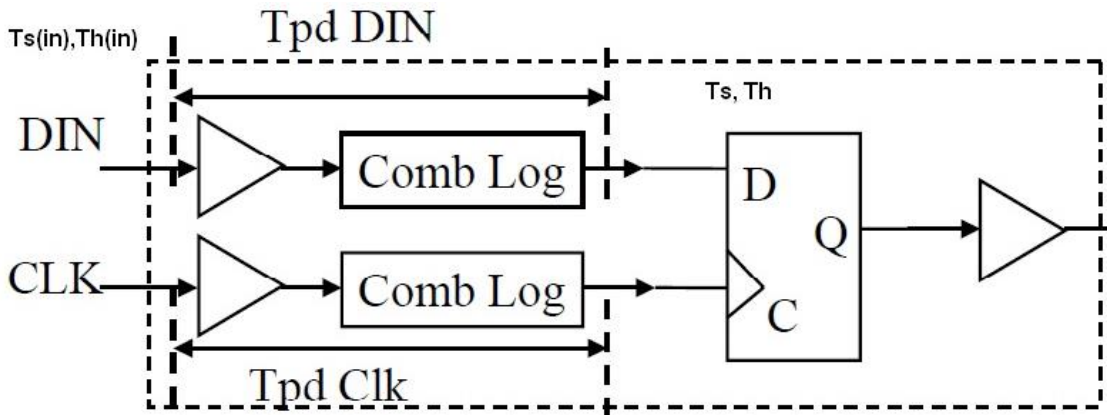
$$T_{clk\text{-}to\text{-}q} + T_{pd} >= T_{hd} + T_{pd}\,(\text{capture path}) - T_{pd}\,(\text{launch path})$$

Summary

- Calculating setup and hold times

$$T_{su}\,(DIN) = Max\ T_{pd}\,(DIN) + T_{su}\,(D) - Min\ T_{pd}\,(Clk)$$

$$T_{hd}\,(DIN) = T_{hd}\,(D) - Min\ T_{pd}\,(DIN) + Max\ T_{pd}\,(Clk)$$



Summary (Cont.)

- Checking setup and hold violations

$$T_{clk\text{-}to\text{-}q} + T_{pd} <= \text{clock period} + T_{pd}\,(\text{capture path}) - T_{pd}\,(\text{launch path}) - T_{su}$$

$$T_{clk\text{-}to\text{-}q} + T_{pd} >= T_{hd} + T_{pd}\,(\text{capture path}) - T_{pd}\,(\text{launch path})$$

Summary (Cont.)

- Calculating minimum clock period
  - Maximum of
    - Flop to flop delays
    - Flop to output delays
    - Input to output delays
    - Input to flop delays

Summary (Cont.)

- Fixing setup violations
  - Decreasing data path delay
  - Using FFs with smaller setup times
  - Increasing clock period
  - Increasing capture path delay
- Fixing hold violations
  - Increasing data path delay
  - Using FFs with smaller hold times
  - Increasing launch path delay