
Sharif University of Technology
Department of Computer Engineering

# Digital System Design
# Introduction

Siavash Bayat-Sarmadi

# Syllabus



- In general
  - Verilog hardware description language (HDL)
  - A glance at FPGAs
  - ASM charts
  - Digital design techniques and considerations
  - Digital design verification (system Verilog)

# Texts and Refs



- Verilog HDL: A Guide to Digital Design and Synthesis, 2nd Edition
  - By: Samir Palnitkar

- http://asic-world.com/

# Course Content



- Intro
- Hierarchical modeling concepts
- Basic concepts
- Module and ports
- Gate level modeling
- Dataflow modeling
- Behavioral modeling
- ASM
- Tasks and functions
- Synthesis
- FSM
- FPGA
- Metastability & CDC
- STA

# Tools



- Modelsim
  - Mentor Graphics
  - A simulation tool
- ISE
  - Xilinx
  - A synthesis tool
- VM
  - Modelsim + Ubuntu 16.04
  - A platform for verification

# Evaluation



- Midterm Exam: 20% (4 marks)
- Practical Exams: 30% (6 marks)
- Final Exam: 30% (6 marks)
- Assignments: 20% (4 marks)
- Total: 100%(20 marks)
- A tentative contest +10% (2 marks)

# Exam Dates and Time

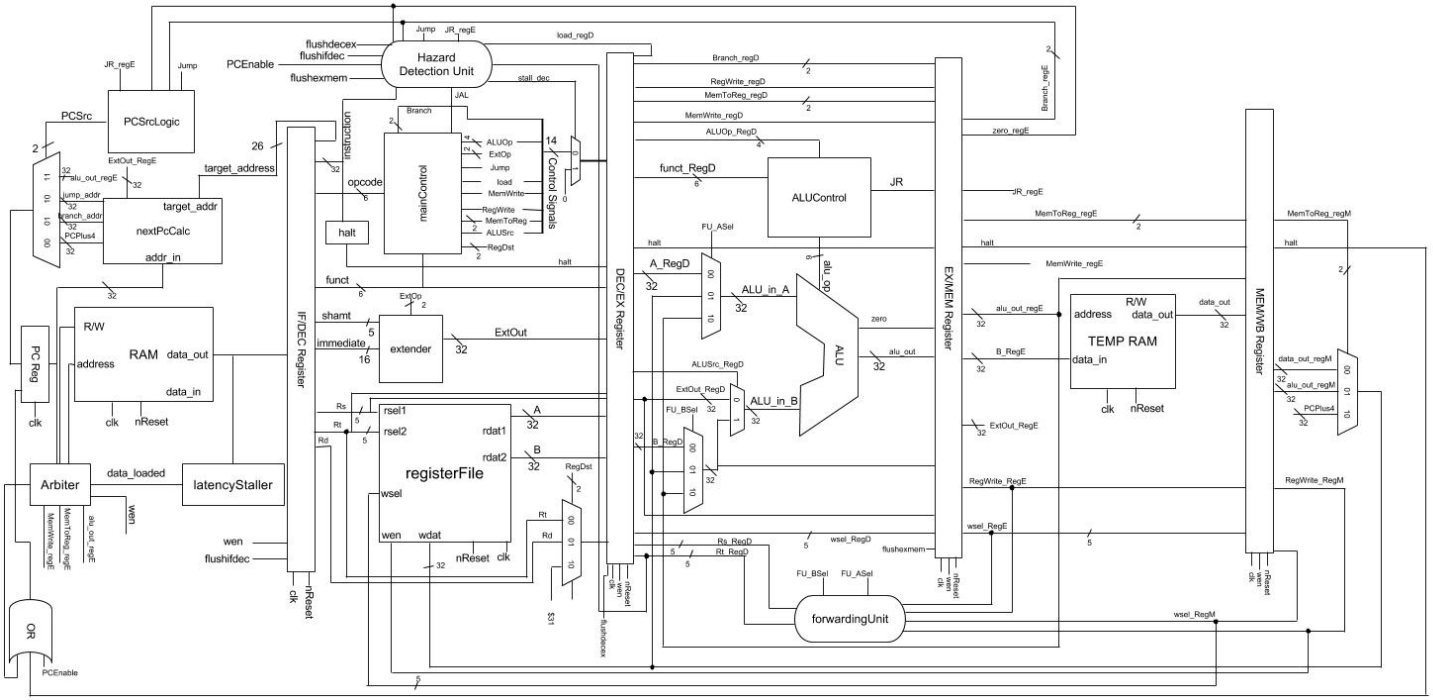


- Midterm Exam: 23 Aban 1398
- Practical Exam 1: 7 Azar 1398
- Practical Exam 2: 21 Azar 1398
- Practical Exam 3: 12 Dey 1398
- Final Exam: 1 Bahman 1398

# Course Project



- Learn and develop a simple 16-bit RISC processor from scratch → In 10 steps
- Review and use the course topics in a real Project



# Tutorials



- Head TA:
  - Farhad Taheri(farhadtaheri@ce)
- Course Website
  - Quera (quera.ir)
    - Password: dsd-fall-98
- Tutorial Date/Time/Room (once required)
  - Tuesdays/ 12-13:30/ Room 201

# Thanks!

# Evolution of Digital Circuits



- Vacuum tubes
- Transistors
- Small Scale Integration (SSI)
- Medium Scale Integration (MSI)
  - 100s of transistors on a chip
- Large Scale Integration (LSI)
  - 1000s
- Very Large Scale Integration (VLSI)
  - 10,000s
  - Computer-Aided Design (CAD)

# Emergence of HDL



- To describe electronic circuits, mainly digital
  - Design
  - Simulation
  - Synthesis

# Verilog HDL



- Verifying Logic
- Originated at Automated Integrated Design Systems (later renamed as **Gateway Design Automation**) in 1985
- Designed by Phil Moorby
- IEEE standard 1995
- Syntax based on C programming language

# VHDL



- VHSIC HDL: Very High Speed Integrated Circuit Hardware Description Language
- By the U.S Department of Defense
  - to document the behavior of the ASICs
- VHDL 7.2 in 1985
- IEEE standard in 1987
- ANSI standard in 1988
- Syntax based on Ada programming language

# Verilog vs. VHDL



| Verilog | VHDL |
| --- | --- |
| Designed for hardware design | Desgined for documentation |
| User defined data types are not allowed | User defined data types are allowed |
| Low level construct | High level construct |
| No concept of a library | Library |
| Powerful PLI | No PLI |
| Case-sensitive | Not case-sensitive |
| More popular in USA | More popular in Europe |

# Hello World!!!



**Verilog**

```
module hello_world;
initial begin
$display(
"Hello World");
#10 $finish;
end
endmodule
```

**VHDL**

```
entity hello_world is
end;
architecture
hello_world of
hello_world is begin
stimulus:process
Begin
assert flase report
"Hello World"
severity note;
wait;
end process stimulus;
end hello_world;
```

www.asic-world.com

# Other HDL example



- Digital: ABEL, AHDL, etc.
- Analog: Verilog-AMS, HDL-A, etc.

# Level of Modelling in Verilog



- Behavioral level
  - Functionality
  - No hardware details
- Dataflow level
  - How data processed
- Gate level
  - Wiring between gates
- Switch level
  - Using transistors

RTL, a mixture of behavioral and dataflow descriptions

# HDL Considerations



- Early verification
- Design hierarchy
- Independence of fabrication technology
- Concurrency
- Timing

# VLSI Design Flow