Sharif University of Technology
Department of Computer Engineering

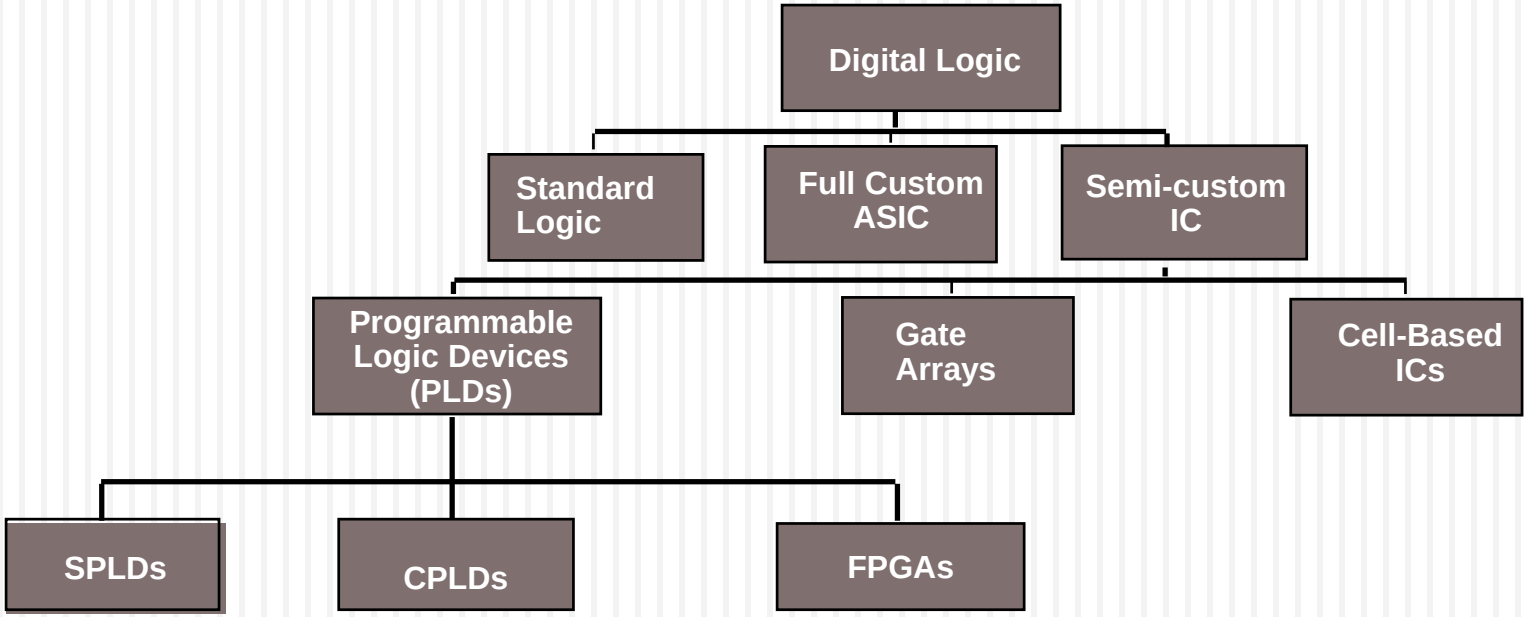
Digital System Design
FPGAs

Siavash Bayat-Sarmadi

Digital Logic Implementation

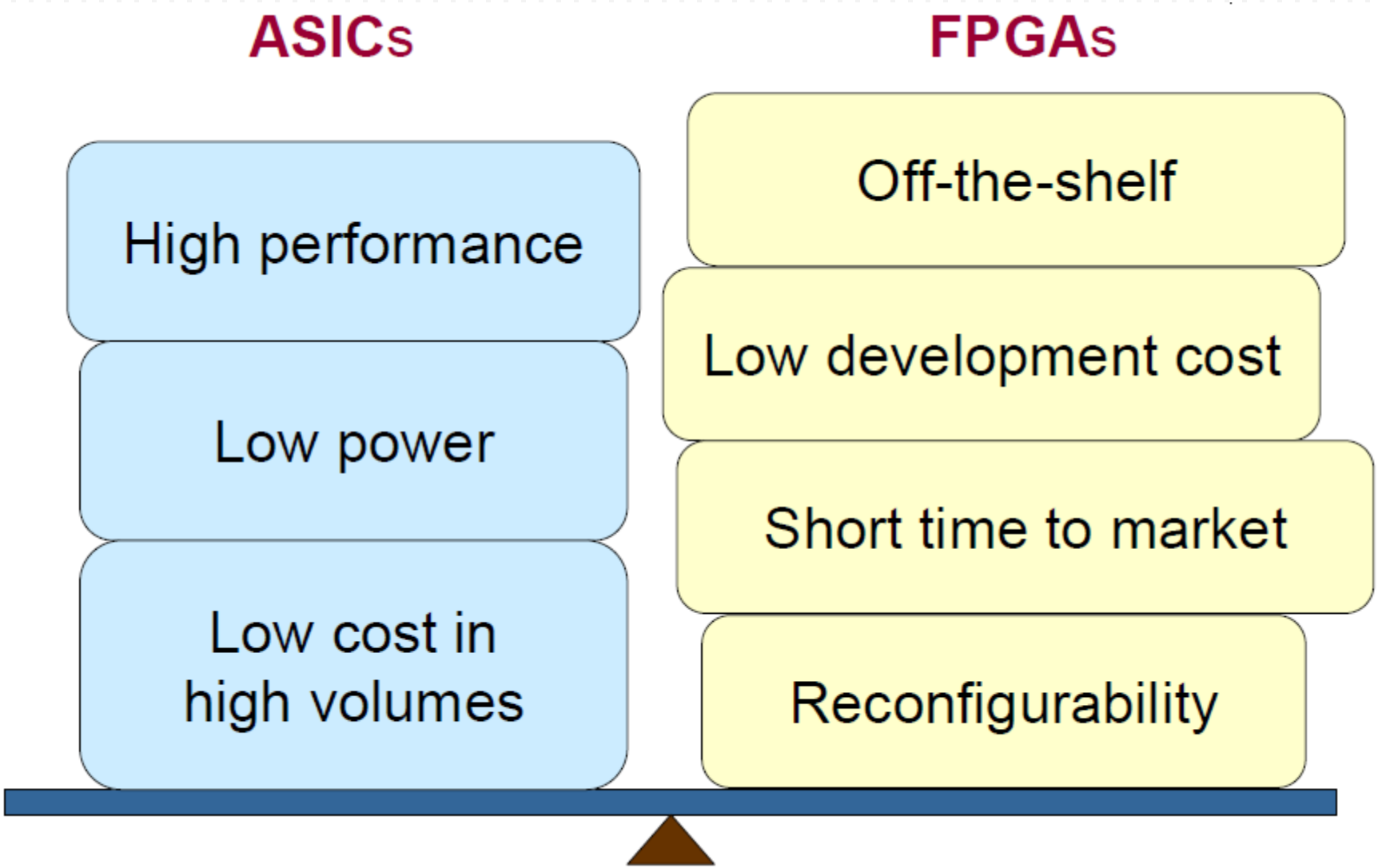
- SPLD (simple programmable logic device)
- CPLD (complex programmable logic device)
- FPGA (Field- Programmable Gate Array)
  - Blocks
    - Logic Block
    - LUT (Look Up Table)
    - I/O (Input,Output)
  - Configuration
  - Examples
    - Xilinx
    - Altera

Digital logic Implementation



Not Programmable	Factory Programmable	Programmable
• Standard Logic • Full Custom ASIC	• Gate Arrays • Cell-Based ICs	• PLDs

ASIC vs FPGA


ASICs
FPGAs
High performance
Low power
Low cost in high volumes
Off-the-shelf
Low development cost
Short time to market
Reconfigurability

ASIC vs FPGA

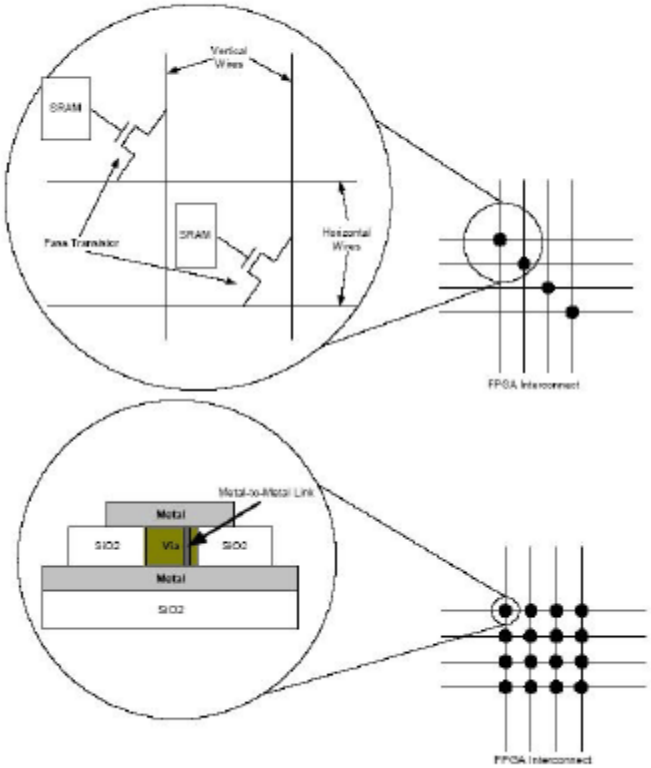
- Manufacturing cycle for ASIC is very costly, lengthy and engages lots of manpower
  - Mistakes not detected at design time have large impact on development time and cost
  - FPGAs are perfect for rapid prototyping of digital circuits
- Easy upgrades like in case of software
- Unique applications
  - reconfigurable computing

PLDs

- SPLD
  - Read Only Memory (ROM)
  - Programmable Logic Array (PLA)
  - Programmable Array Logic (PAL)
- Complex Programmable Logic Device (CPLD)
- Field- Programmable Gate Array (FPGA)

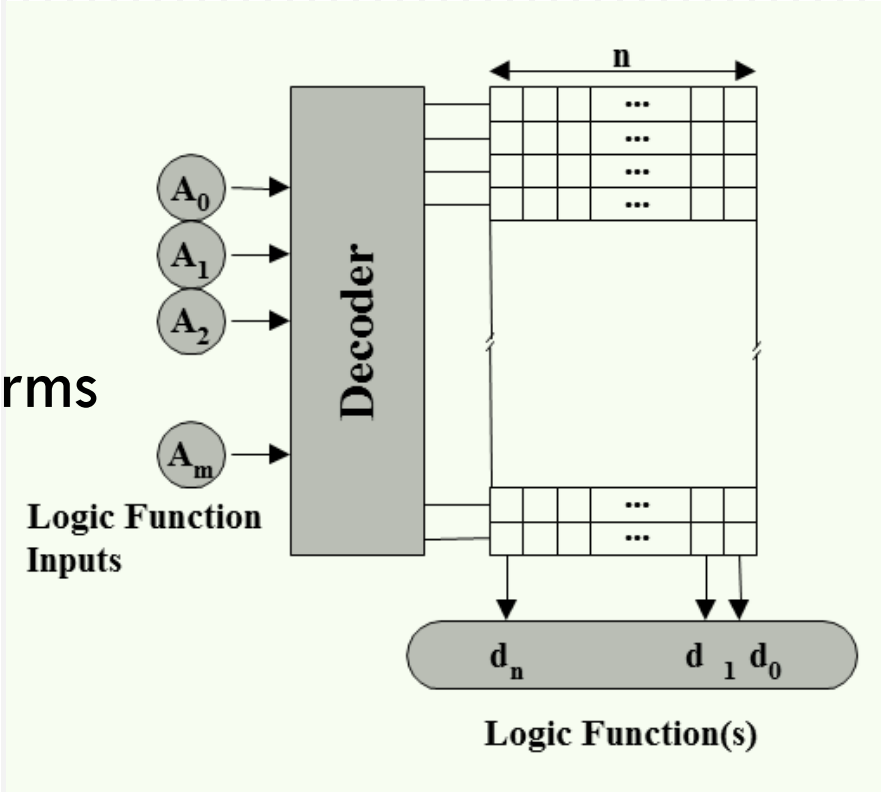
How can we make a programmable logic?

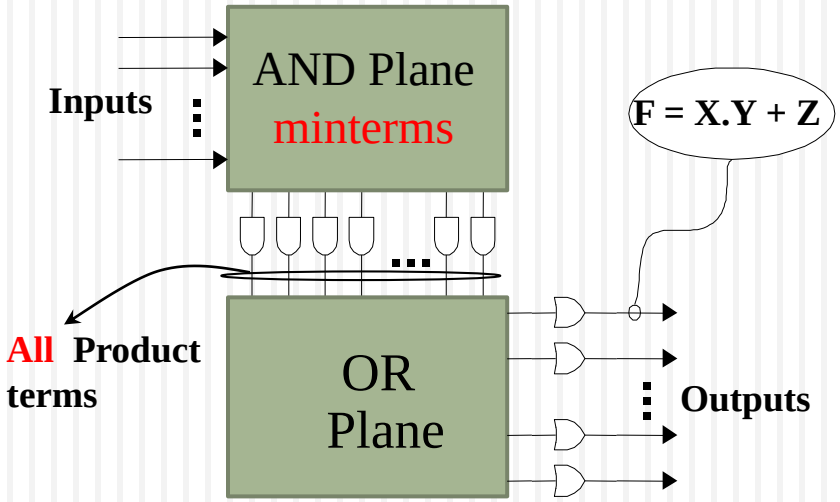
- SRAM-based
  - Reconfigurable
  - Track latest SRAM technology
  - Volatile
  - Generally high power
- Anti-fuse technique
  - One-time programmable
  - Non-volatile – security app.



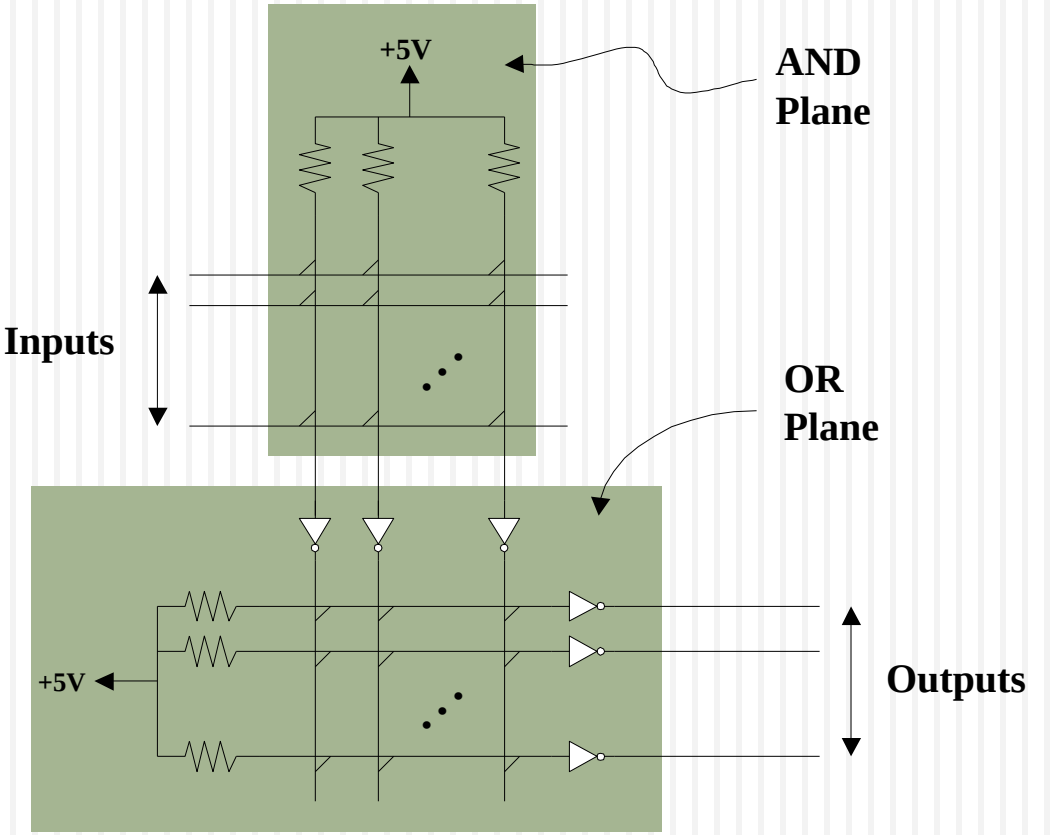
Read Only Memory (ROM)

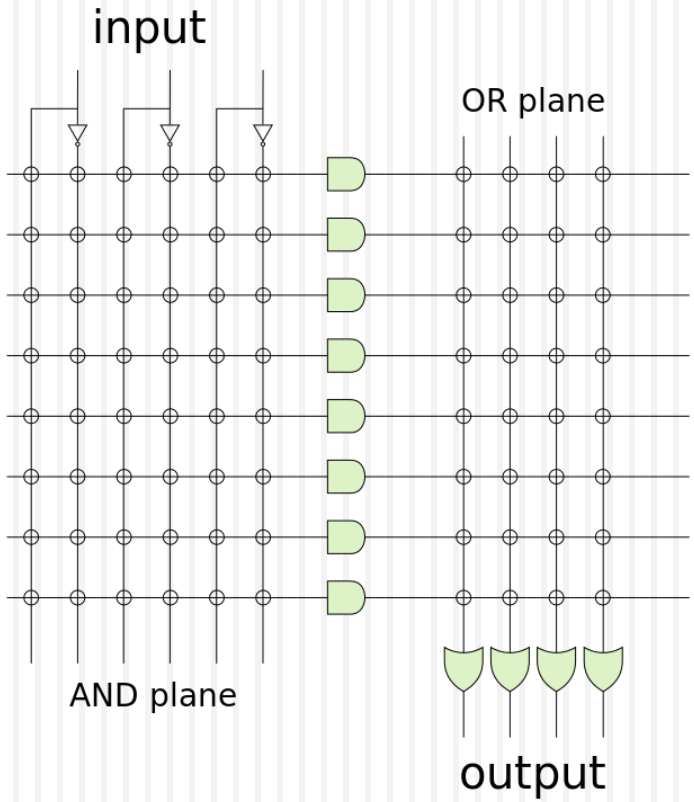
- AND plane feeding a programmable OR plane
- A special kind of Memory
- Advantages:
  - High number of inputs
  - High number of product terms





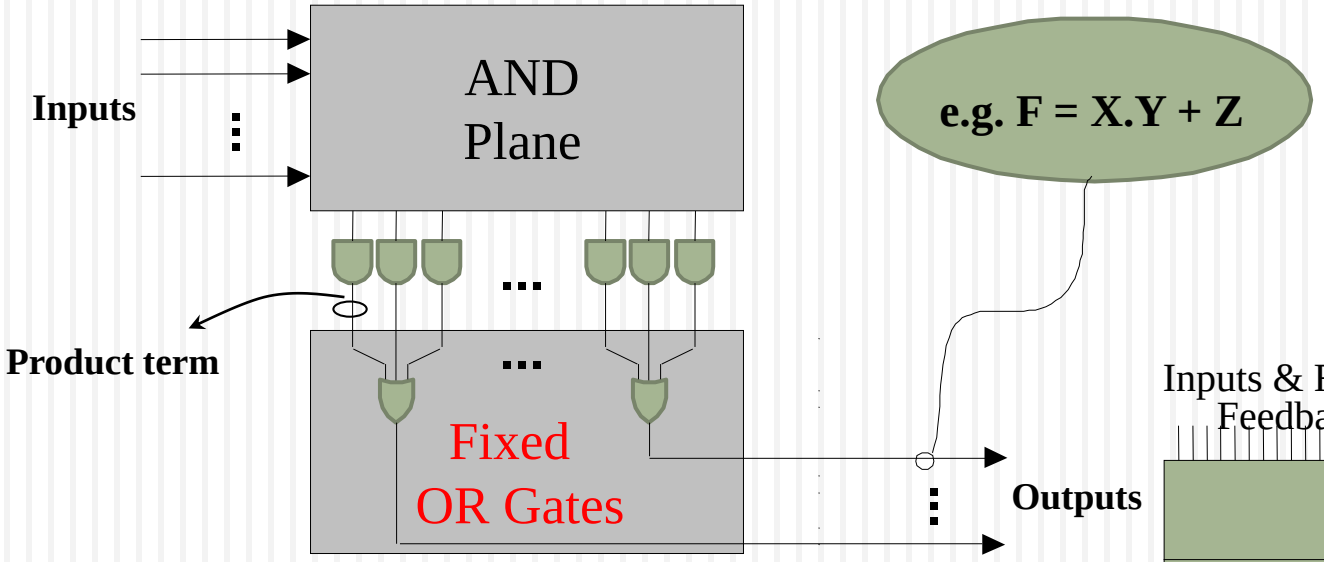
Programmable Logic Array (PLA)

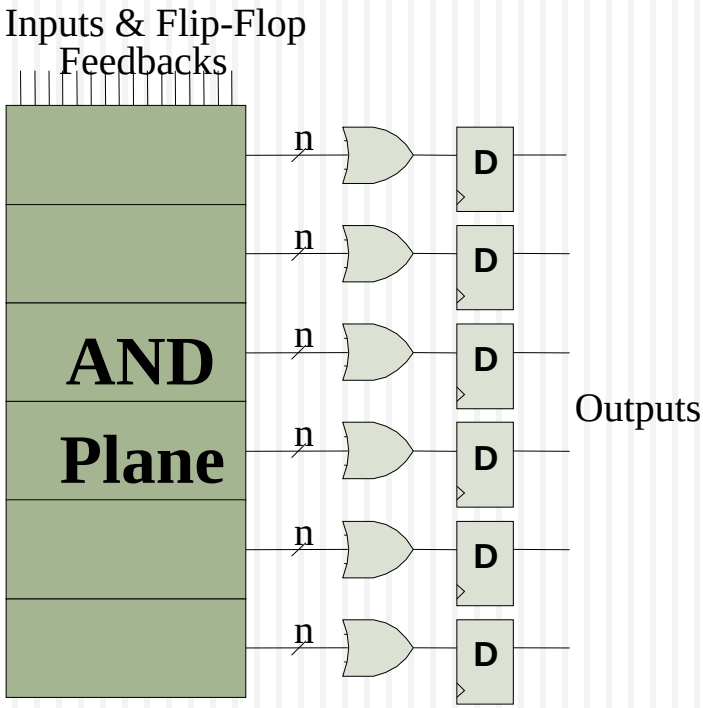




AND and OR planes are implemented using wired-AND

Programmable Array Logic (PAL)





- Cons of 2 programmable planes
  1. Higher cost
  2. higher delay
- PAL = PLA with fixed OR plane
- PAL is faster than PLA

Summary of SPLDs

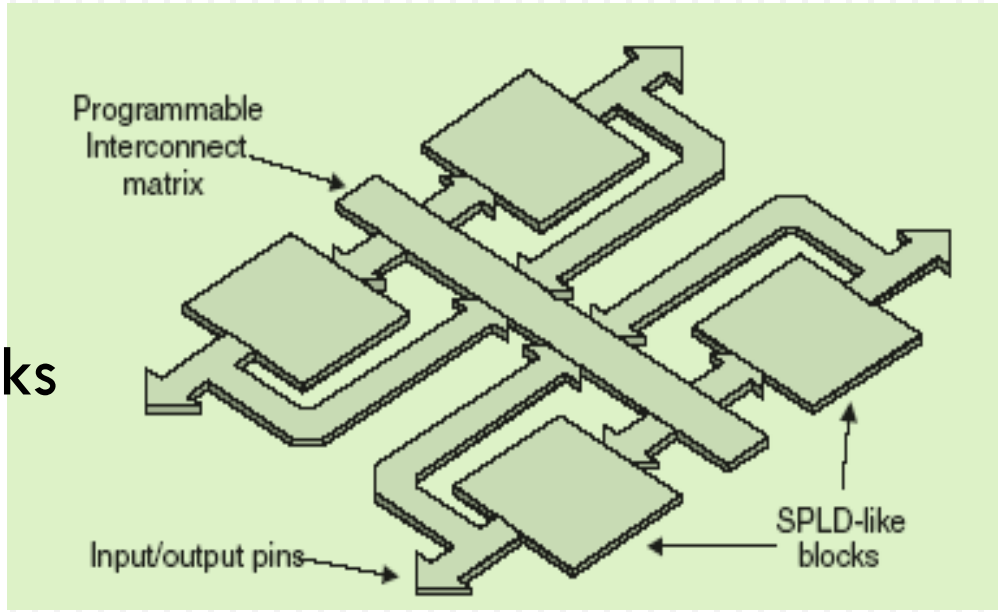
- Typical capacity: ~200 Gates
- PLA: Most flexible, low speed
- PROM: Fixed AND plane
- PAL: Fixed OR plane
- Not scalable due to structure
- Typical use:
  - Control circuitry
  - Glue logic
  - FSM
- Products from:
  - AMD, Altera, Atmel, Cypress, ICT, Lattice, Philips

Summary of SPLDs Cont'd

- SPLDs are inexpensive
  - $1 to $15 each (typically)
- SPLD CAD tools are inexpensive
- SPLDs are fast
  - 4ns to 35ns pin-to-pin
- Programming technology
  - OTP: fuse
  - EPROM/EEPROM transistors

Complex Programmable Logic Device

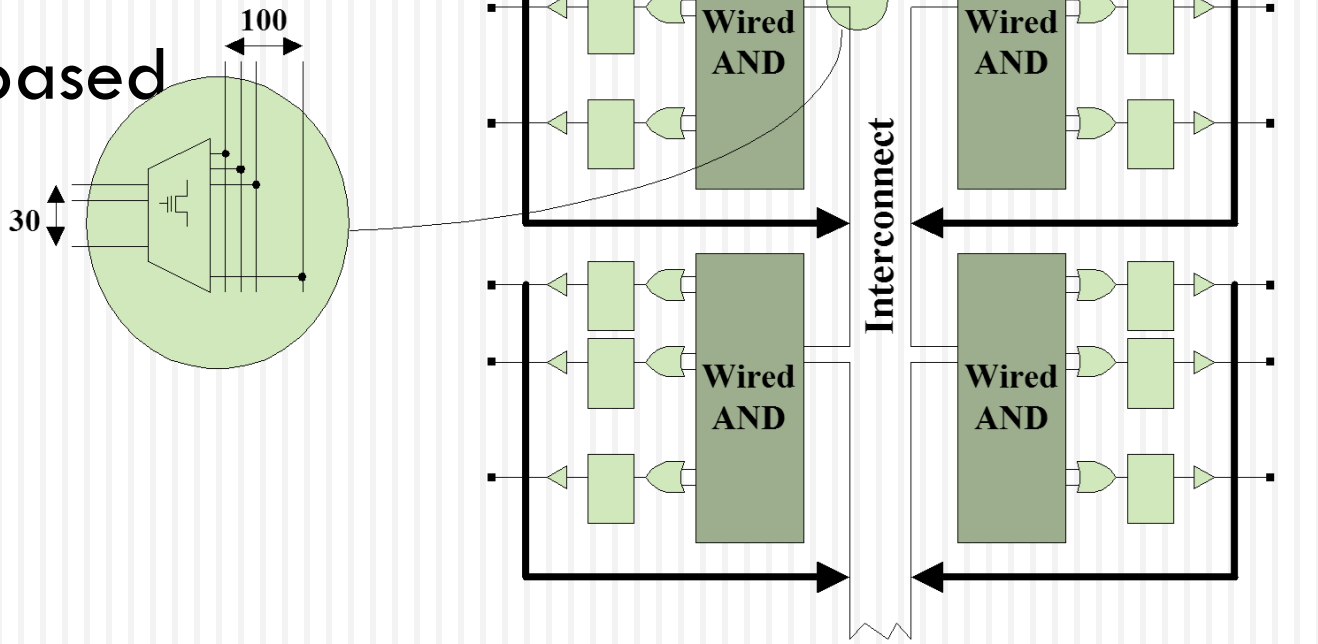
- CPLDs
  - Programmable PLD Blocks
  - Programmable Interconnects
  - Electrically Erasable links



CPLD Architecture

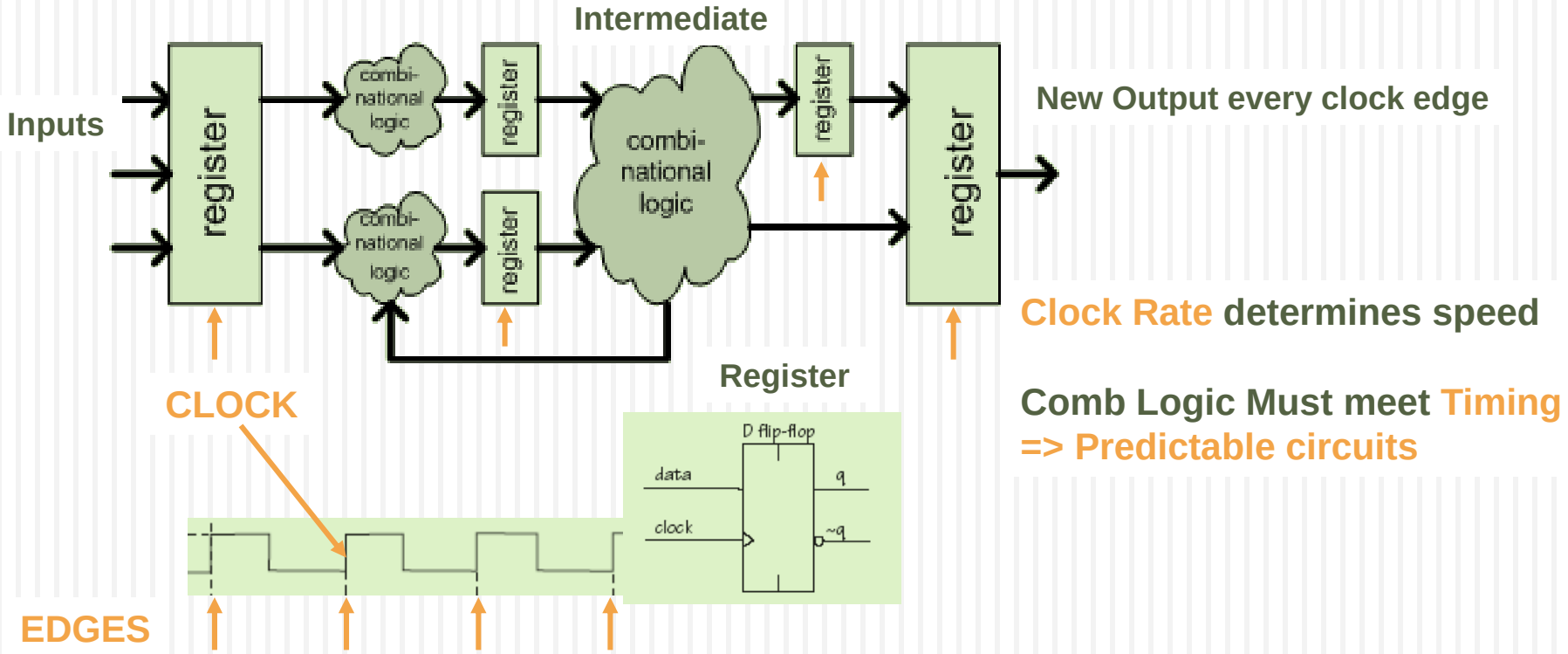
CPLD Cont'd

- Contains an arrangement of multiple PAL-like blocks
- Programming Technology:
  - EPROM, EEPROM
  - SRAM-based



Sequential Circuits

- Combinational Logic (Larger circuits difficult to predict)
- Synchronous Logic driven by a CLOCK
- Registers, Flip Flops (Memory)



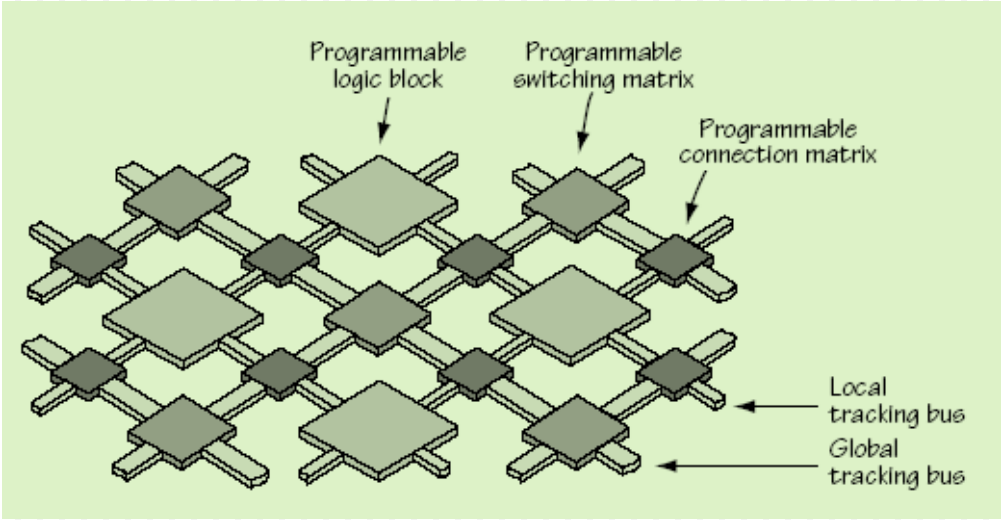
FPGAs

- Field Programmable Gate Array
  - 'Simple' Programmable Logic Blocks
  - Massive Fabric of Programmable Interconnects
  - Standard CMOS Integrated Circuit fabrication process as for memory chips

Huge Density of Logic Block 'Islands'

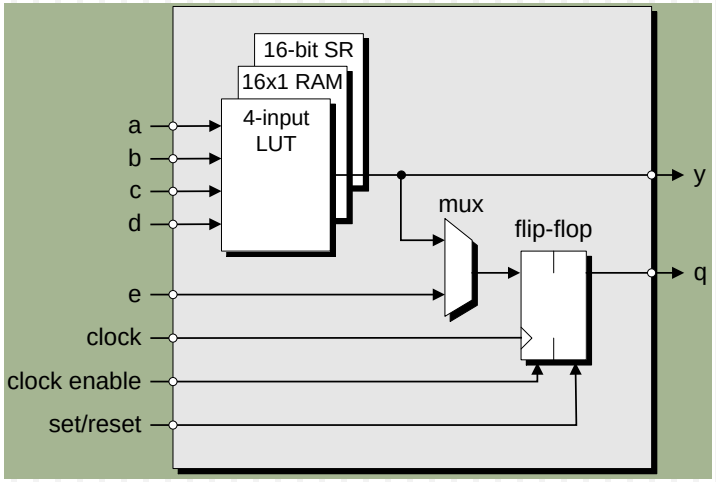
1,000 … 100,000's

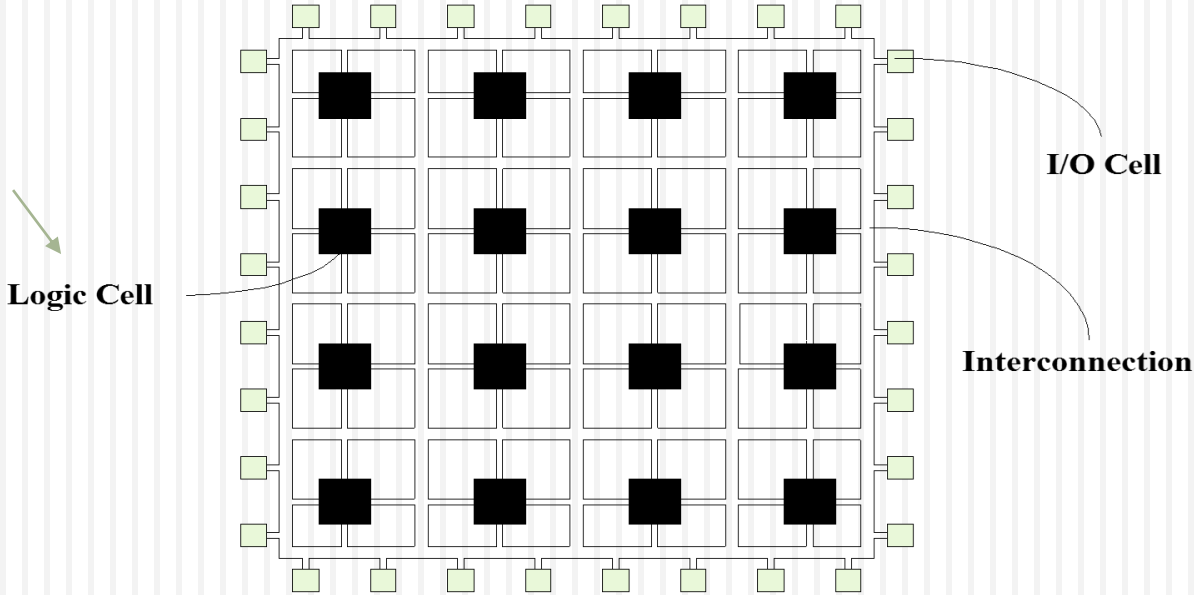
in a 'Sea' of Interconnects



FPGAs Cont'd

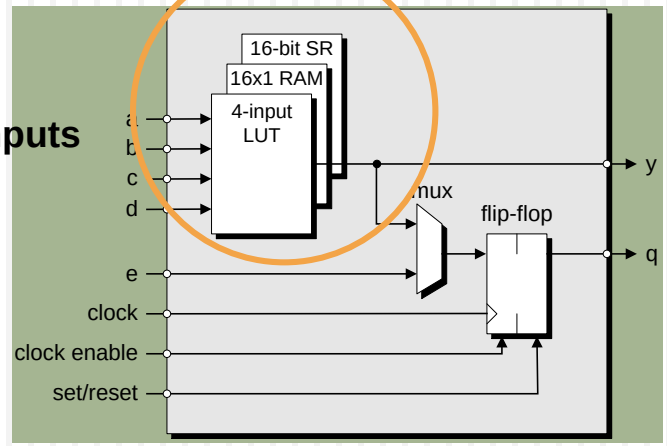
- Logic Blocks
  - Logic Functions implemented in Look Up Table LUTs.
  - Flip-Flops. Registers. Clocked Storage elements.
  - Multiplexers (select 1 of N inputs)

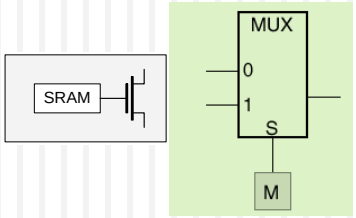




FPGAs Cont'd

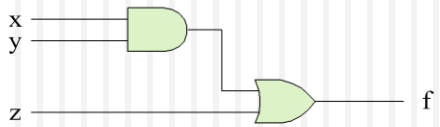
- Look Up Tables
  - LUT contains Memory Cells to implement small logic functions (SRAM)
  - Each cell holds '0' or '1' .
  - Programmed with outputs of Truth Table
  - Inputs select content of one of the cells as output

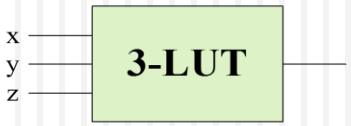




LUT Cont'd

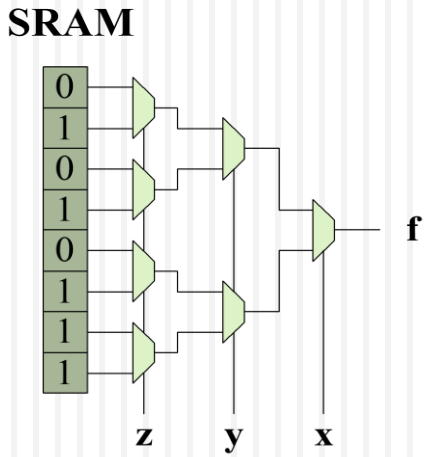
- Example
  - F = xy + z





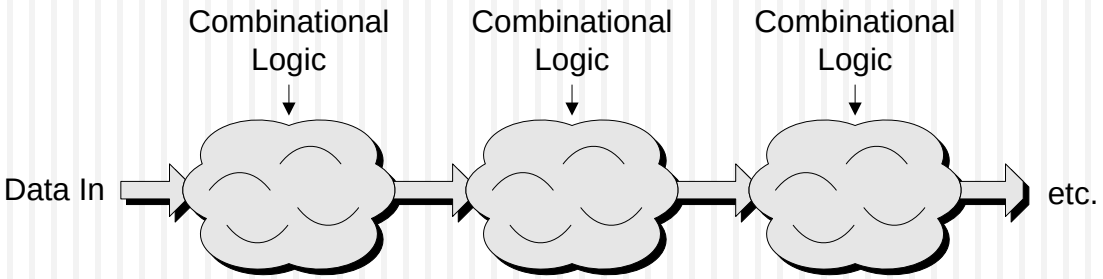
Truth Table

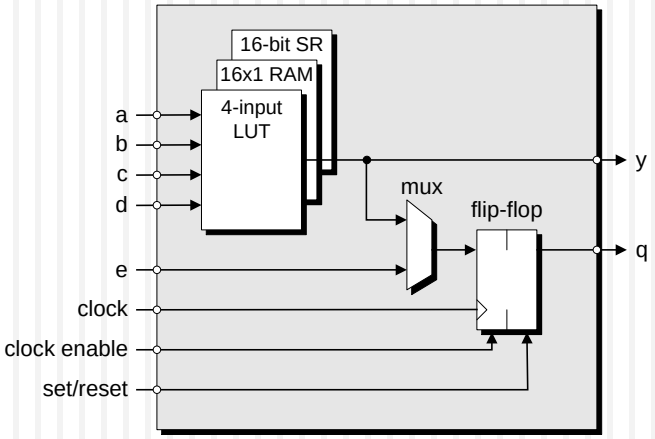
x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



LUT Cont'd

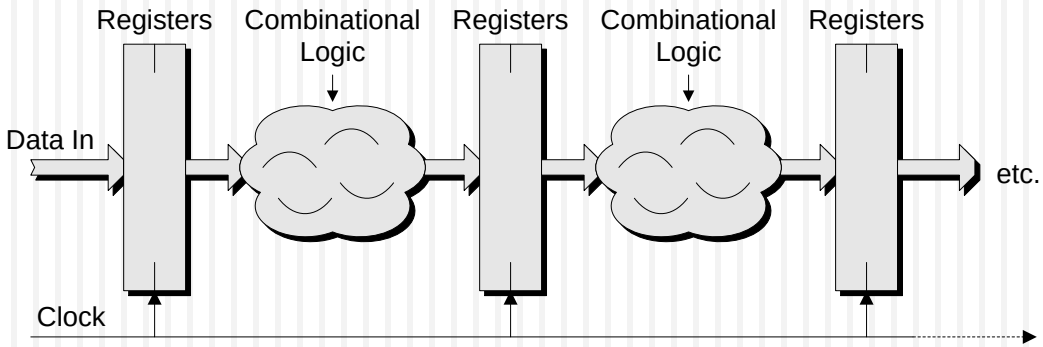
Larger Logic Functions built up by connecting many Logic Blocks together

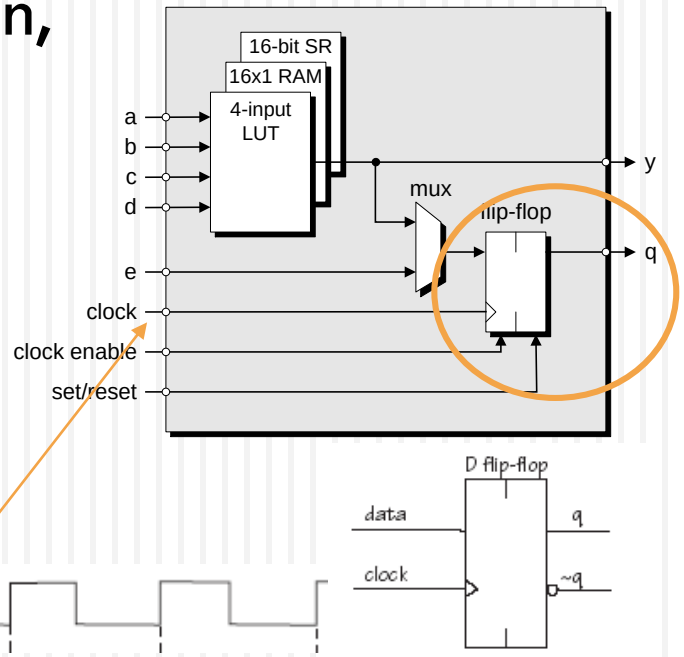




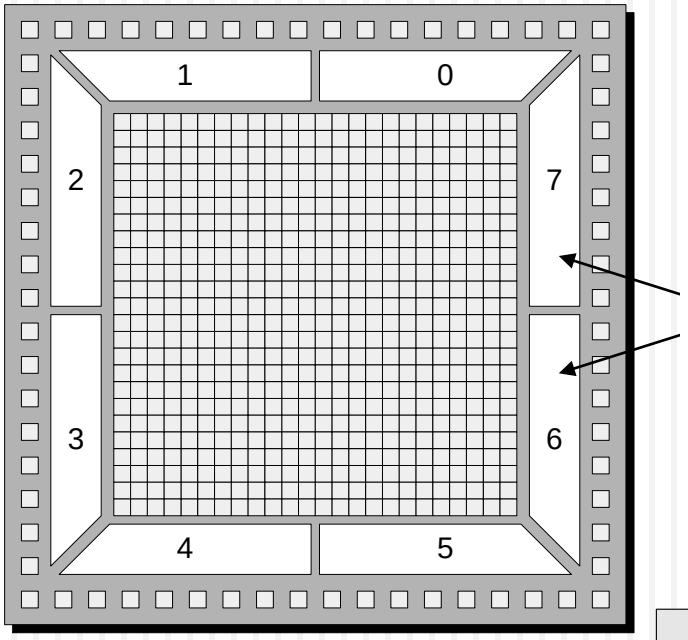
FPGAs Cont'd

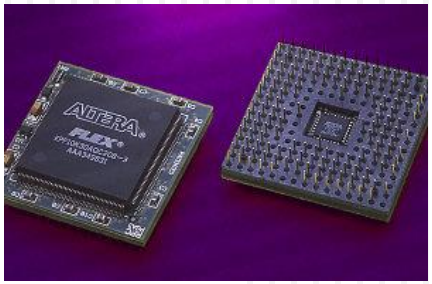
- Clocked Logic
  - Registers on outputs. CLOCKED storage elements.
  - Synchronous FPGA Logic Design, Pipelined Logic.





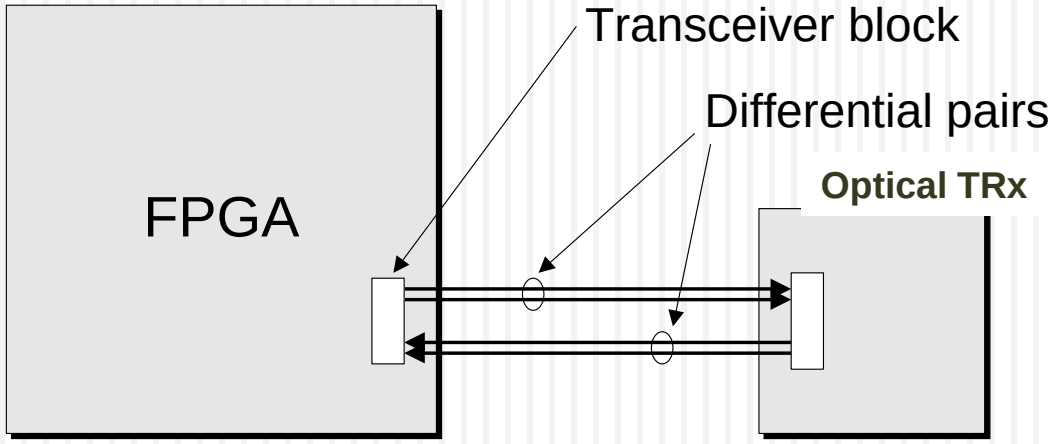
FPGAs Cont'd





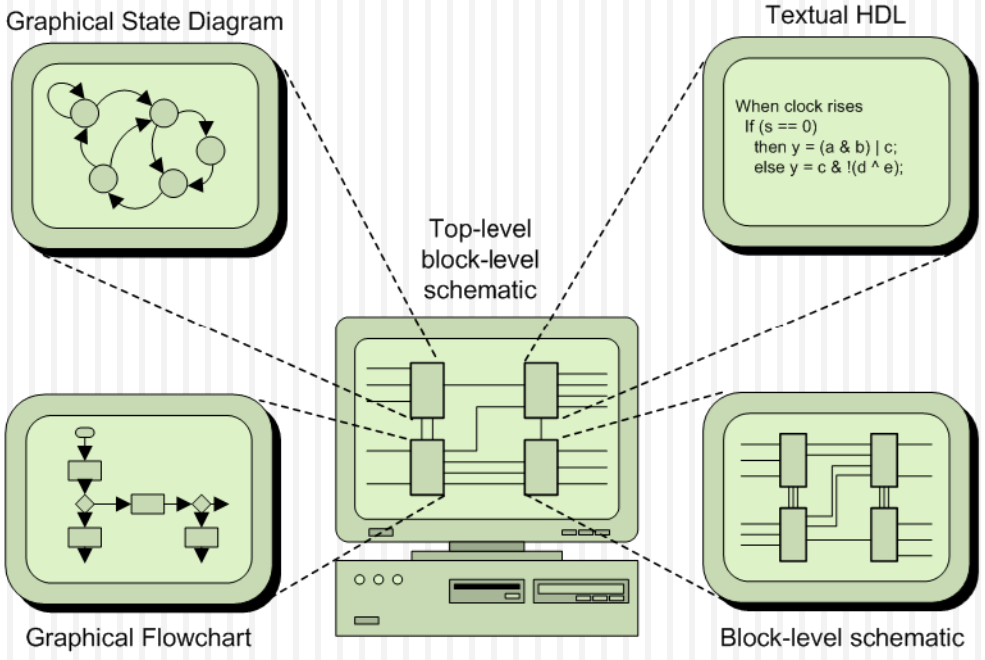
Up to > 1,000 I/O "pins" (several 100 MHz)

Special I/O SERIALISERS
~ 10 Gbps transfer rates



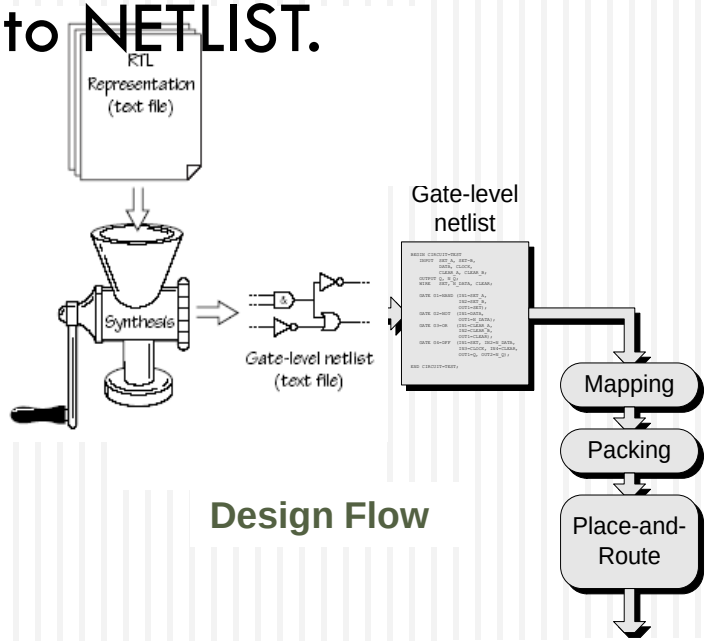
Designing Logic with FPGAs

- Design Capture.
- High level Description of Logic Design.
  - Graphical descriptions
  - Hardware Description Language (Textual)



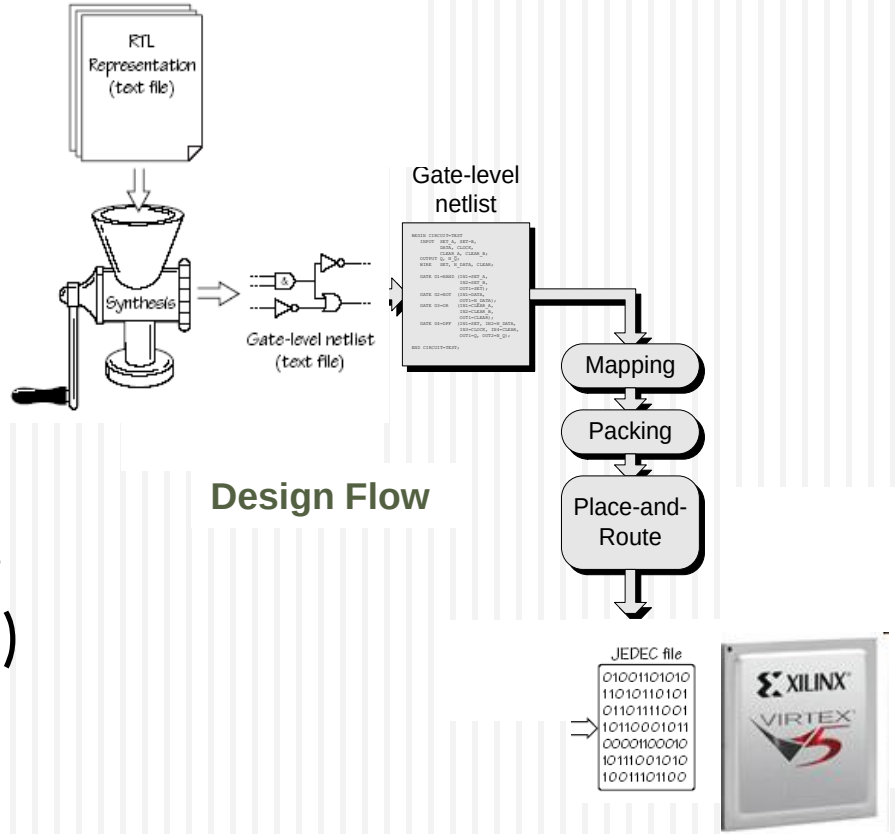
Designing Logic with FPGAs (Cont'd)

- High level Description of Logic Design
  - Hardware Description Language (Textual)
- Compile (Synthesis) into NETLIST.
- Boolean Logic Gates.



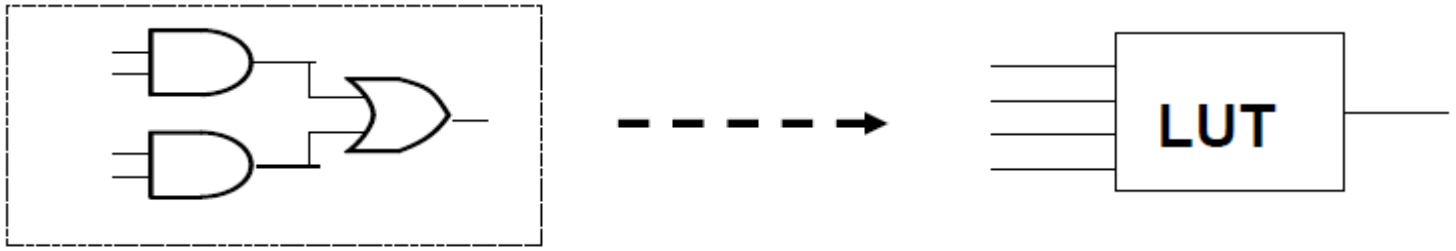
Designing Logic with FPGAs (Cont'd)

- Target FPGA Device
  - Mapping
  - Routing
- Bit File for FPGA
  - Configuration bits
- Commercial CAD Tools (Complex & Expensive)
- Logic Simulation

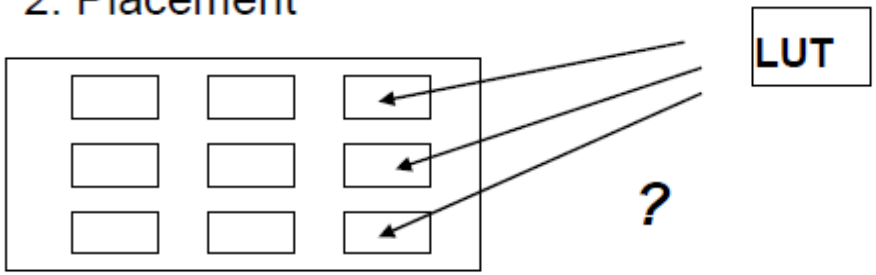


Designing Logic with FPGAs (Cont'd)

1. Technology Mapping

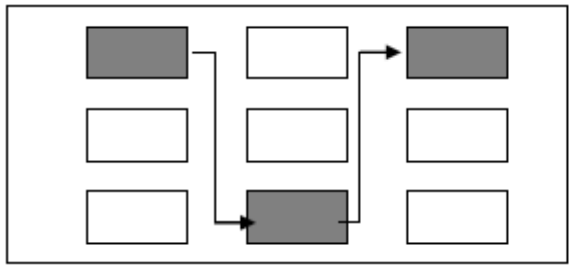


2. Placement



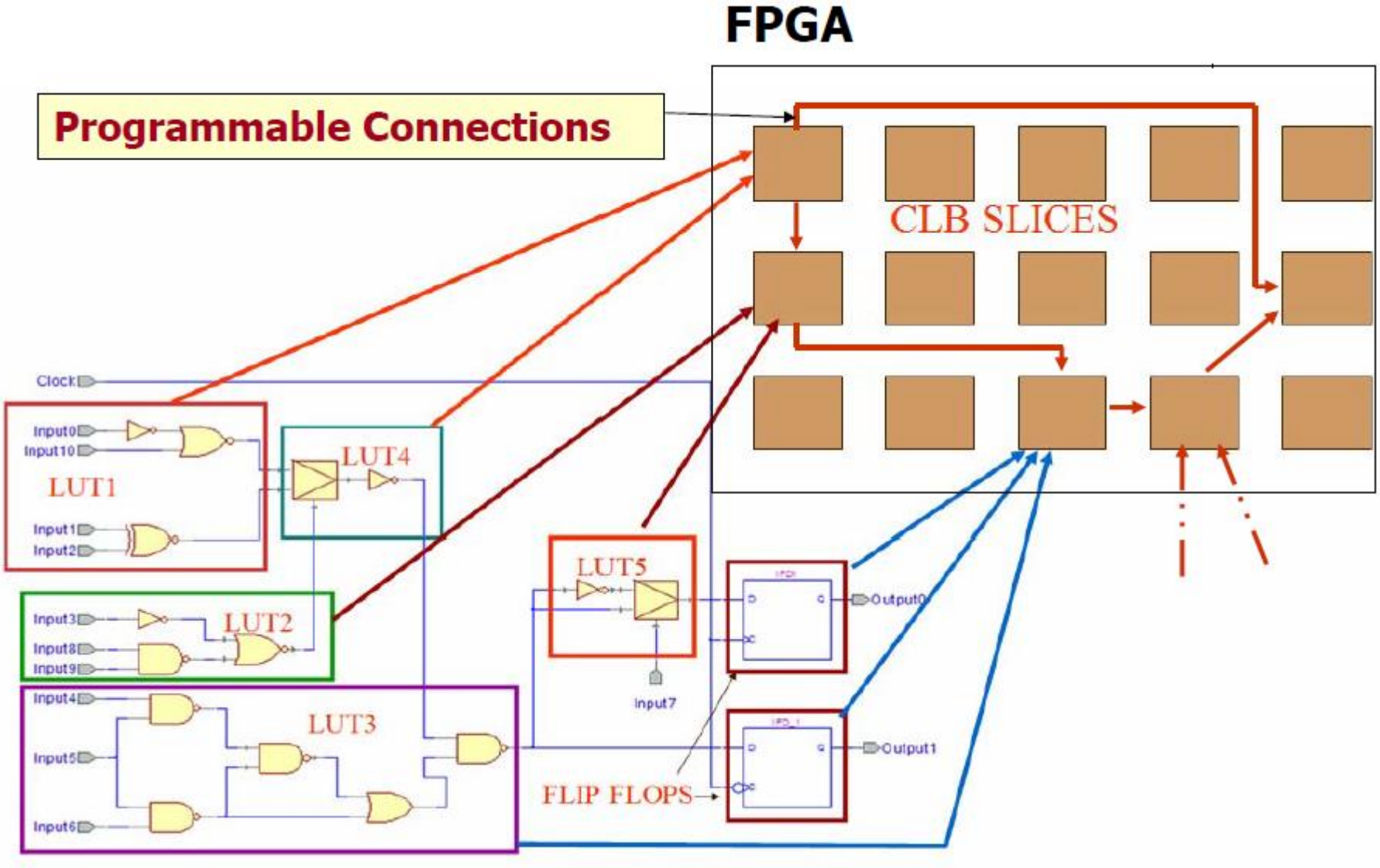
Assign a logical LUT to a physical location.

3. Routing



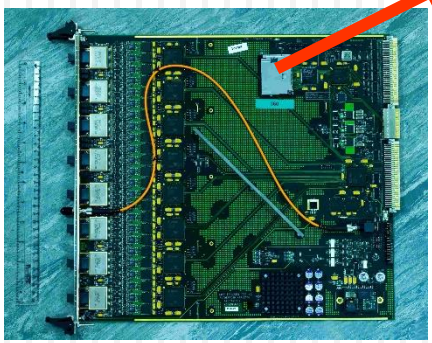
Select wire segments And switches for Interconnection.

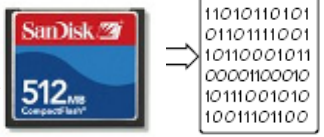
Routing Example



Configuring an FPGA Cont'd

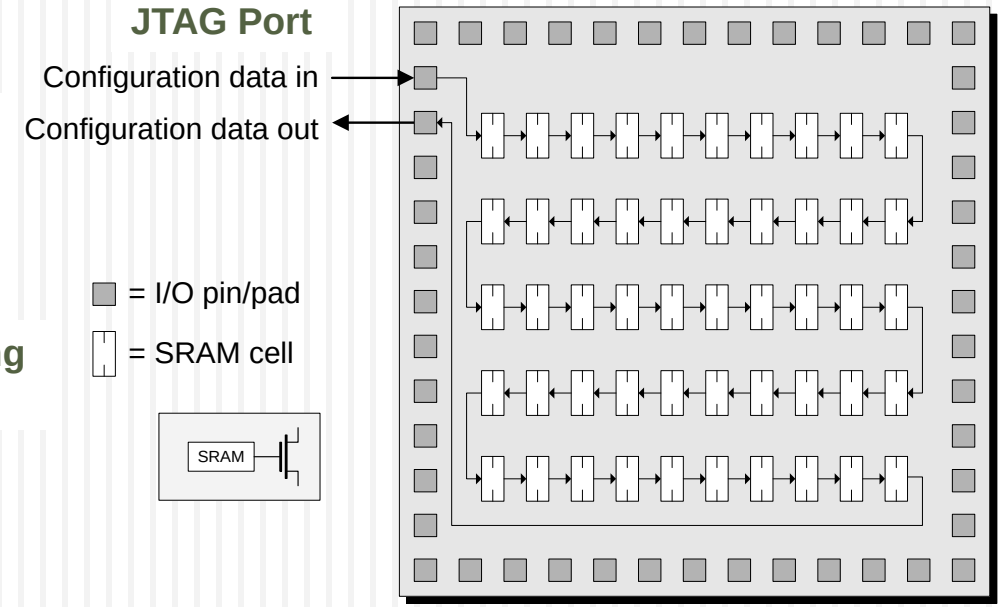
- Millions of SRAM cells holding LUTs and Interconnect Routing
- Volatile Memory. Lose configuration when board power is turned off.





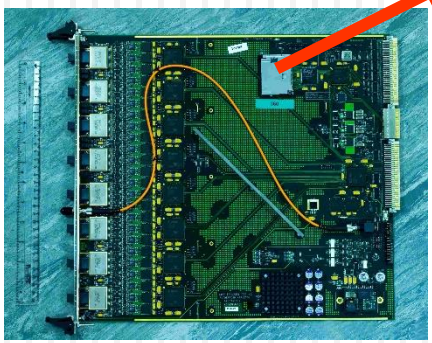
Programming Bit File

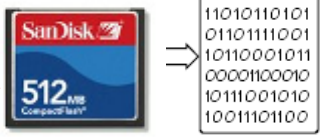
JTAG Testing



Configuring an FPGA

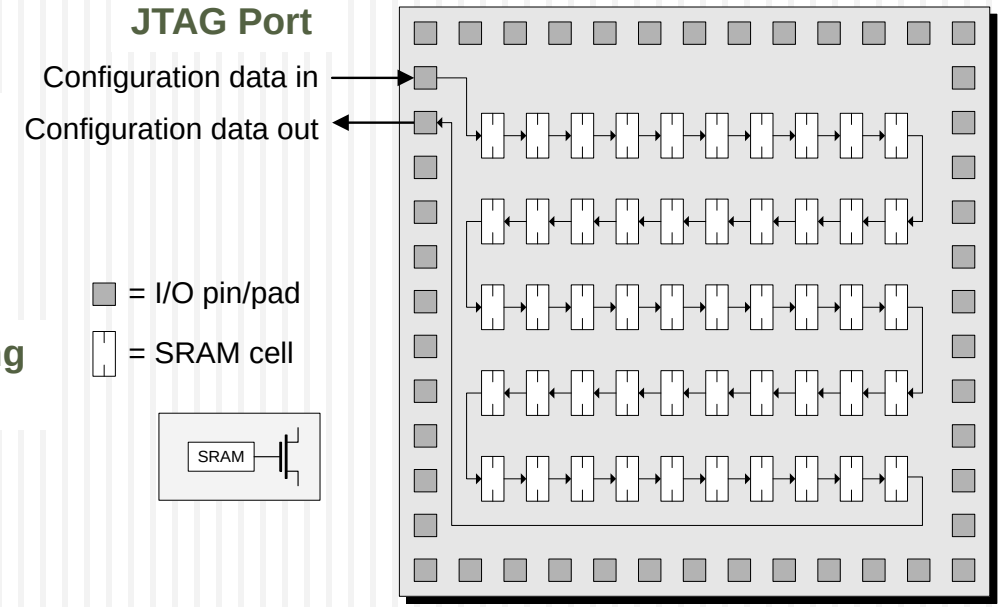
- Keep Bit Pattern describing the SRAM cells in non-Volatile Memory e.g. PROM or Digital Camera card
- Configuration takes ~ seconds





Programming Bit File

JTAG Testing



Major FPGA Vendors

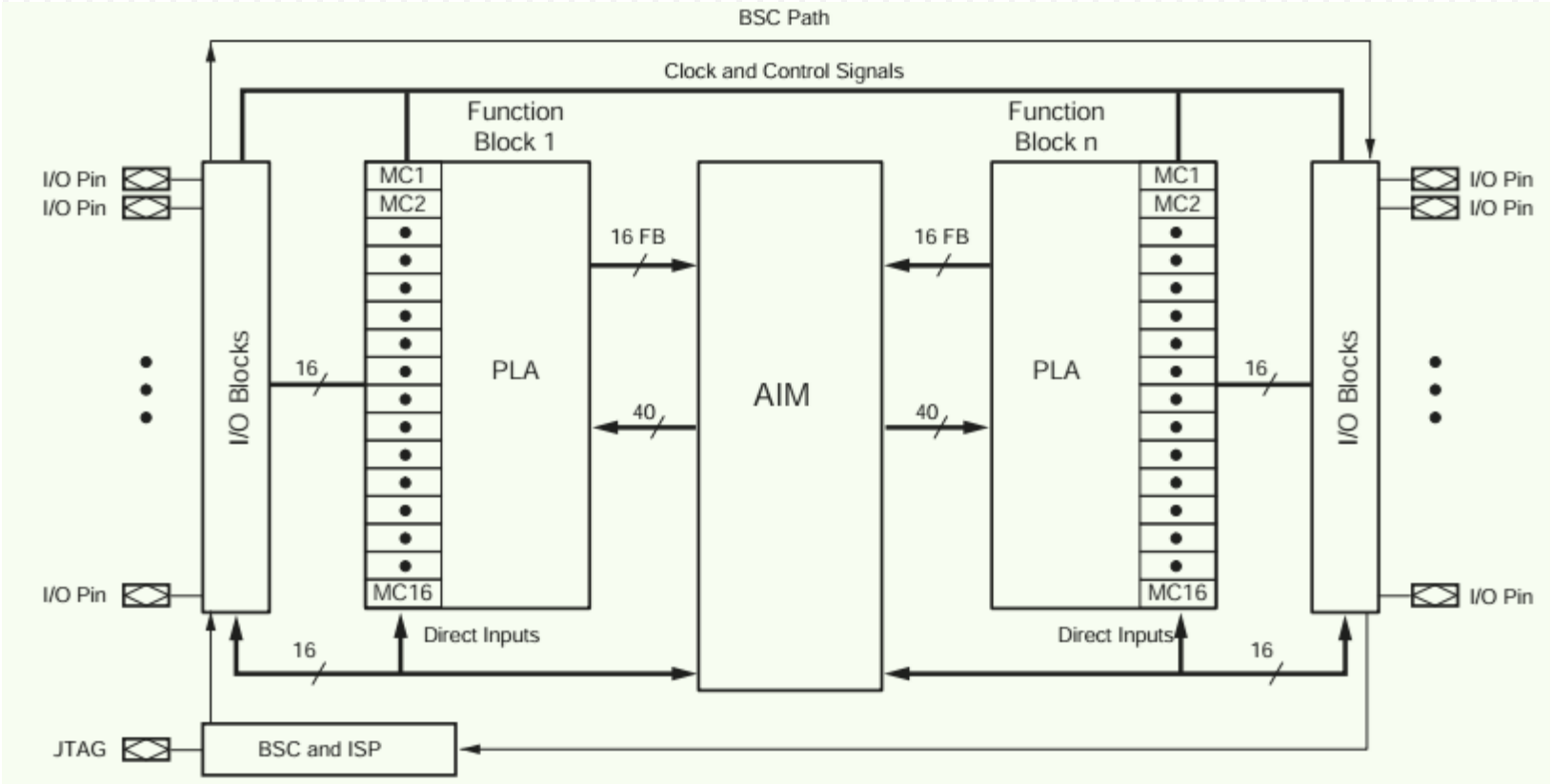
- Top FPGA companies
  - SRAM-based FPGAs
    - Xilinx
    - Altera
    - Lattice Semiconductor
  - Flash & antifuse FPGAs
    - Microsemi (was Actel)
    - QuickLogic

Xilinx CPLD

- Cool Runner II
  - PLA (instead of PAL) for SPLD-like blocks
  - Low power (1.8V)
  - 0.18u process
  - ISP (In-System Programmable) through JTAG
  - OTF (On-The-Fly reconfiguration)
    - = Partial reconfiguration
    - 50-300us transition time

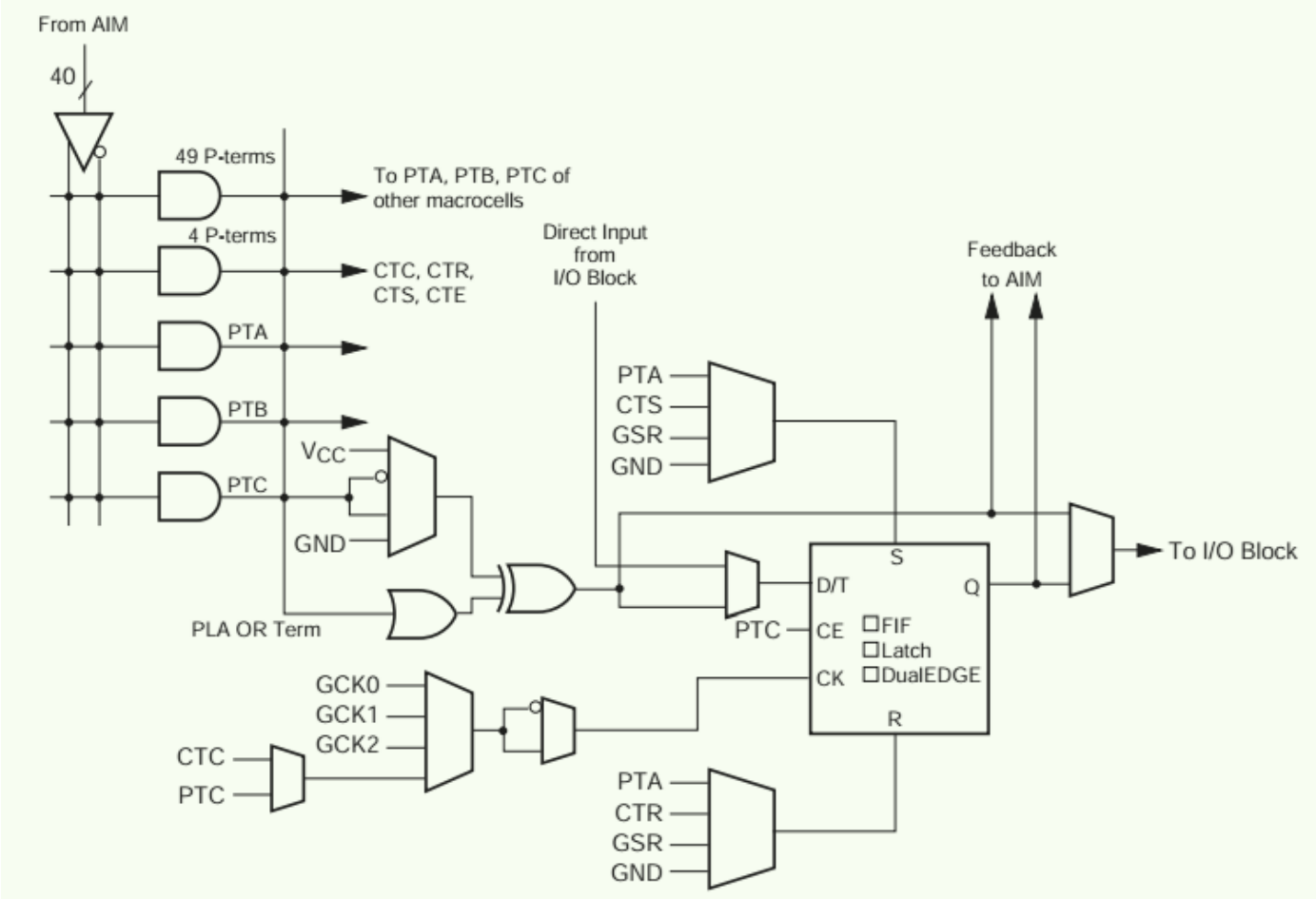
Xilinx CPLD Cont'd

- Xilinx Cool Runner-II Internals



Xilinx CPLD Cont'd

- Xilinx Cool Runner-II Macro cell



Xilinx FPGAs

- FPGAs
  - Artix (Low end)
    - Machine vision camera
  - Kintex (Mid range)
    - 3G/4G wireless, VOIP solutions
  - Virtex (High end)
    - 10G/100G networking, ASIC prototyping
- 3D-ICs
- EasyPath
- Family numbers
  - II, …, 5, 6, 7

Xilinx FPGAs Cont'd

- 3D-ICs: Xilinx UltraScale family
  - More connectivity
  - More connection bandwidth
  - Extends both Virtex and Kintex architectures

Xilinx FPGAs Cont'd

- Latest Products

Table 2: **Artix-7 FPGA Feature Summary by Device**

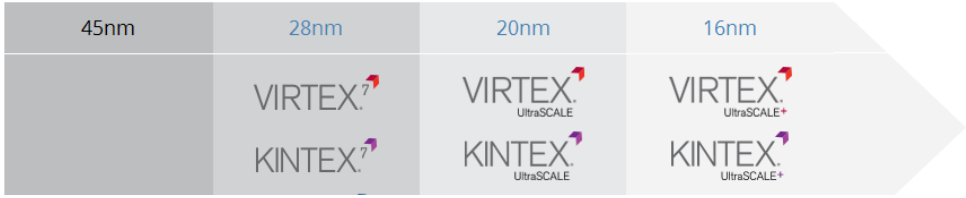
Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices(2)	Block RAM Blocks(3)			CMTs(4)	PCIe(5)	GTPs	XADC Blocks	Total I/O Banks(6)	Max User I/O(7)
		Slices(1)	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7A15T	16,640	2,600	200	45	50	25	900	5	1	4	1	5	250
XC7A35T	33,280	5,200	400	90	100	50	1,800	5	1	4	1	5	250
XC7A50T	52,160	8,150	600	120	150	75	2,700	5	1	4	1	5	250
XC7A75T	75,520	11,800	892	180	210	105	3,780	6	1	8	1	6	300
XC7A100T	101,440	15,850	1,188	240	270	135	4,860	6	1	8	1	6	300
XC7A200T	215,360	33,650	2,888	740	730	365	13,140	10	1	16	1	10	500

Notes:

1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains one MMCM and one PLL.
5. Artix-7 FPGA Interface Blocks for PCI Express support up to x4 Gen 2.
6. Does not include configuration Bank 0.
7. This number does not include GTP transceivers.

Xilinx FPGAs Cont'd

- Latest Products



Kintex-7 FPGA Feature Summary

Table 4: **Kintex-7 FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices(2)	Block RAM Blocks(3)			CMTs(4)	PCIe(5)	GTXs	XADC Blocks	Total I/O Banks(6)	Max User I/O(7)
		Slices(1)	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7K70T	65,600	10,250	838	240	270	135	4,860	6	1	8	1	6	300
XC7K160T	162,240	25,350	2,188	600	650	325	11,700	8	1	8	1	8	400
XC7K325T	326,080	50,950	4,000	840	890	445	16,020	10	1	16	1	10	500
XC7K355T	356,160	55,650	5,088	1,440	1,430	715	25,740	6	1	24	1	6	300
XC7K410T	406,720	63,550	5,663	1,540	1,590	795	28,620	10	1	16	1	10	500
XC7K420T	416,960	65,150	5,938	1,680	1,670	835	30,060	8	1	32	1	8	400
XC7K480T	477,760	74,650	6,788	1,920	1,910	955	34,380	8	1	32	1	8	400

Notes:

1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains one MMCM and one PLL.
5. Kintex-7 FPGA Interface Blocks for PCI Express support up to x8 Gen 2.
6. Does not include configuration Bank 0.
7. This number does not include GTX transceivers.

Xilinx FPGAs Cont'd

Table 6: **Virtex-7 FPGA Feature Summary**

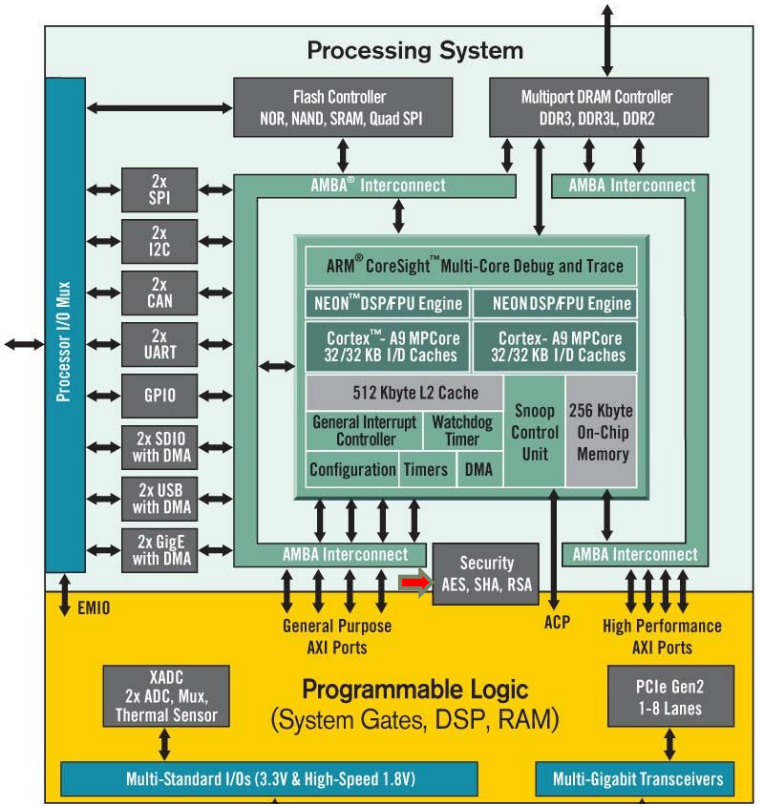
Device[1]	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices[3]	Block RAM Blocks[4]			CMTs[5]	PCIe[6]	GTX	GTH	GTZ	XADC Blocks	Total I/O Banks[7]	Max User I/O[8]	SLRs[9]
		Slices[2]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)									
XC7V585T	582,720	91,050	6,938	1,260	1,590	795	28,620	18	3	36	0	0	1	17	850	N/A
XC7V2000T	1,954,560	305,400	21,550	2,160	2,584	1,292	46,512	24	4	36	0	0	1	24	1,200	4
XC7VX330T	326,400	51,000	4,388	1,120	1,500	750	27,000	14	2	0	28	0	1	14	700	N/A
XC7VX415T	412,160	64,400	6,525	2,160	1,760	880	31,680	12	2	0	48	0	1	12	600	N/A
XC7VX485T	485,760	75,900	8,175	2,800	2,060	1,030	37,080	14	4	56	0	0	1	14	700	N/A
XC7VX550T	554,240	86,600	8,725	2,880	2,360	1,180	42,480	20	2	0	80	0	1	16	600	N/A
XC7VX690T	693,120	108,300	10,888	3,600	2,940	1,470	52,920	20	3	0	80	0	1	20	1,000	N/A
XC7VX980T	979,200	153,000	13,838	3,600	3,000	1,500	54,000	18	3	0	72	0	1	18	900	N/A
XC7VX1140T	1,139,200	178,000	17,700	3,360	3,760	1,880	67,680	24	4	0	96	0	1	22	1,100	4
XC7VH580T	580,480	90,700	8,850	1,680	1,880	940	33,840	12	2	0	48	8	1	12	600	2
XC7VH870T	876,160	136,900	13,275	2,520	2,820	1,410	50,760	18	3	0	72	16	1	6	300	3

Notes:

1. EasyPath™-7 FPGAs are also available to provide a fast, simple, and risk-free solution for cost reducing Virtex-7 T and Virtex-7 XT FPGA designs
2. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
3. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
4. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
5. Each CMT contains one MMCM and one PLL.
6. Virtex-7 T FPGA Interface Blocks for PCI Express support up to x8 Gen 2. Virtex-7 XT and Virtex-7 HT Interface Blocks for PCI Express support up to x8 Gen 3, with the exception of the XC7VX485T device, which supports x8 Gen 2.
7. Does not include configuration Bank 0.
8. This number does not include GTX, GTH, or GTZ transceivers.
9. Super logic regions (SLRs) are the constituent parts of FPGAs that use SSI technology. Virtex-7 HT devices use SSI technology to connect SLRs with 28.05 Gb/s transceivers.

Xilinx FPGAs Cont'd

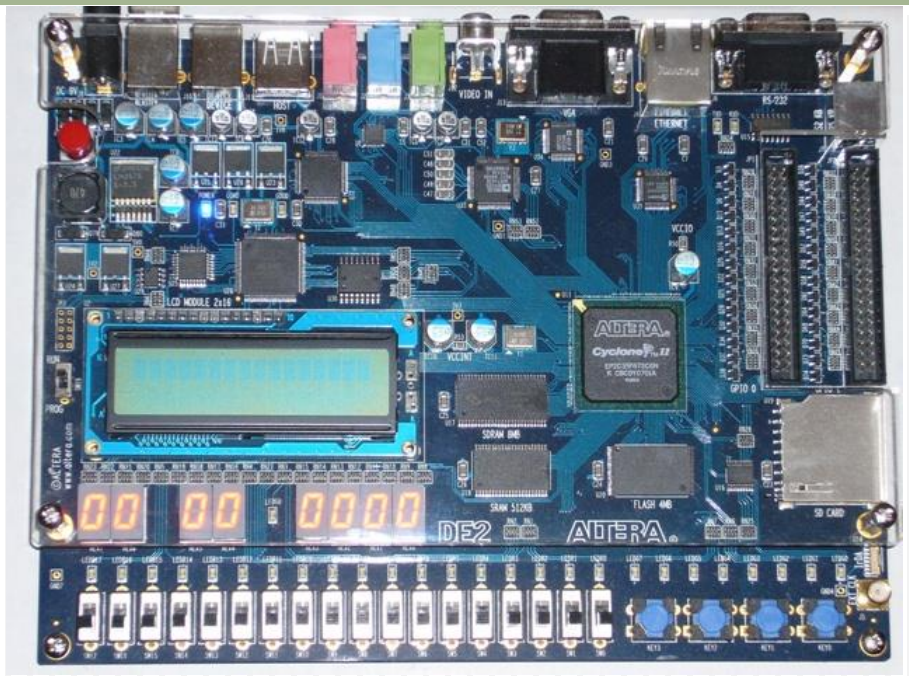
- PSoC: Xilinx Zynq-7000



	Low-End Portfolio			Mid-Range Devices			
Device Name	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
Part Number	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™						
Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor						
Maximum Frequency	866MHz			Up to 1GHz[1]			
L1 Cache	32KB Instruction, 32KB Data per processor						
L2 Cache	512KB						
On-Chip Memory	256KB						
External Memory Support[2]	DDR3, DDR3L, DDR2, LPDDR2						
External Static Memory Support[2]	2x Quad-SPI, NAND, NOR						
DMA Channels	8 (4 dedicated to Programmable Logic)						
Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO						
Peripherals w/ built-in DMA[2]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO						
Security[3]	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot						

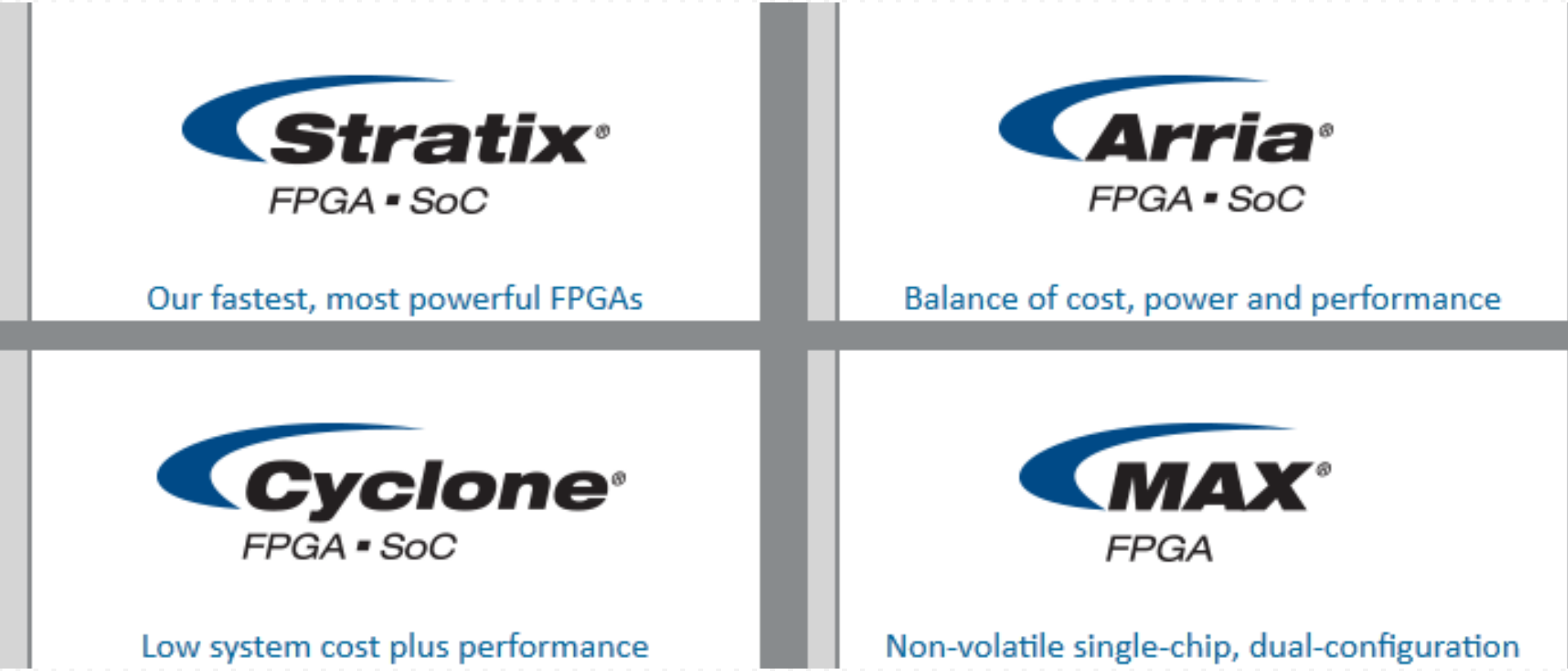
Altera FPGAs

- Low-cost FPGAs
  - Cyclone family
- Mid-range FPGAs
  - Arria family
- High-end FPGAs
  - Stratix family (>4M logic elements claimed)
- You may have seen one of them in DSD LAB!!



Altera de2

Altera FPGAs Cont'd



Stratix Series FPGAs

- High density
- High performance
- Rich feature set
- Stratix series FPGAs allow you to integrate
  - more functions and
  - maximize system bandwidth.

Device Family	Stratix	Stratix GX	Stratix II	Stratix II GX	Stratix III	Stratix IV	Stratix V	Stratix 10
Year of introduction	2002	2003	2004	2005	2006	2008	2010	2013
Process technology	130 nm	130 nm	90 nm	90 nm	65 nm	40 nm	28 nm	14 nm Tri-Gate

Cyclone Series FPGAs

- The Cyclone® FPGA series is built to meet
  - low-power
  - cost-sensitive design needs
  - faster time to market

	Cyclone FPGA	Cyclone II FPGA	Cyclone III FPGA	Cyclone IV FPGA	Cyclone V FPGA
Year introduced	2002	2004	2007	2009	2011
Process technology	130 nm	90 nm	65 nm	60 nm	28 nm
Recommended for new designs	No	Yes	Yes	Yes	Yes

Arria Series FPGAs

- Altera's Arria® family delivers
  - optimal performance
  - power efficiency
  - midrange
  - The SoC variants in the Arria V and Arria 10
    - An ARM®-based hard processor system (HPS)
    - for even higher integration and power savings.

Family	Arria GX	Arria II GX	Arria II GZ	Arria V GX, GT, SX	Arria V GZ	Arria 10 GX, GT, SX
Year of introduction	2007	2009	2010	2011	2012	2013
Process technology	90 nm	40 nm	40 nm	28 nm	28 nm	20 nm

Any Question ?