Hardware Implementations of Evolvable Systems
A critical analysis on self-adaptive autonomic systems on reconfigurable architectures

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November 3, 2013

Abstract

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Keywords: bio-inspired , self-aware , computing systems, machine learning

Blabla

1 Introduction

Introduction [5] blabla [**?**]

2 Prior knowledge

[still need to give an introduction to all the matters spoken. what is evolvable hardware?] [firstly introduce the self* properties as they are mentioned right into the discussion]

Self-aware adaptive computing systems are capable of adapting their behavior and resources thousands of times based on changing environmental conditions and demands [6]. This allows them to automatically accomplish their goals in the best way possible.

Evolvable systems exploiting self-adaptive techniques are self-configuring and self-optimizing systems capable of changing their operations to meet the given performance goals by modifying either the underlying heterogeneous architecture, the operating system and the self-adaptive applications. [4] Meeting efficiency and accuracy constraints is getting more and more difficult , mainly because of the exponential increase of interactions among systems and the environments in which the systems are required to work.

Heartbeat makes it possible to assert performance goals as heart-rate windows each of each is delimited by a minimum and maximum heart-rate. It updates the progress of the execution calling the function that signifies a

heartbeat. It monitors the progress of the execution through either a windows heart rate and a global heart-rate.[4]

The monitoring process is central to self-adaptive systems and is done by the application HeartBeats. Using machine learning, one can enhance synchronization techniques. K32 is a modern object-oriented operating system that responds to changing and challenging environments adapting its operations. It supports on line reconfiguration of functionalities by interposition, hot-swap and dynamic update. [4]

3 Discussion of the Different Papers

[introduction to discussions and seperation of the topics, maybe seperate hardware from software solution from these papers?] [Give some small introduction to each paper in 3 sentences and then maximum of 15 for every paper]

Considerable research has already been done in order to efficiently accelerate hardware while still maintaining virtually unlimited adaptability. Software techniques in autonomic computing systems such as hot-swapping and data clustering are discussed in [1]. These self-aware systems can adapt their behavior on FPGA-based system as discussed in [6]. Other approaches start with a FPGA-based architecture with a reconfigurable core [2], added programming schemes and new cell structures [3], [7] or even bio-inspired hardware using the POE-model [8]. More recent papers put effort a combined approach by either implementing autonomic systems on reconfigurable architectures [9] or creating evolvable systems via self-aware applications [4].

3.1 Software based flexible approaches

The results of [6] presents a system built on top of a set of enabling technology that proves the effectiveness of using self-aware adaptive computing systems. Self-aware adaptive computing focuses on creating a balance of resources to improve performance, utilization, reliability and programmability. A programmer will ideally only have to provide the system its goal, rather than a description of tasks, provided with some constraints.

In a system like this, the hardware, the application and the operating system have to be seen as unique entities to autonomously adapt itself. The underlying architecture has cognitive hardware mechanisms in its core to observe and affect the execution. The self-aware adaptive computing system also implements learning and decision making engines to determine appropriate actions. A key challenge is to identify what parts of a computer need to be adapted.

3.2 Hardware based fast approaches

Inspired by life on Earth and the natural processes of living organisms, *bio-inspired* hardware systems have evolved. [8] introduces the POE model, that classifies bio-inspired systems according to three axes:

- Phylogeny, where evolvable hardware can be found.
- Ontogeny, where systems have the ability to self-repair as the main goal of ontogeny is (cell) growth or construction.
- Epigenesis, which is more software-based.

By looking at these biological phenomena, researchers can be inspired when developing evolvable hardware systems.

[detailed technical discussion follow later]

The Erlangen Slot Machine from [7] tackles the three major limitations of the Virtex-II

FPGA produced by Xilinx. A pipelined data flow architecture has been used, replacing the finite state machine by a MicroBlaze microcontroller and employing a data crossbar between plug-ins. Providing a new architecture to avoid the current physical problems of reconfigurable FPGAs, a new inter-module communication concept, as well as an intelligent module reconfiguration management has made the ESM an alternative for the Xilinx FPGAs.

In [3] a Virtex4 FPGA implementation is introduced for evolvable systems. Other then earlier versions of Virtex (e.g. the Virtex-II Pro), Virtex4 devices enable two-dimensional dynamic reconfiguration, a feature which considerably reduces the reconfiguration time an thus the evoltuion time ([3]). By using both VRCs (Virtual Reconfigurable Circuits) and direct bitstream manipulation, this new architecture eliminates the biggest limitation of Virtex FPGAs, which is an almost unknown and undocumented bitstream data format and an unsafe configuration schema.

This Virtex4-based device, which takes advantage of 2D reconfiguration capabilities and direct manipulation of the bitstreams is the first one of its kind and will be discussed later.

Another FPGA-based architecture is proposed in [**?**]. A highly regular and modular architecture is being integrated with a widely known 2D systolic processing architecture with an optimized DPR control engine. In the design, the processing elements (PEs) of the reconfigurable core are structured as a 2D systolic array, known for its high performance and restrained use of resources (for collection of processed data only the lowest and rightmost PE has to be considered).

Also, the reconfiguration engine has been enhanced by applying three changes that will be discussed in **??**.

3.3 Co-design based systems

In [9] the importance of hardware/software co-design during design space exploration is urged on. Right now this co-design emphasizes on identifying intensive kernel tasks and implementing these tasks on the reconfigurable hardware. Existing adaptive systems often fail because of they are largely ad hoc and fail to incorporate true goals. The current performance model of the hardware however, depends on the degree of parallelism while the performance model for software execution is static and does not become affected by external factors. Since the introduction of reconfigurable hardware platforms such as FPGAs, the hardware domain shifted into the software domain: the possibility of implementing a reconfigurable architecture increased the flexibility of the hardware.

Partial dynamic reconfiguration is a key feature that makes FPGAs unique. This addresses the lack of resources to implement an application and its adaptability needs. Reconfigurable hardware taking advantage of partial dynamic reconfiguration is the perfect trade-off between the speed of HW and the flexibility of SW. Other aspects that motivate the use of online self-adaptable systems are the QoS and the reliability and continuity of the service.

However, an important problem often neglected is the time overhead the reconfiguration process introduces and the two-dimensional partitioning strategy reconfigurable devices need: spatial and temporal. [9] presents the urge to carefully evaluate the overhead created as a negative impact of reconfiguration latency which is not always discussed in present papers. In [4] an evolvable system running self-adaptive application on top of a heterogeneous systems is proposed. The operating system running on top is responsible for providing the self-* proporties and runs this on a general purpose processor and a reconfigurable device

In [4], the underlying hardware architecture is made up of static area and a dynamic area. The reconfigurable device can be configured to implement different functionality through dynamic reconfiguration support provided by the operating system. This is provided through standard libraries and the OS implements parts of the loop. The OS is therefor capable of choosing at run-time the best implementation for the required functionality among the available. The switchable units in the hot-swap method in [4] are identified as the libraries that export an implementation of a certain functionality. The self-adaptive library or Dynamic-link library(DLL) and the software implementation library target the reconfigurable FPGA and multicore respectively.

4 Analysis of techniques

This section provides an overview of techniques that are used in current research to create evolvable hardware implementations of evolvable systems. To create such a system, the system has to be self-aware, able to make decisions, self-adapting and the hardware has to support a certain amount of reconfiguration. In section 5 the overall best combination will be presented, utlizing the flexibility of software and the speed of hardware.

4.1 Self-awareness techniques

* present heart beats and monitoring and passing arguments *

4.2 Decision making techniques

* present heuristics, best algorithm etc *

4.3 Self-adapting techniques

* optimization techniques *

4.3.1 Virtex-4 based FPGA

On Virtex-4 FPGAs, two-dimensional dynamic reconfiguration is supported. This 2D architecture of the reconfiguration core (or RC) speeds up the reconfiguration time and deploys more candidate solutions (arrays of bidimensional cells, see figure). Candidate solutions are chosen because of their internal flip-flops, which use direct bitstream manipulation. Also a new cell structure for the candidate solutions using LUTs and a MUX is introduced, in order to provide direct bitstream manipulation. This deals with the unsafe configuration schema of Virtex FPGAs. Combined with the 2D-reconfiguration mechanism, the new architecture causes a speed up of 16x factor. For this system, only Virtex-4 or Virtex-5 FPGAs can be used since Virtex-II does not support 2D reconfiguation ([3].

A drawback of using Virtex FPGAs are the feed-through signales. Each module must be implemented with all possible feed-through channels needed by other modules. Because we only know at run-time which module needs to feed through a signal, many channels reserved for a possible feed-through become redundant. Also, modules accessing external pins are no longer relocatable, because they are complied for fixed locations where a direct signal line to these pins is established ([7]).

4.3.2 2D systolic approach for RC and optimized DPR RE

The second architecture used for the reconfiguration core (RC) of the Virtex-4 FPGA is an array of processing elemens (PEs), also following a 2D approach. A major feature is the possibility to change the functionality of the PEs by means of Dynamic and Partial Reconfiguration (DPR). This gives the system the capability adapt. The outputs of the PEs (east and south side) are connected to the close neighbour's input (west and north side), such that only the

lowest and right-most PE has to be read for data output. This systolic approach of communication reduces the reconfiguration time and makes the architecture easy to extend.

By storing only the body of the bitstream (cutting of the header and the tail), overclocking the FPGA by 2,5x and including internal memory (to avoid pasting the same configuration module in different positions of the architecture) the DPR is optimized. Due to this the reconfiguration time is greatly reduced. By adding the header and the tail of the bitstream at runtime, it is allowed having a unique bitstream for each PE that can be configured in any position of the array. Also, bitstream reduction reduces the data transference time from the external memory ([2]).

4.3.3 Erlangen Slot Machine

The architecture of [7] the Erlangen Slot Machine deals with three drawbacks of FPGAs, being fixed pins which are spread around the device (I/O dilemma0, the inter-module dilemma and the local memory dilemma. First, the I/O dilemma caused by fixed pins spread around the device is solved by connecting all bottom pins from the FPGA to an interface controller realizing a crossbar. It connects FPGA pins to peripherals automatically based on the slot position of a placed module. This I/O rerouting principle is done without reconfiguration of the crossbar FPGA.

Second, the memory dilemma has been solved. In normal Virtex-II FPGAs, a module can only occupy the memory inside its physical slot boundary. Storing data in off-chip memories is therefore the only solution. In the ESM, six SRAM banks are connected to the FPGA. Since these banks are placed at the opposite side as the crossbar, a module will connect to peripherals from one side, while the other side will be used for temporally storing computational data. In order to use a SRAM bank (called a slot), the module must have at least a width of three micro-slots, in which the total device is divided. This organization simplifies relocation, enabling a partially reconfigurable computing system. Also, equal resources will be available for each module.

Finally, the inter-module communication dilemma is dealt with. Dynamically routing signal lines on the hardware is a very difficult task. The ESM uses a combination of bus-macros, shared memory, RMB (Reconfigurable Multiple Bus) and a crossbar to take away the limiting factor for the wide use of partial dynamic reconfiguration ([7]).

5 Proposed adaptive system design

* set up of a proposed system *

6 Related works

a presentation of related combination of techniques presented in previous paper

7 Conclusion

Comparison

References

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