A 380 fW Leakage Data Retention Flip-Flop for Short Sleep Periods

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***Abstract*—Data-retention flip-flops (DR-FF) provide an efficient state retention capability for any processor with frequent active-to-sleep mode transitions. This brief proposes new ultra-low-power balloon-based DR-FFs operating over a wide supply voltage range achieving a sleep mode power consumption as low as 380 fW, an improvement of 185× over the previously reported CMOS DR-FFs. The proposed DR-FFs have significantly lower transition mode energy consumption compared to prior-art non-volatile DR-FFs (>18×). The proposed DR-FFs consume the lowest total energy (sleep, store and restore modes) for sleep mode times less than 520 ms. Additionally, the designed DR-FFs are comparable with most of the NV-FFs in literature for sleep times of up to 100 s, while eliminating the drawbacks of Non-volatile data retention FFs (higher/multiple supplies, integration/endurance issues).**

***Index Terms*—Flip-flop, dynamic leakage suppression, data/state retention, ultra-low power.**

I. Introduction

IOT DEVICES operating using a small battery and/or an energy harvesting source often require an ultra-low-power sleep mode with data/state retention capability to achieve 1) a long operational lifetime and 2) consistent task execution.

Traditionally, power gating a processor along with a data retention capability is the most efficient way to minimize sleep power [1], [2], [3]. In this technique, critical data is maintained in an ultra-low power circuitry during sleep mode to guarantee continuous operation when the system is reactivated.

In the prior art there are two approaches to achieve a low leakage flip-flop (FF) with data retention capability 1) non-volatile data retention FF (NV-FF) [1], [2], [3], [4], [5], [6], [7], [8], [9], [10] and 2) CMOS FF with a balloon latch (DR-FF). The NV-FF allows zero power consumption to maintain the data during the sleep mode, whereas the DR-FF requires an always-on circuity to preserve the data [11], [12], [13], [14], [15], [16]. Nevertheless, NV-FFs have several disadvantages over CMOS DR-FFs, particularly for duty-cycled systems with short and frequent sleep modes. These are: 1) NV-FFs require higher state-transition energy than DR-FFs (Fig. 1). 2) NV-FFs have limited endurance. For example, RRAM and MTJ NV-FFs have a maximum write endurance of 10^9 and 10^{12} cycles, respectively [8]. 3) NV-FFs require a high transition mode supply voltage as well (>1 V), which makes them difficult to integrate in systems [17]. 4) Additionally, NV-FFs generally come with relatively higher active mode power, delay and area overheads. 5) Finally, NV-FFs require special technology support and additional manufacturing costs.

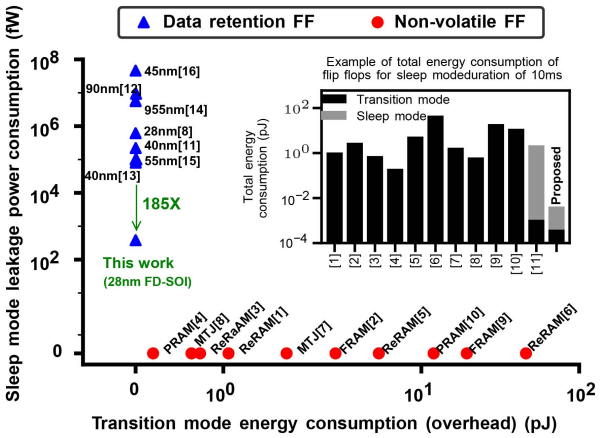

Fig. 1. Sleep mode leakage power consumption vs state-transition energy consumption for DR-FFs and NV-FFs.

CMOS DR-FFs prevent the aforementioned disadvantages associated with NV-FFs. However, even prior-art CMOS DR-FFs have a relatively high sleep mode power consumption, typically in the order of hundreds of pico-watt, leading to a considerable leakage power consumption for a design consisting of numerous flip-flops. This brief presents an ultra-low-leakage balloon-based DR-FF leveraging dynamic leakage suppression (DLS) and dual-mode (DM) logic techniques introduced in [18] and [19], respectively. The main contributions of this brief are as follows:

- Use of hybrid cell (DLS and DM) to enable the efficient design of the balloon in the DR-FF, which operates over a wide voltage range (down to sub-threshold 0.4 V-0.9 V). The achieved leakage power consumption is 380 fW, 185× lower than the previously reported DR-FFs.
- Extensive design analysis of three different possible combinations of inverters for the design of the balloon (DLS-DLS, DLS-DM and DM-DM) over process, voltage and temperature ranges.
- Dynamic control of the transistors in the DM inverter to switch between high-performance store/restore mode and low leakage sleep mode.

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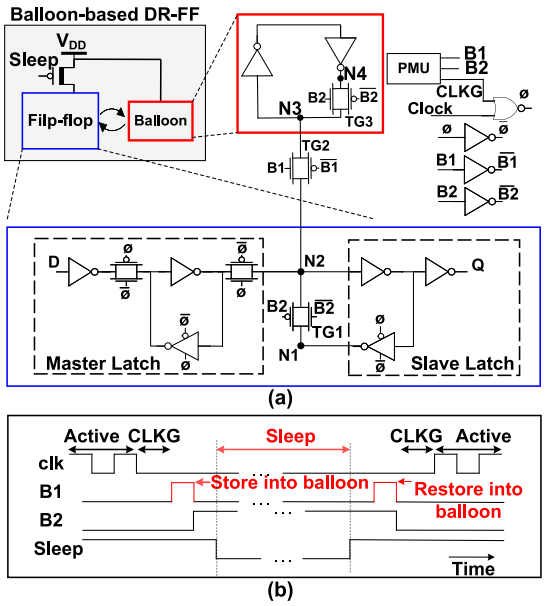

Fig. 2. A typical balloon DR-FF. (a) Circuit diagram. (b) Operation waveform of the control signals.

Our solution is an attractive alternative to NV-FFs that enables IoT devices with ultra-low-leakage power and ultra-low state-transition energy consumption avoiding the aforementioned disadvantages of NV-FFs.

II. Background

In prior work, various DR-FFs have been proposed to reduce the sleep mode leakage power consumption. In [11], a DR-FF is proposed which can be configured as a Schmitt-trigger inverter and as a regular inverter during sleep and active mode, respectively. This design enables data retention down to 0.2 V with 220 pW sleep mode power consumption. In [12], a balloon-based DR-FF was introduced with 11% area overhead and 5.5 nW sleep mode power consumption. A DR-FF with ~70 pW was proposed in [13] to enable data retention without any additional circuitry. The DR-FFs in [11] and [13] come at the cost of considerable active mode power and delay overhead due to the use of high-V_{th} transistors in the critical path of the flip-flop. Among the prior art, balloon-based DR-FFs have the least impact on the degradation of the active mode specifications as the critical path remains untouched. In this section, the preliminaries of a balloon-based DR-FF are discussed.

A. Balloon-Based Data Retention Flip-Flop Structure

A typical balloon DR-FF scheme is shown in Fig. 2(a). It consists of an always-powered latch (balloon) connected through a transmission-gate (TG2) to the slave stage of a flip-flop. Transmission-gates TG1 and TG3 enable store/restore operation to/from the balloon. The TGs in the balloon DR-FF are turned on/off by signals B1 and B2. A power management unit (PMU) generates B1 and B2 signals according to the transition between store-sleep-restore modes. Usually, high-V_{th} transistors are used for the inverters in the balloon to minimize the leakage power consumption during sleep mode.

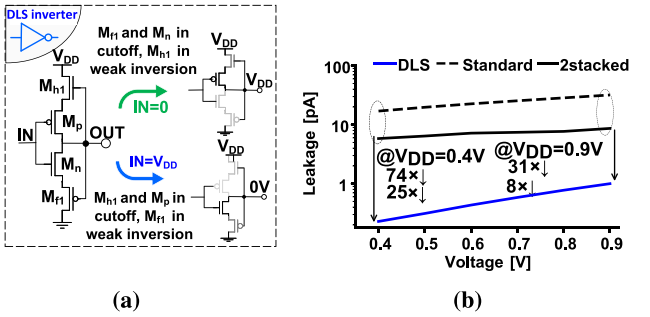

Fig. 3. (a) DLS inverter structure and operation. (b) Leakage comparison with standard and 2-stacked inverters in 28-nm FD-SOI *(for comparison all transistors are minimum sized (W/L = 80nm/30nm))*.

B. Balloon-Based Data Retention Flip-Flop Operation

The balloon DR-FF operation and the control signals during different modes (active, gated clock (CLKG), store, sleep, and restore) are shown in Fig. 2(b) During the store mode (B1=V_{DD}, B2=0), TG2 is turned-on. Hence, the data at node N2 is stored into the balloon. The store mode delay is the time required for the data at node N4 to reach a stable voltage. The data is recovered during the restore mode. In restore mode (B1=V_{DD}, B2=V_{DD}), TG2 is turned on so that the data is transmitted from N3 to node N2 in the FF. The restore mode delay is the time required for the data at the output of the flip-flop to stabilize. Once the data is stored or restored, the balloon is detached (sleep-mode (B1=0, B2=V_{DD})) from the FF by turning off the TG2. The switches TG1 and TG3 in the FF prevent nodes N2 and N3 to be overwritten, respectively. In this brief, we propose new balloon-based DR-FFs, which have a significantly lower sleep mode power consumption as compared to the DR-FFs using standard inverters.

III. Proposed Data Retention Flip-Flops

The proposed balloon DR-FFs leverage two types of inverters based on the dynamic leakage suppression (DLS) and dual-mode (DM) design techniques. In this section, these two inverters are first introduced and then the structure and operation of the proposed DR-FFs are presented.

A. DLS and DM Inverter Operation

A DLS inverter (Fig. 3(b)) consists of a standard inverter whose output node is connected to a header NMOS transistor and a footer PMOS transistor. These additional transistors act as power-gating transistors to the standard inverter through which the leakage current consumption is reduced significantly [20]. The leakage current consumption of the designed regular-V_{th} based DLS, standard, and 2-stacked inverters in 28nm FD-SOI are shown in Fig. 3. According to the simulation results, the DLS inverter is 74× and 25× less leaky at 0.4 V, and 31× and 8× less leaky at 0.9 V as compared to the standard and 2-stacked inverter, respectively. Conversely, the DLS inverter acts considerably slower than the standard inverter. Thus, it is inefficient in the active mode (store/restore mode). Therefore, dual-mode logic was introduced in [19] to address the active mode delay issue of DLS design.

A dual-mode (DM) inverter structure and its operation are shown in Fig. 4(a). A DM inverter includes two extra transistors in parallel with the header and footer of the DLS

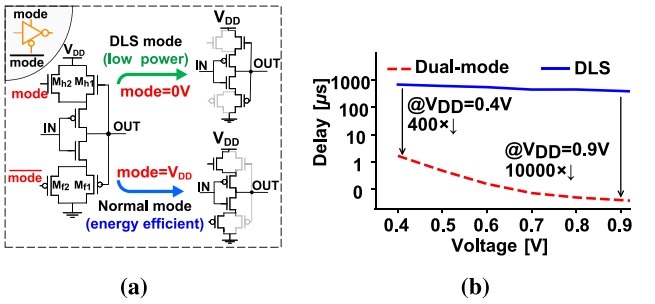

Fig. 4. (a) Dual-mode inverter structure and operation. (b) Delay comparison with DLS inverter in 28-nm FD-SOI *(for comparison all transistors are minimum sized (W/L=80nm/30nm))*.

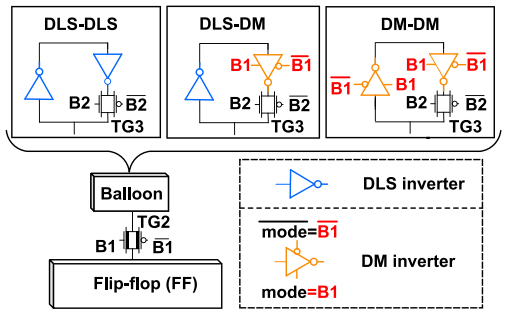

Fig. 5. 3-alternative designs of the balloon in the DR-FF.

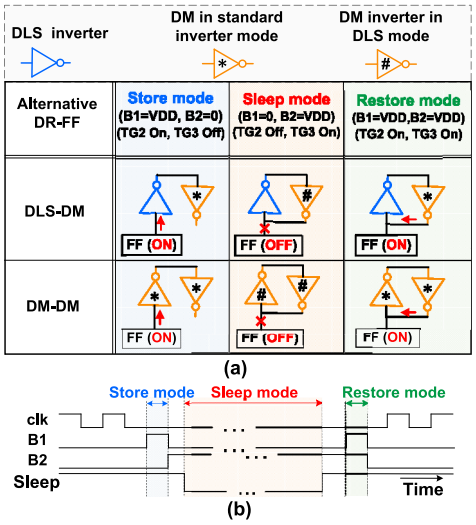

Fig. 6. An overview of DLS-DM and DM-DM DR-FFs operations. (a) Overview of the possible modes of operations. (b) Timing diagram.

inverter. These additional transistors are driven by an input signal (mode) according to which the inverter operates as either a DLS inverter or a standard inverter. This flexibility of the DM inverter allows switching between low-power idle mode and fast operation mode. Fig. 4(b) shows the simulated delays of the DM and DLS inverters for a voltage range of 0.4 V to 0.9 V. As shown in Fig. 4(b), the DM inverter is 400× and 10k× faster at 0.4 V and 0.9 V, respectively, than the DLS inverter.

B. Design of the Proposed DR-FFs

The three proposed balloon DR-FFs are shown in Fig. 5. The balloons comprise different combinations of DLS and DM inverters. These balloons are designed based on 1) two DLS inverters connected in series (DLS-DLS), 2) a DLS inverter connected to a DM inverter (DLS-DM), and 3) two DM inverters connected in series (DM-DM). In the DLS-DM balloon, the DM inverter is used as the driver of node N2 (Fig. 2) to improve the restore operation as it has to drive the higher capacitive load. The transmission-gates operation for store-sleep-restore mode transition are the same as in Fig. 2. Furthermore, the mode control signal for the DM inverter to switch between standard and DLS operation is dynamically controlled using the B1 signal, eliminating the requirement for an additional control signal. In this way, the DM inverters in DM-DM and DLS-DM balloons are dynamically configured according to the operation modes.

Fig. 6(a) shows in a simplified way how the proposed DR-FFs from Fig. 5 are configured in each mode of operation. As shown in Fig. 6(b), during sleep mode (B1=0, B2=V_{DD}), all inverters in the balloon are structured as DLS inverters to enable low leakage power consumption. During store (B1=V_{DD}, B2=0) and restore modes (B1=V_{DD}, B2=V_{DD}), the DM inverters in the DLS-DM and DM-DM balloons are configured as a standard inverter to perform faster data transition as shown in Fig. 6(a). The inverters in the proposed balloons are sized and optimized for two aspects: Pull-up and pull-down parts are sized to achieve balanced rise and fall delays. Then, the transistors are resized to verify the store and restore operations for data (0/V_{DD}) at all the process corners (TT, SS, FF, SNFP, and FNSP), temperature ranges from 0°C to 80°C, and over a supply voltage range from 0.4 V to 0.9 V. The sizing of the transistors in the DLS-DLS balloon is challenging. During the restore operation, the DLS inverter has to charge/discharge node N2. Since the DLS inverter has a low drive/pull strength and node N2 is connected to multiple switches, the leakage of the switches creates a problem. Therefore, the DLS inverter driving N2 must be sized relatively big (4×) compared to the other DLS inverters to enable operation at all the aforementioned operating conditions.

IV. Results and Evaluation

In this section, the sleep mode power consumption and transition modes (store/restore) energy consumption are evaluated. In order to provide a reference comparison for leakage power consumption and store/restore delay, the smallest size latches from the commercial 28-nm FDSOI libraries (PB0 and PB16) are chosen for comparison against the designed balloons. Note that the FF for all the DR-FFs is the same to make the comparison fair. To verify the functionality, all the DR-FFs are simulated for a supply voltage range from 0.4 V to 0.9 V, process variation corners (TT, SS, FF, SNFP, and FNSP), and for a temperature range of 0°C to 80°C.

A. Sleep Mode Comparison

1) Sleep Mode Leakage: Fig. 7 illustrates the average leakage power consumption for data (0/ V_{DD}) of the proposed DR-FFs and the latch from the library for a voltage range from 0.4 V to 0.9 V. The results show that the proposed DR-FFs have considerably lower sleep mode power consumption compared to the least leaky latch from the library by up to 13×

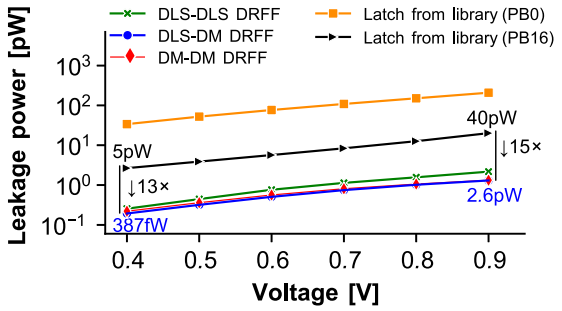

Fig. 7. Leakage power consumption of the DR-FFs at different supply voltages at typical corner 25°C.

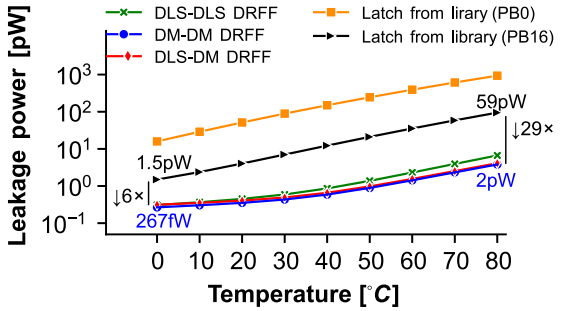

Fig. 8. Impact of temperature variation on the leakage power consumption of the DR-FFs at the typical corner, 0.4 V.

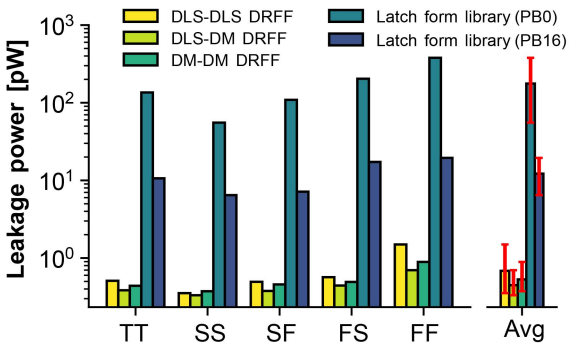

Fig. 9. Impact of process corner variation on the leakage power consumption of the DR-FFs at 25°C, 0.4 V.

and 15× at 0.4 V and 0.9 V, respectively. Among the proposed DR-FFs, the DLS-DM DR-FF has the lowest leakage power consumption of 380 fW at 0.4 V and 2.6 pW at 0.9 V. This is because it has fewer transistors than the DM-DM DR-FF and smaller transistors (4×) than the DLS-DLS DR-FF. Note that the DLS-DLS transistors are sized relatively bigger to enable operation at all PVT conditions.

2) Temperature Variations Impact: To investigate the impact of temperature variations, the DR-FFs and the latch from the library are simulated over a temperature range of 0°C to 80°C at 0.4 V and the typical corner. The leakage power consumption savings is greater than 6× above 0°C compared to the latch (BP16) from the library.

3) Process Variations Impact: Fig. 9 shows the leakage power consumption of the DR-FFs and the latch from the library for process variations. The results show that the proposed DR-FFs have considerably less leakage power consumption and less sensitivity to process variations than the

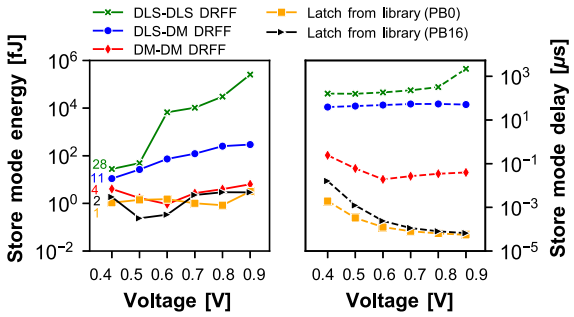

Fig. 10. Store mode energy consumption and delay of DR-FFs.

TABLE I
ACTIVE-MODE SPECIFICATION OF THE DR-FFS OPERATING AT 0.4 V, TT, 25°C, AND 1MHZ CLOCK FREQUENCY

	Power (nW)	Delay (CLK-to-Q) (ns)	Setup / Hold time (ns)	Area (μm^2)
FF only	0.814	19.8	7.26 / -7.23	3.7
DR-FFs based on: (Latch, DLS-DLS, DLS-DM, DM-DM)	0.833*	22.75*	8.55*/ -7.24*	4.9, 7.1, 5.9, 6.3

* Performance identical since balloon has negligible impact on active mode.

latch from the library. The DLS-DM DR-FF has the least leakage power consumption in all corners.

B. Store and Restore Comparison

It is essential to consider the store/restore-mode energy overhead, as the mode transition energy consumption must not degrade the energy saved during the sleep mode. To evaluate this, the worst-case mode-transition delays for data ($0/V_{DD}$) and the corresponding energy consumption are considered.

1) Store Operation: Fig. 10 shows the energy consumption of DR-FFs during store mode. The DM-DM DR-FF is superior to the other proposed DR-FFs and comparable with the latches from the library connected to the same flip-flop as in the proposed DR-FFs. The DM-DM DR-FF is 85% and 63% more energy efficient than the DLS-DLS and DLS-DM DR-FFs, respectively, at 0.4 V. The total energy consumption of the DM-DM remains below 10 fJ over the voltage range of 0.4 V to 0.9 V. The store mode energy consumption of DLS-DLS and DLS-DM DR-FFs increases as the DLS inverter delay is relatively constant with supply voltage change. While the DM-DM DR-FF and the latches from the library (PB0 and PP16) are structured as standard inverters during store mode and they have a minimum energy at 0.6 V, 0.8 V and 0.5 V, respectively.

2) Restore Operation: As shown in Fig. 11, the restore mode energy consumption of the DR-FFs is relatively similar. In this mode, the balloons are static and they are not toggling. Thus, the energy consumption is dominated by the flip-flop. Nevertheless, DM-DM and DLS-DM are slightly more energy-efficient, as they have lower balloon leakage compared to the other designs.

C. Active-Mode Overhead

In Table I, the DR-FFs active-mode power consumption with 1 MHz clock frequency, delay (CLK-to-Q), set-up time

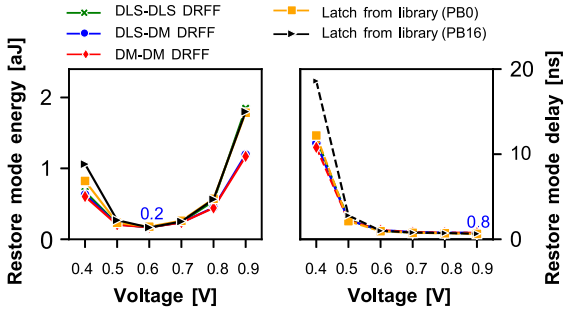

Fig. 11. Restore mode energy consumption and delay of DR-FFs.

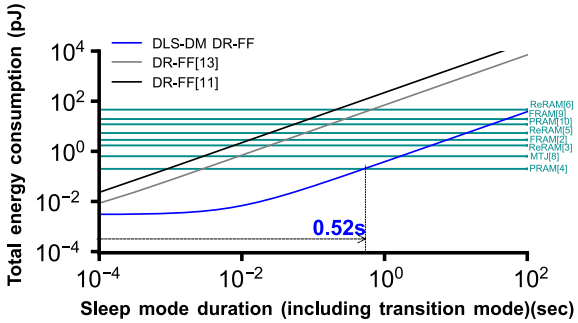

Fig. 12. DR-FFs vs. NV-FFs with sleep mode duration.

TABLE II
COMPARISON OF THE PROPOSED DLS-DM FF WITH PRIOR ART

	This work (DLS-DM)	[13] 2020	[12] (2019)	[11] (2018)	[8] (2020)	[6] (2017)
Technology	28nm FDSOI DR-FF	40nm DR-FF	90nm DR-FF	40nm DR-FF	MTJ NV-FF	ReRAM NV-FF
$V_{store/restore}$	(0.4-0.9) V	1.1 V	(0.2-1) V	(0.2-1) V	1 V	1.5 V
Leakage power*	**380 fW**	70 pW	5.5 nW	220 pW	0	0
Store/Restore energy*	11 fJ	1.5 fJ	-	1 fJ	630 fJ	199 fJ
Overhead	2.3% pwr, 14% per, 60% area	- - 2% area	- - 11% area	- 30% per, 50% area	45% pwr, 30% per, 66% area	- - 18% area

* at minimum supply voltage

and hold time and area are compared with the flip-flop without the balloon. The parasitic capacitance of TG2 at node N3 (Fig. 2) adds a small overhead in active mode properties.

V. Comparison With the State-of-the-Art

Table II summarizes the key parameters and compares proposed DLS-DM FF, as it has the lowest sleep power, with the recent prior arts. Unlike NV-based designs, data retention FFs are able to store/restore data at a supply voltage down to the near/sub-threshold. In addition, DR-FFs have less store/restore energy overhead. Additionally, we achieve a state-of-the-art leakage power consumption of 380 fW. Fig. 12 presents a comparison of the total energy consumption during sleep mode including transition and sleep modes energy. The total energy of DR-FFs increases with time due to the constant leakage power during sleep mode. The proposed DR-FFs are more efficient for sleep mode duration below 520 ms. Thus, the proposed DR-FFs are an attractive alternative to the NV-FFs for applications with short sleep durations, furthermore prohibiting NVM DR-FF drawbacks.

VI. Conclusion

This brief proposes the design of ultra-low-power balloon-based DR-FFs using dynamically controlled hybrid DLS and DM cells operating over a wide supply voltage range down to sub-threshold with the lowest leakage power consumption of 380 fW as compared to the previously reported CMOS DR-FFs. Also, the proposed DR-FFs are more energy-efficient than the prior art NV-FFs with short and frequent sleep-mode transitions, avoiding the disadvantages of non-volatile FFs.

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