Low Power Design Techniques and Implementation Strategies Adopted in VLSI Circuits

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***Abstract* - Low power plays a very important role and in today's current trends of VLSI. There are appraisal techniques and extension circuits employed in low power VLSI designs. Power dissipation has main thought as performance and area. Because of higher quality, decreasing power consumption and power management on chip are the key challenges right down to 100nm.Reducing package price and battery life is a very important issue in optimization of power. Leakage current plays a very important role in power management and conjointly low power is a major drawback in high performance digital and micro chip system. Leakage current is a primary issue in total power dissipation of integrated circuits. For victorious chip it solely wants low power consumption, calculation of power dissipation. This paper discusses about future challenges that must be to design and use for low power circuits spans a wide range from device or method level to formula level.**

Keywords:

Power dissipation, low power process, leakage current, power management, and optimization.

I .INTRODUCTION

The advantage of low power design techniques is a lot of valuable than earlier. In this technologies design area, performance, cost and reliability could be a major concern. Power consumption is merely a second issue. Now a days, improvement of aggressive market sectors like wireless applications, laptops and movable medical devices, supported power dissipation as a vital one. The action for decreasing power consumption varies from application to application. In micro powered battery operated moveable applications like cell phones to stay the battery life time and packaging price low. In portable computers as laptops to cut back the power dissipation of the natural philosophy elements of the system is merely two divided of the complete total power dissipation. At last, in high performance systems process technology has been driven power to be first altogether factors of such designs.

II. POWER DISSIPATION

In this power dissipation they have different strategies,

- Dynamic power dissipation.
- Static power dissipation.
- Short-circuit power dissipation.
- Leakage power dissipation.

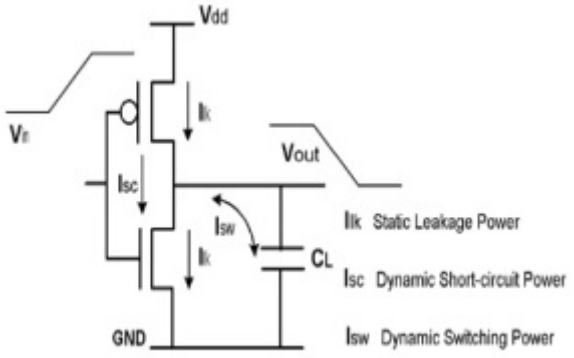

FIG 1. Power dissipation in CMOS.

A.Dynamic power dissipation**:**

They are divided into three divisions: switched, short circuit, glitch power dissipation. This is based on activity, timing output capacitance and supply voltage of the circuit. They occur has result of charging and discharging of the output capacitance is compulsory to convey information in CMOS.

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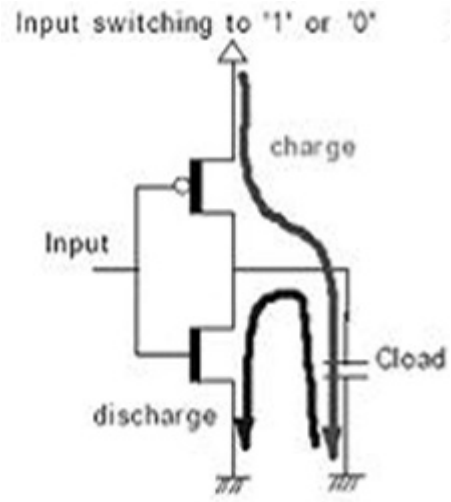

FIG 2.Dynamic Power dissipation.

B.Static power dissipation**:**

Static power is power consumed whereas there's no circuit activity. In static power dissipation they need subthreshold and reverse biased diode discharge currents. The subthreshold discharge is attractive known as a result of its discharge power collage. The transistors isn't obtaining off, only in weak reversal of threshold voltage. The threshold current has lustiness supported threshold voltage.

C.Short-circuited power dissipation**:**

In CMOS logic P-branch and N-branch are momentarily shorted as logic gate changes state resulting in short circuit power dissipation. In this, the current does not cause to charging capacitance of the circuit. This is known as short circuit current consumption. This element is common if the input signal rise and fall time is high or the output load capacitance is low.

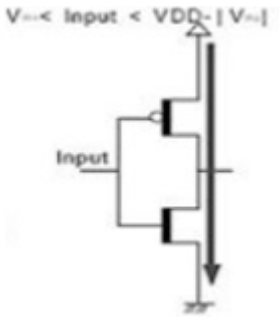

FIG 3.Short Circuit Power dissipation.

D.Leakage power dissipation**:**

This is the ability dissipation that happens once the system is in standby mode. There are several sources of discharge currents are n-well, subthreshold leakages, gate leakages etc. Processing parameters are fastened in VLSI CMOS circuits. Normally CMOS logic gates were used. In case of chip, it consists of varied circuits having continuous current path between power source and ground so it examines with a static component of power. Dynamic power is in switch and discharge current is constant however the subthreshold discharge is a crucial component in over all technologies larger than 130nm.

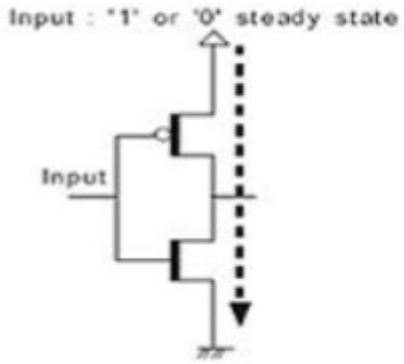

FIG 4.Leakage Power dissipation.

III. OPTIMIZATION TECHNIQUES

The abstraction layers are:

Stem level,algorithm level,architectural level,circuit level,technology level.

System level:

Dynamic power management is a design methodology for dynamically reconfiguring syst9+ems with minimum number of active components or with a minimum load but providing with higher performance level. For achieving this, the system employs power manageable components to be used in the circuit which impacts the overall power consumption. We measure the power by means of power analysis tool only at gate or circuit level.

Algorithm level**:**

Optimization of the circuit for low power is done by behavioral synthesis. The behavioral synthesis involves optimization in the overall algorithm used which depends upon the circuit components used .It denotes only the register transfer level design from high level specification problem. The hardware used actually is reduced by employing better algorithm levels.

Architectural level:

The architectural level involves two techniques. They are pipelining and parallel processing. Pipelining increases the clock speed or reduces power consumption. Parallel processing is also

used for compact area for low power dissipation. It also enhances the speed of the operation of the circuit.

Circuit level**:**
The basic circuit level involves adjusting the size of each transistors or gate for minimum power. This has optimized circuits thereby decreasing the area which too results in lesser area. If the transistors in a given gate or if a transistor size is increased, delay becomes increased. Delay of the fanin gates gets increased due to load capacitance increases. As a result, the overall delay of the circuit increases as the load capacitance increases.

Technology level:
It is a variation of CMOS technology that has transistors with multiple threshold voltages so as to optimize delay or power. The threshold voltage of a MOS is in gate voltage wherever AN inversion layer forms at the interface between the insulating layer and also the substrate of the semiconductor device. Low threshold voltage devices switch quicker, and square measures so helpful on crucial delay methods to attenuate clock periods. Low power devices has considerably higher static leakage power. High threshold voltage devices square measure used on non crucial methods to scale back static leakage power while not acquisition a delay penalty. Typically high threshold devices cut back static leakage by ten times compared with low threshold devices.

Design Level	Strategies
Operating System Level	Portioning, Power down
Software level	Regularity, locality, concurrency
Architecture level	Pipelining, Redundancy, data encoding
Circuit /Logic level	Logic styles, transistor sizing and energy recovery
Technology Level	Threshold reduction, multi threshold devices

FIG 5.Various Levels of Abstraction

IV. OPTIMIZATION CIRCUITS USED IN VLSI

SLEEP TRANSISTORS:

Sleep transistors are high threshold voltage transistors connected in series with low threshold voltage logic has been drawn below. By the normal operation of the circuit, due to the main circuit consisting of low threshold voltage devices ON, the sleep transistor is also ON. Because of high threshold transistors is connected in series with low threshold transistors , the leakage current loss is measured by high threshold voltage devices.

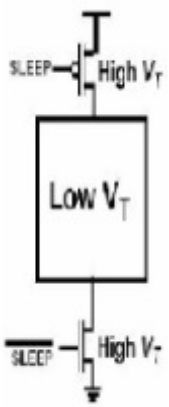

FIG 6.Sleep transistor.

Traditional Techniques	Dynamic power reduction	Leakage power reduction	Other power reduction techniques
--Clock gating	--Clock gating	--Minimize usage of low Vt cells	--Multi oxide devices
--Power gating	--Power efficient circuits	--Power gating	--Minimize capacitance by custom design
--Variable frequency	--Variable frequency	--Back biasing	--Power efficient circuits
--Variable voltage supply	--Variable voltage supply	--Reduce oxide thickness	
--Variable device threshold	--Voltage Islands	--Use FinFET	

FIG 7.Optimization techniques in VLSI.

ADIABATIC CIRCUIT**:**

In adiabatic circuits, as a replacement of dissipating, the power is reused. By obviously regulating the length and shape of signal transistors energy spent to flip a bit can be reduced to very small values. MOSFET should not be turned ON ,If there is heavy potential difference between source and drain and should not be turned off there is a heavy current flowing through the device.

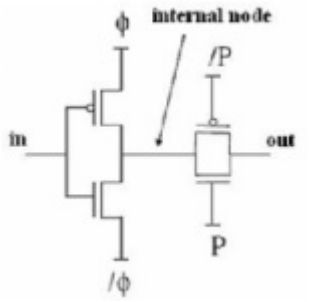

FIG 8 . Charge recover logic.

CONCLUSION

In conclusion, there are different techniques used in low power design as discussed in this paper. Technology Scaling reduces 30% in capacitance mode, 15% in voltage supply. A low voltage design circuits results in less leakage power. Improvement of power reacting techniques and tools for behavioral synthesis, logic synthesis and layout optimization can be adopted. By using low power interconnects, Using newer technologies, decreased swing and activity application can be achieved. Now a days, low power may be a vital role in VLSI. In this paper, We had seen completely different power improvement, dissipation, consumption and conjointly various fields low power applications. With respect to low power VLSI design, area unit measurability in technologies, leakage power, improvement of power etc.

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