Week 6 Task – Physical Design Workshop

Objective

To perform **hands-on Physical Design labs** using a pre-configured VDI image and understand the complete hierarchy of **digital and mixed-signal design implementation** — from standard cell design to DRC and STA validation.

Why This Task Is Important

Having completed OpenROAD installation and basic floorplanning/placement, you are now ready to explore **end-to-end physical design**.
This workshop bridges the gap between theory and real-world chip implementation. It will help you understand:

- How **hierarchical digital design** integrates with **custom analog/mixed-signal blocks**
- The interplay between **layout**, **timing**, and **design rule checks (DRC)**
- How physical design affects the **final sign-off quality** and **silicon reliability**

By the end of this week, you'll appreciate how synthesis, STA, and layout interact to bring a design from RTL to physical silicon.

Lab Setup

You will receive a **document** containing:

- A download link for the **Physical Design Tools VDI image** https://drive.google.com/file/d/1Ri30Yeqjyprv-rStHEScUMpKtw2JfVJe/view
- **Step-by-step installation instructions** for running it on Windows using **Oracle VirtualBox**

Follow that document carefully to set up your local environment before beginning the labs.

Workshop Access

Once the environment is ready:

1. Log in to the **Physical Design Workshop** (access will be enabled for all participants).
2. Watch all the **lab demonstration videos** provided in the workshop interface.
3. Re-create each lab **on your own laptop** using the installed VDI environment.
4. Document your lab work in your **personal GitHub repository**.

Reference for Documentation Format

Follow the documentation style shown here:
📎 Sample Reference Repository – SoC Design and Planning (NASSCOM × VSD)

https://github.com/fayizferosh/soc-design-and-planning-nasscom-vsd/

Your documentation should include:

- Lab objectives and context
- Screenshots of terminal outputs, tool GUIs, and layouts
- Short technical explanations of each step performed
- Reflections or observations connecting each lab to physical design flow concepts (floorplanning, placement, routing, DRC, STA)

Deliverables

- **GitHub Repository Documentation** containing:
    - Screenshots of each completed lab step
    - Summary of key learnings per lab
    - Notes on how digital and analog blocks interact
    - Observations on DRC, LVS, and STA inter-dependencies
- **Proof of Setup:** Screenshot of your running VDI environment showing your **username** in the Linux terminal.

✅ **By the end of Week 6**, you will:

- Successfully set up and operate the **Physical Design lab environment** on your local system.
- Perform and document multiple **hierarchical physical design experiments**.
- Understand the **complete flow from digital synthesis to layout verification and STA sign-off**, linking all previous weeks into one coherent learning path.