
Title: Top Level Sch Abstraction
Size: A4 | **Prj:** Autonomous Control Unit

Date: 22/02/2024 | **16:01:51** | **Sheet 1 of 7**
Git Hash: dd47d3ed

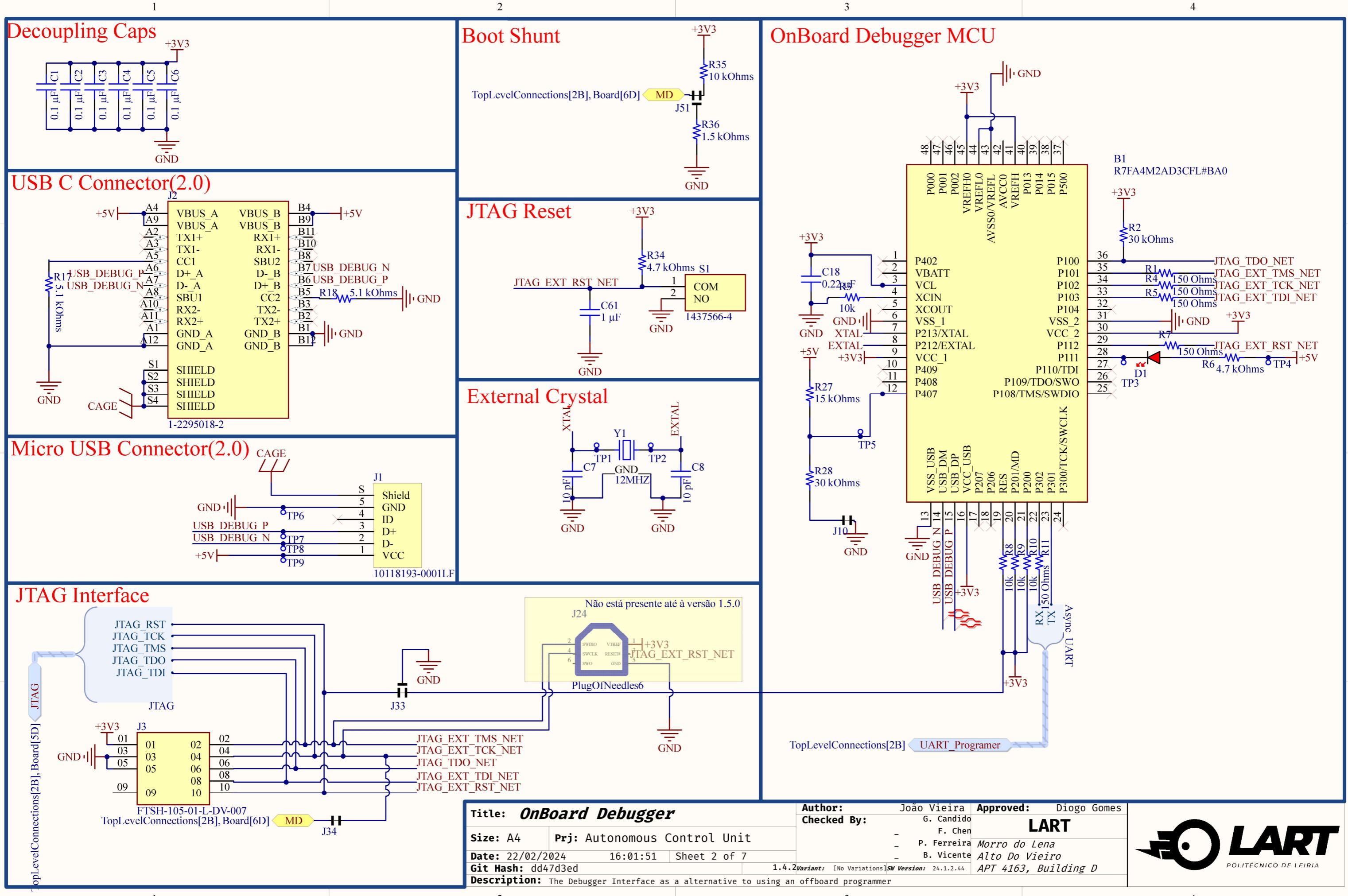
Description: An Abstract Representation of the wiring between schematics

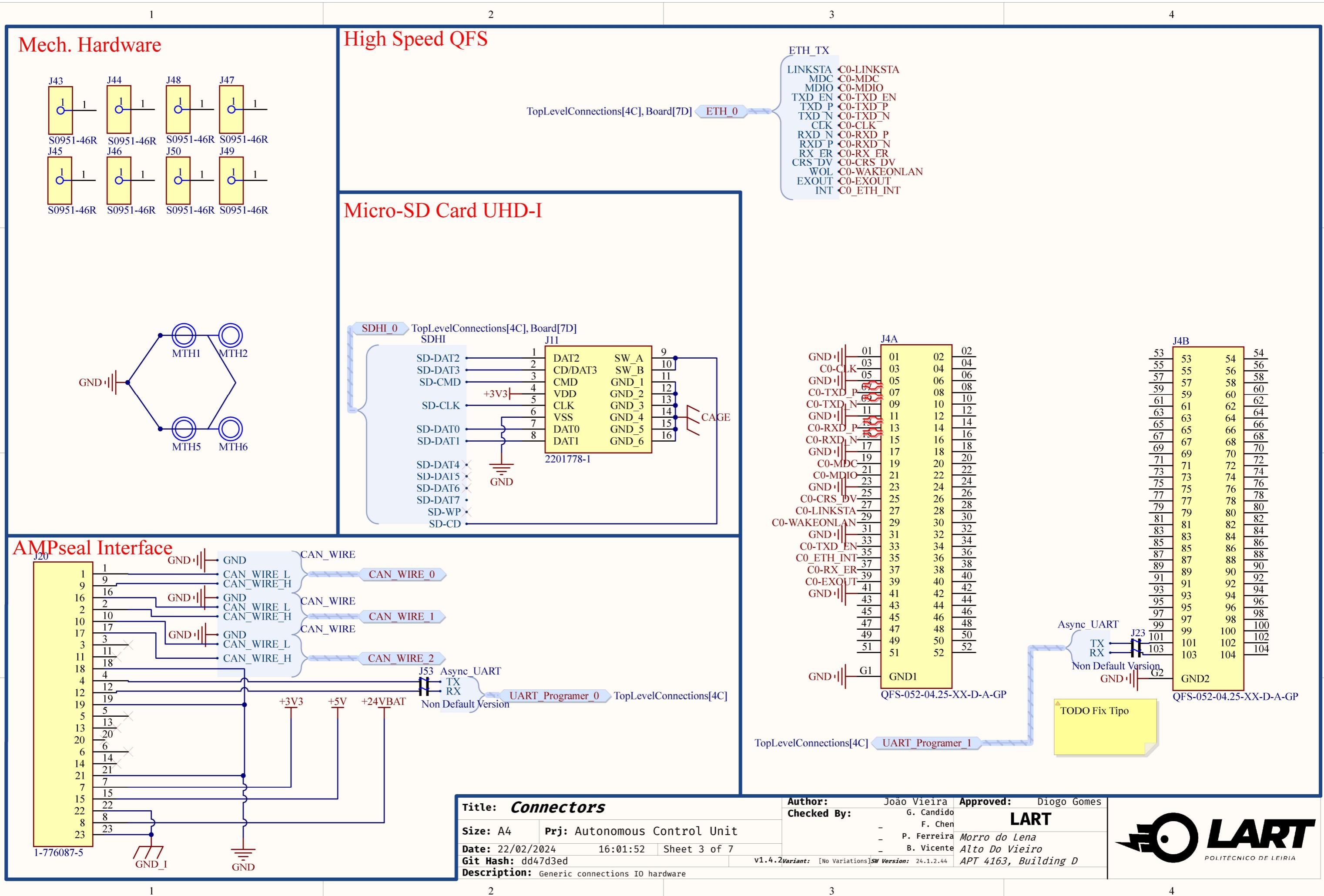
Author: João Vieira
Checked By:

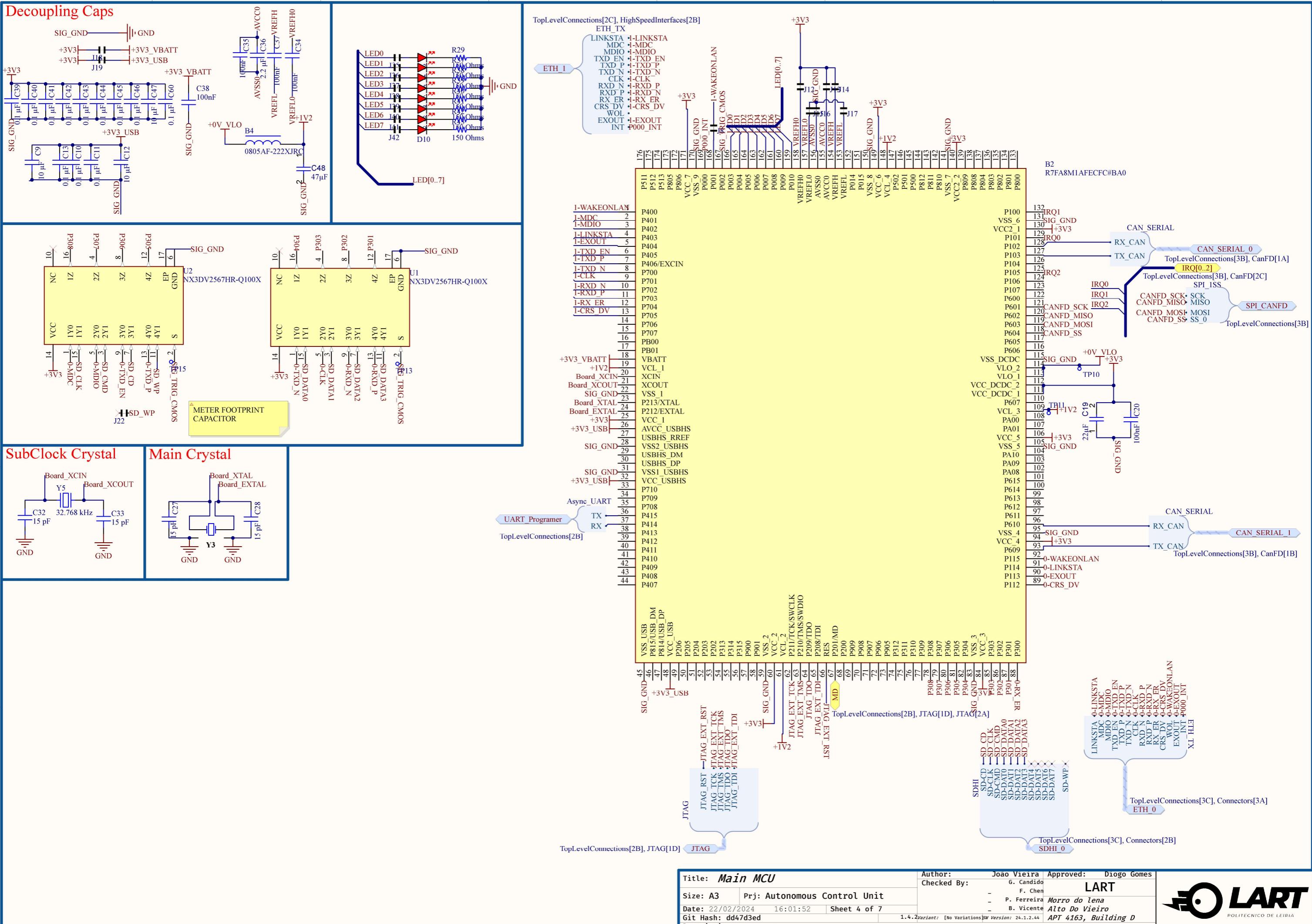
- G. Candido
- F. Chen
- P. Ferreira
- B. Vicente

Approved: Diogo Gomes

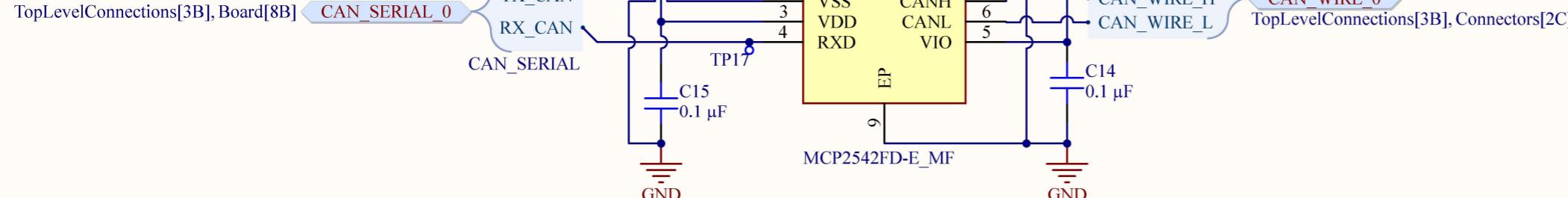
LART

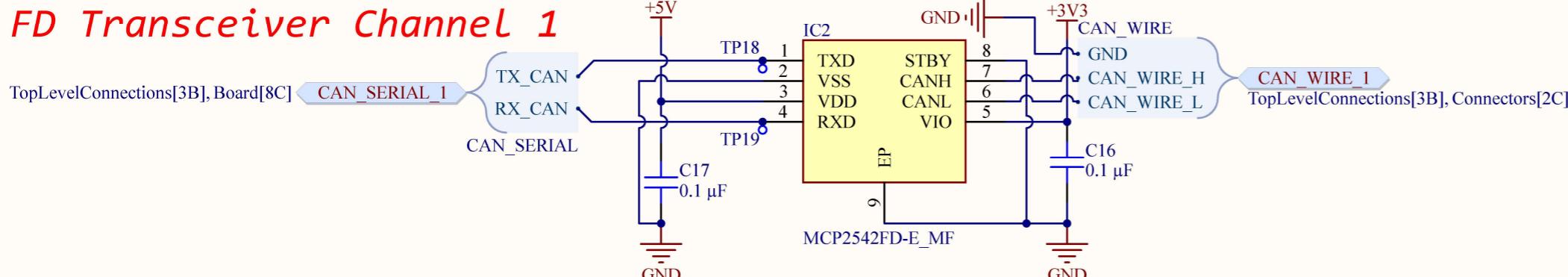




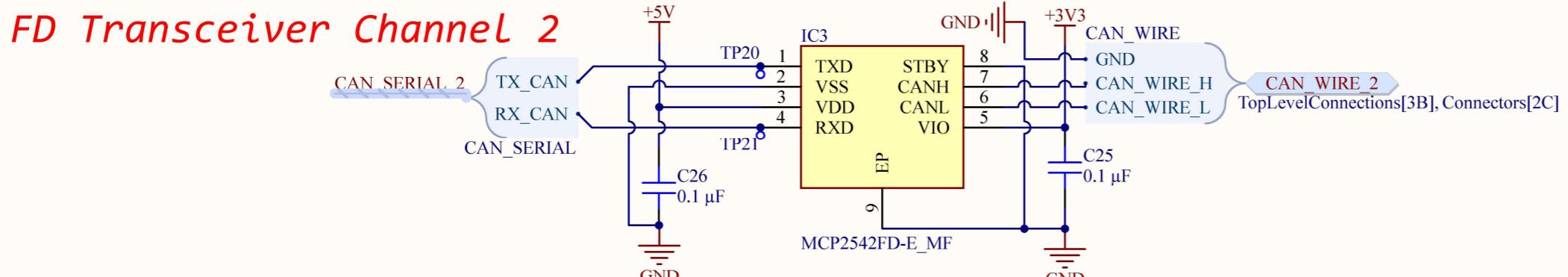
FD Transceiver Channel 0



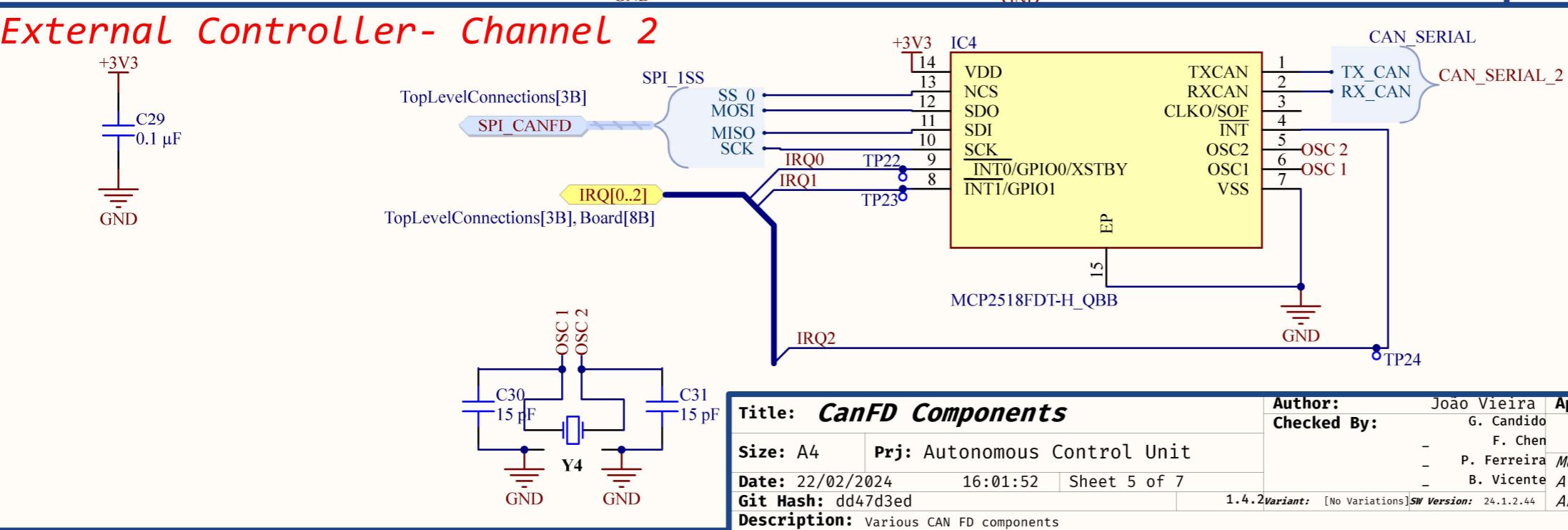
FD Transceiver Channel 1



FD Transceiver Channel 2

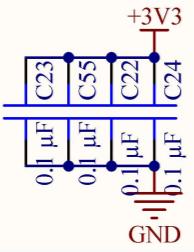


External Controller- Channel 2

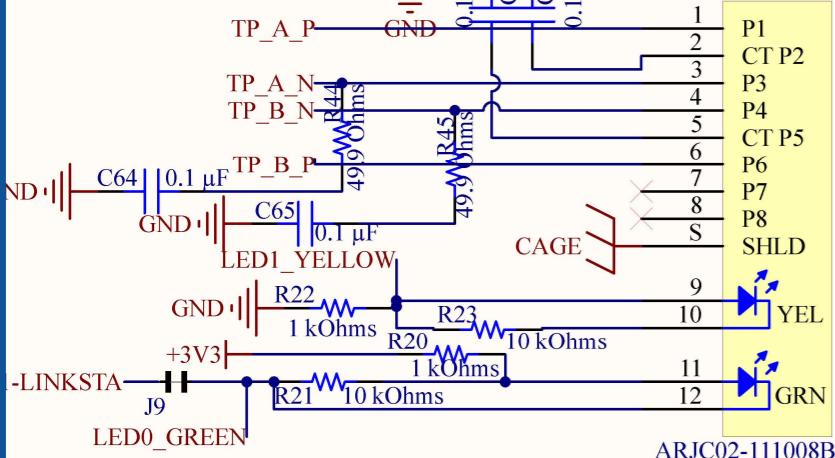


Bonus: Free Space :^)

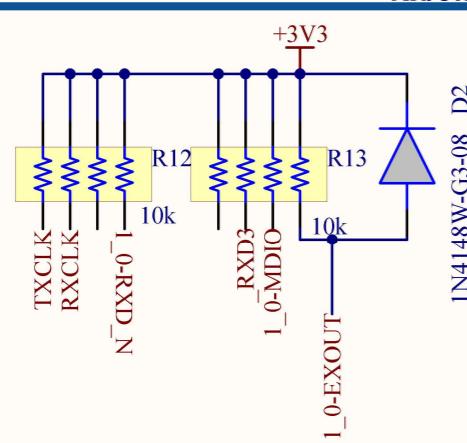
Decoupling Caps



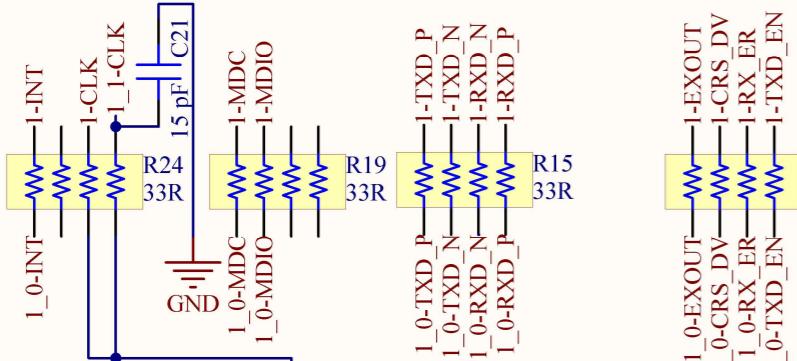
Harness Reference



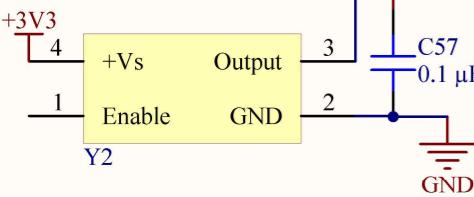
Pull Power



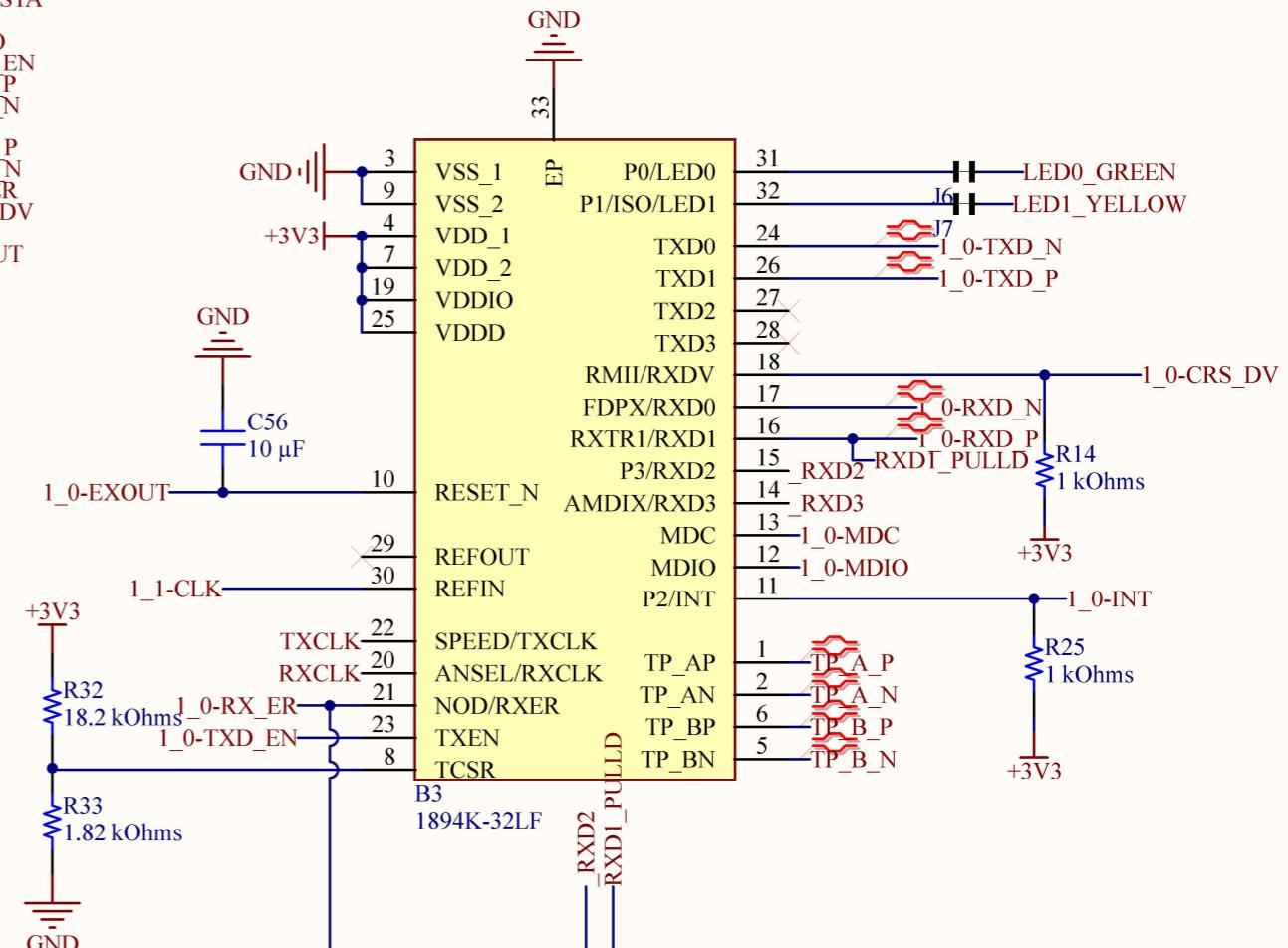
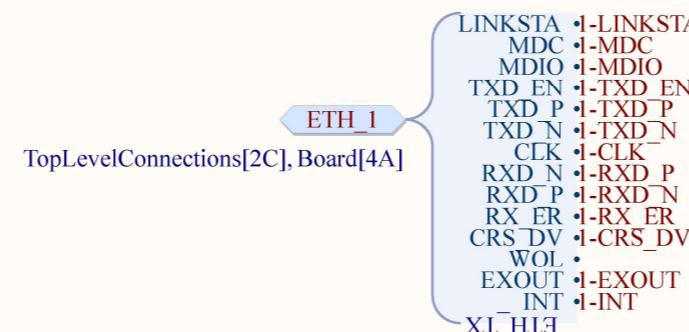
Termination Resistors



Resonator 50MHz



Ethernet PHY Base10/Base100



Title: High Speed Interfaces

Size: A4 **Prj:** Autonomous Control Unit

Date: 22/02/2024 **16:01:52** **Sheet 6 of 7**

Git Hash: dd47d3ed

Description: The various High Speed IOs, for now this only includes Ethernet

Author: João Vieira **Approved:** Diogo Gomes
Checked By: G. Cândido LART
F. Chen

P. Ferreira Morro do lena
B. Vicente Alto Do Vieiro

Variant: [No Variations] **SW Version:** 24.1.2.44 **APT 4163, Building D**



