

Title: **Top Level Sch Abstraction**

Size: A4 Prj: Autonomous Control Unit

Date: 24/02/2024 19:24:50 Sheet 1 of 7

Git Hash: dbc13111

Description: An Abstract Representation of the wiring between schematics

Author: João Vieira

Checked By: G. Candido

F. Chen

P. Ferreira

B. Vicente

1.4.2 Variant: [No Variations] SW Version: 24.1.2.44

Approved: Diogo Gomes

LART

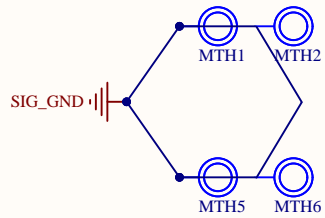
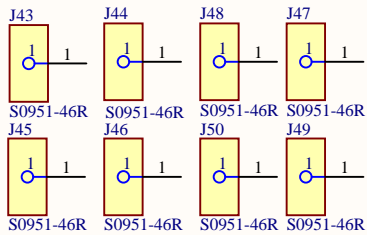
Morro do lena

Alto Do Vieiro

APT 4163, Building D



Mech. Hardware

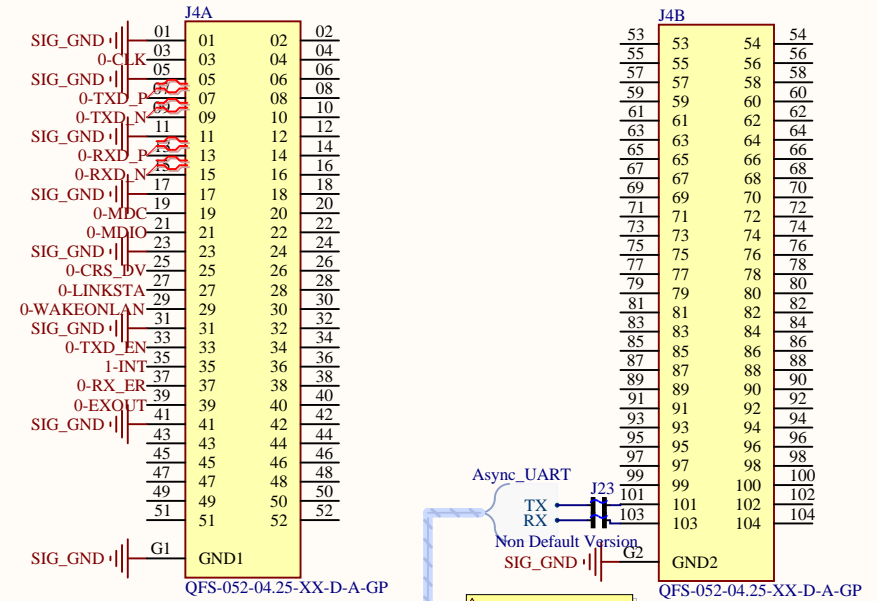
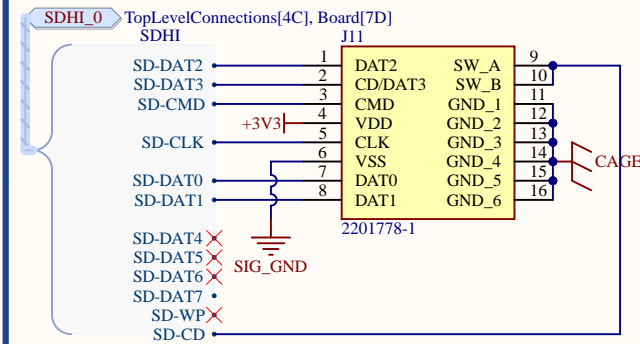


High Speed QFS

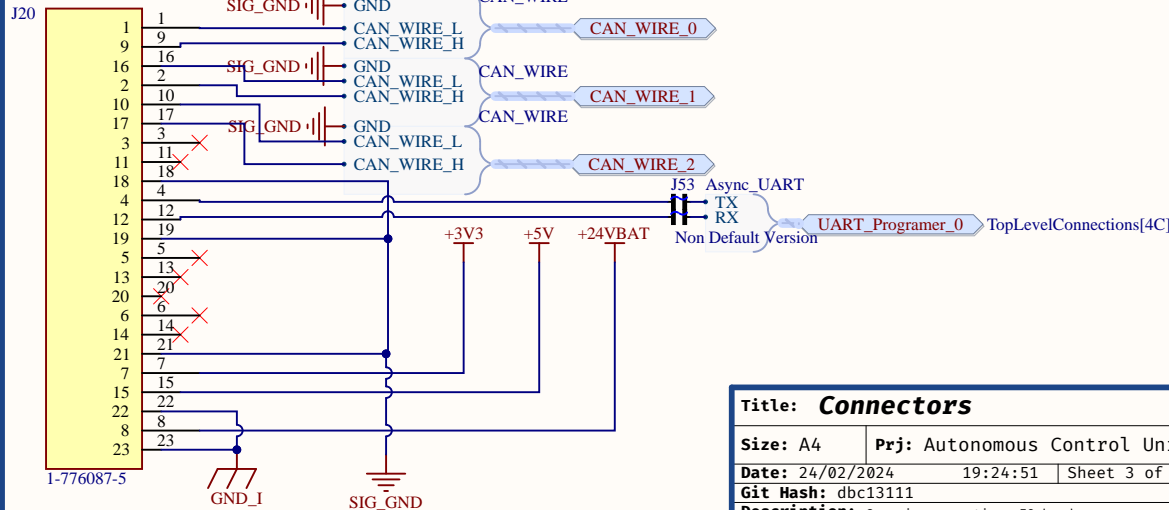
TopLevelConnections[4C], Board[7D] ETH_0

ETH_TX
LINKSTA 0-LINKSTA
MDC 0-MDC
MDIO 0-MDIO
TXD_EN 0-TXD_EN
TXD_P 0-TXD_P
TXD_N 0-TXD_N
CLK 0-CLK
RXD_N 0-RXD_P
RXD_P 0-RXD_N
RX_ER 0-RX_ER
CRS_DV 0-CRS_DV
WOL 0-WAKEONLAN
EXOUT 0-EXOUT
INT 1-INT

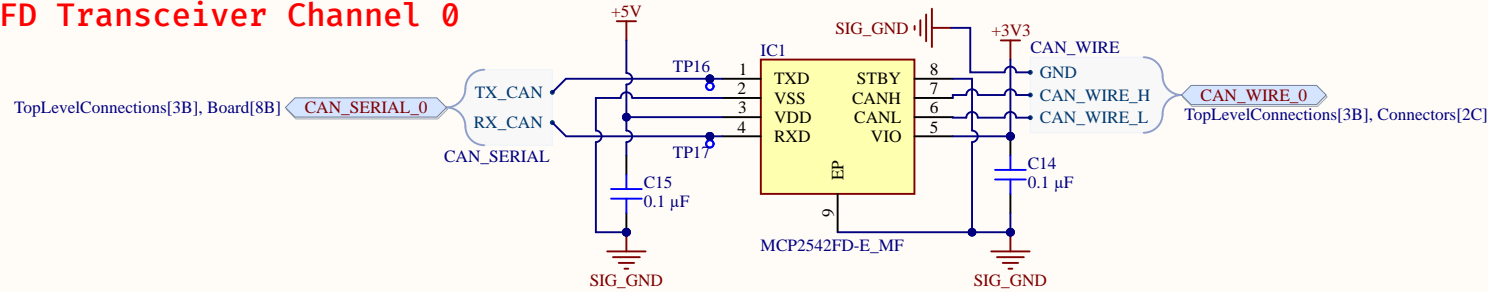
Micro-SD Card UHD-I



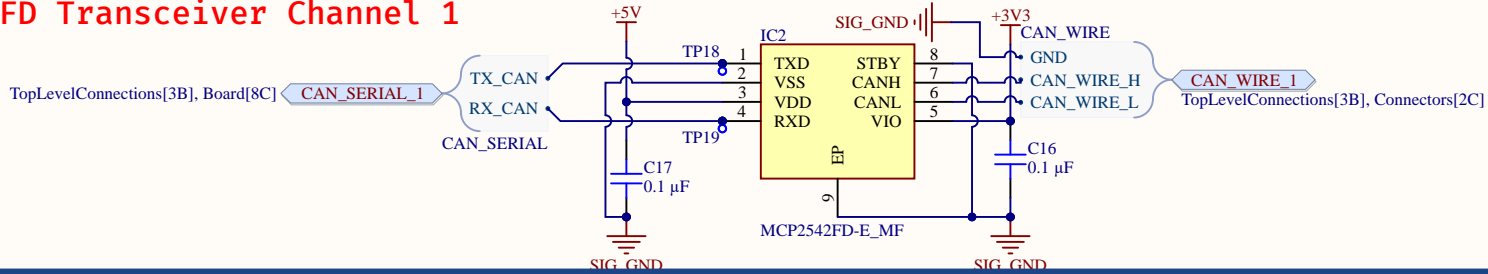
AMPseal Interface



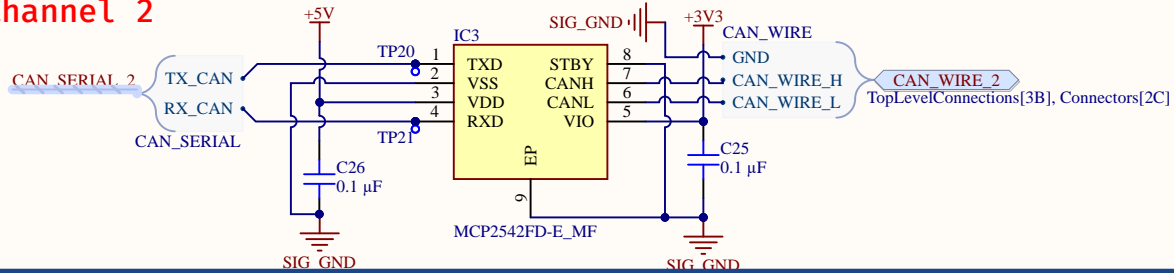
FD Transceiver Channel 0



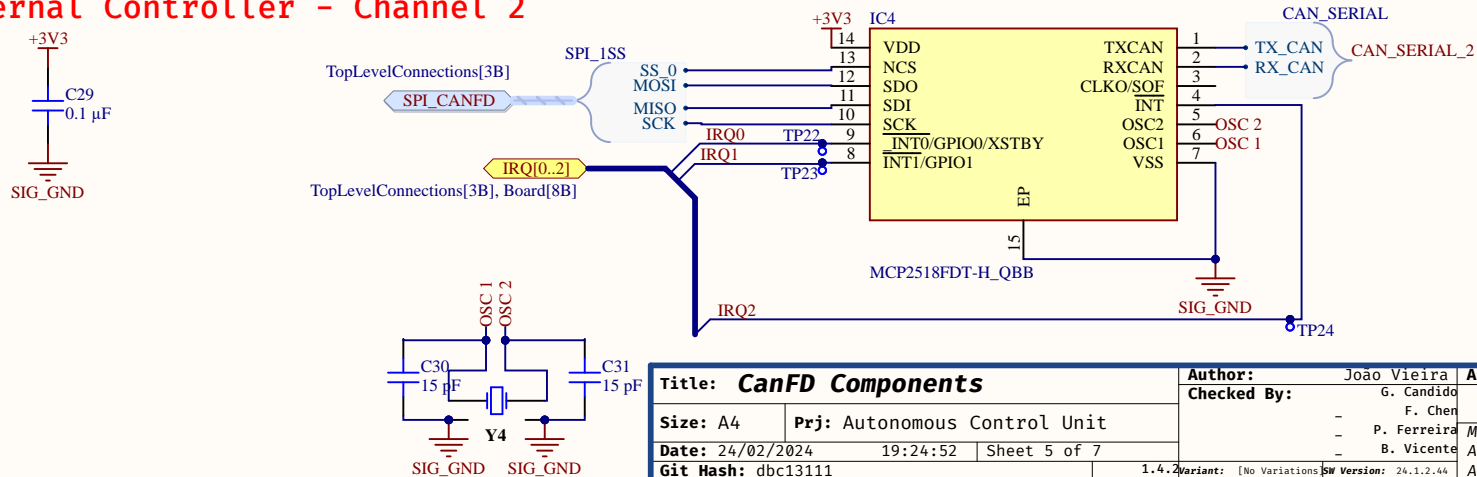
FD Transceiver Channel 1



FD Transceiver Channel 2



External Controller - Channel 2



Title: **CanFD Components**

Size: A4 Prj: Autonomous Control Unit

Date: 24/02/2024 19:24:52 Sheet 5 of 7

Git Hash: dbc13111

Description: Various CAN FD components

Author: João Vieira

Checked By: G. Candido

F. Chen

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B. Vicente

1.4.2 Variant: [No Variations] SW Version: 24.1.2.44

Approved: Diogo Gomes

LART

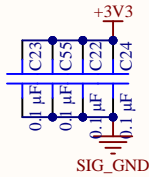
Morro do lena

Alto Do Vieiro

APT 4163, Building D

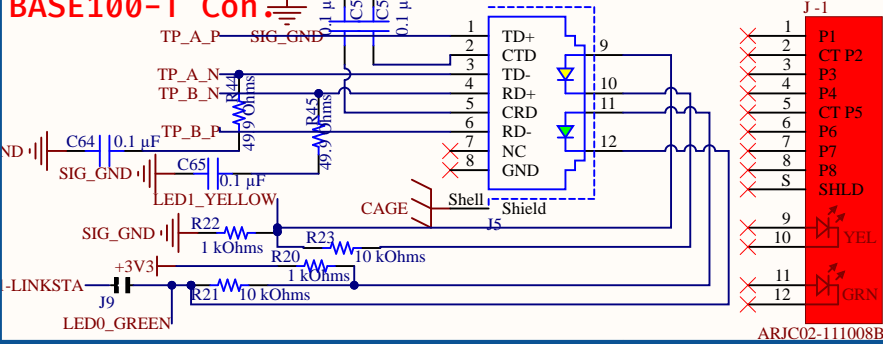


Decoupling Caps

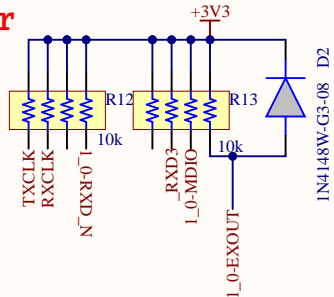


BASE100-T Con

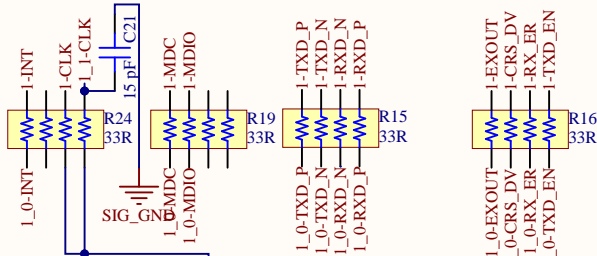
Este conector é axanado, ORIG ARJC02-111008B



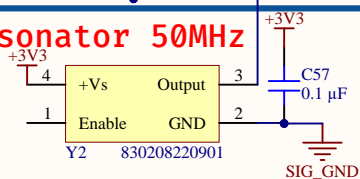
Pull Power



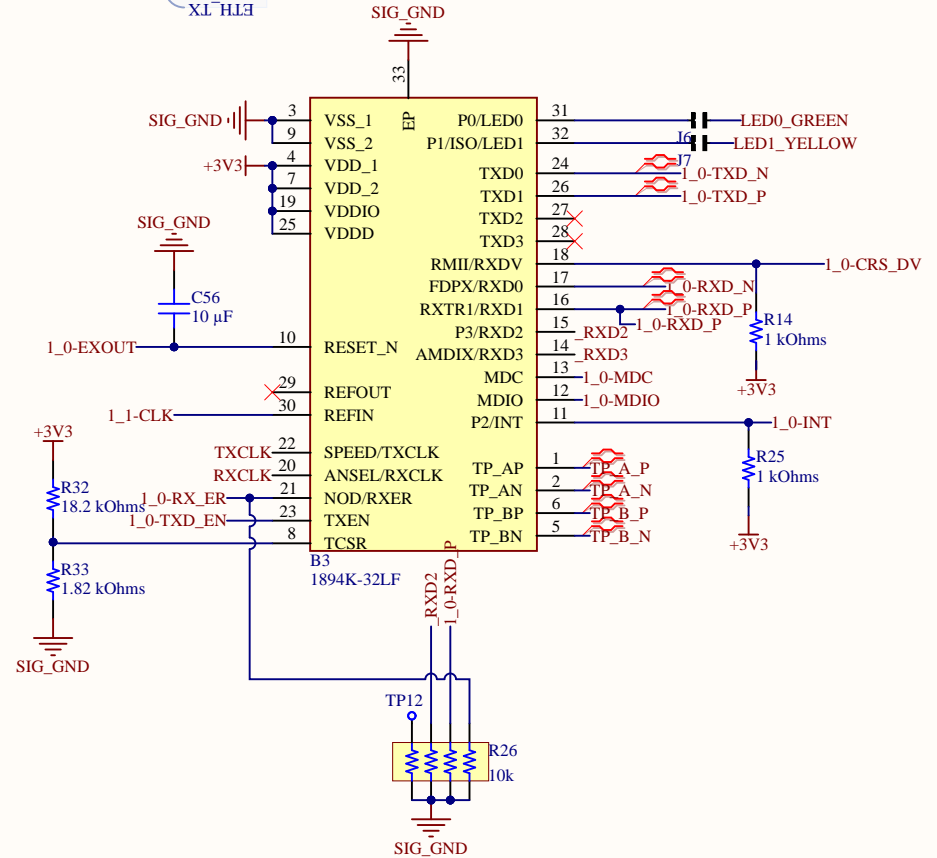
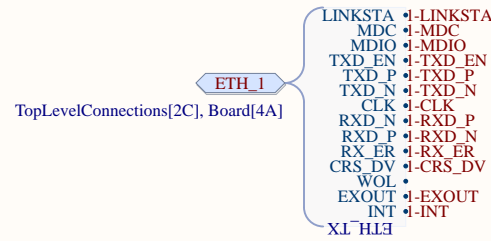
Termination Resistors



Resonator 50MHz



Ethernet PHY Base10/Base100



Title: **High Speed Interfaces**

Size: A4 Prj: Autonomous Control Unit

Date: 24/02/2024 19:24:52 Sheet 6 of 7

Git Hash: dbc13111

Description: The various High Speed I/Os, for now this only includes Ethernet

Author: João Vieira

Checked By: G. Candido

- F. Chen

- P. Ferreira

- B. Vicente

SW Version: 24.1.2.44

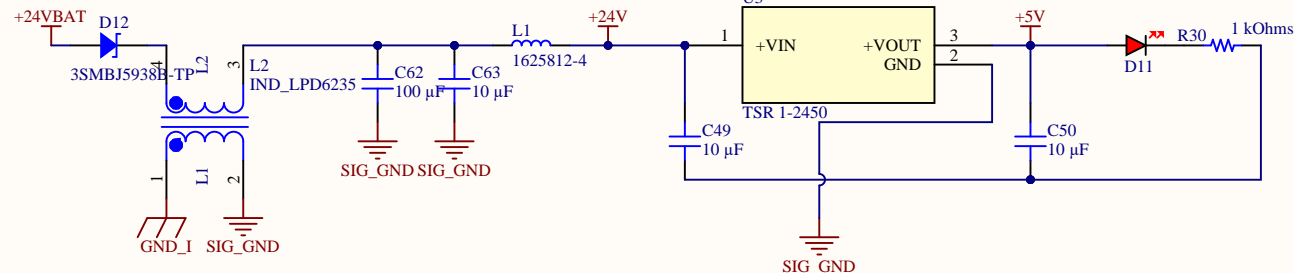
Approved: Diogo Gomes

LART

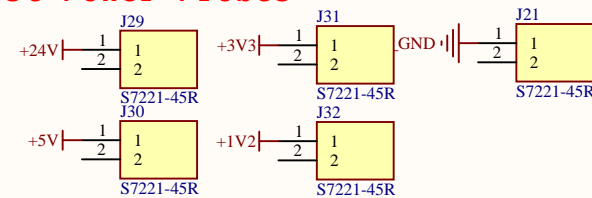
Morro do lena
Alto Do Vieiro
APT 4163, Building D



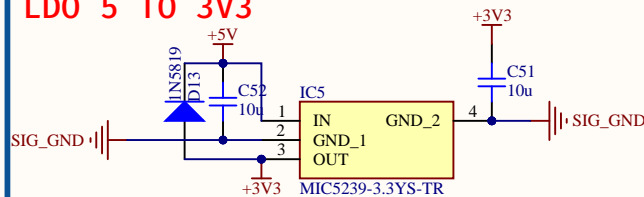
DC/DC Step Down 24V TO 5V



Test Power Probes

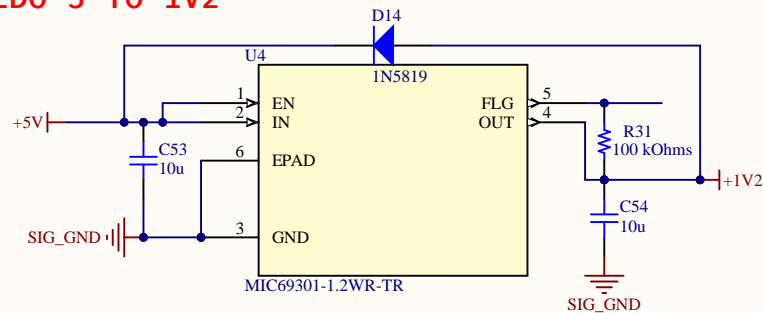


LDO 5 TO 3V3



Bonus: Free Space :^)

LDO 5 TO 1V2



TODO: add backup super-cap circuit

Title: Power			Author: João Vieira	Approved: Diogo Gomes
Size: A4	Prj: Autonomous Control Unit		Checked By: G. Candido	LART Morro do lena Alto Do Vieiro APT 4163, Building D
Date: 24/02/2024	19:24:52	Sheet 7 of 7	- F. Chen	
Git Hash: dbc13111		1.4.2 Variant: [No Variations] SW Version: 24.1.2.44	- P. Ferreira	
Description: Includes the various reference voltages needed to power all the chips in the ACU			- B. Vicente	

