**Introduction**: Perform addition and multiplication on selected inputs and select the operation wanted using a 2 to 1 mux circuit.

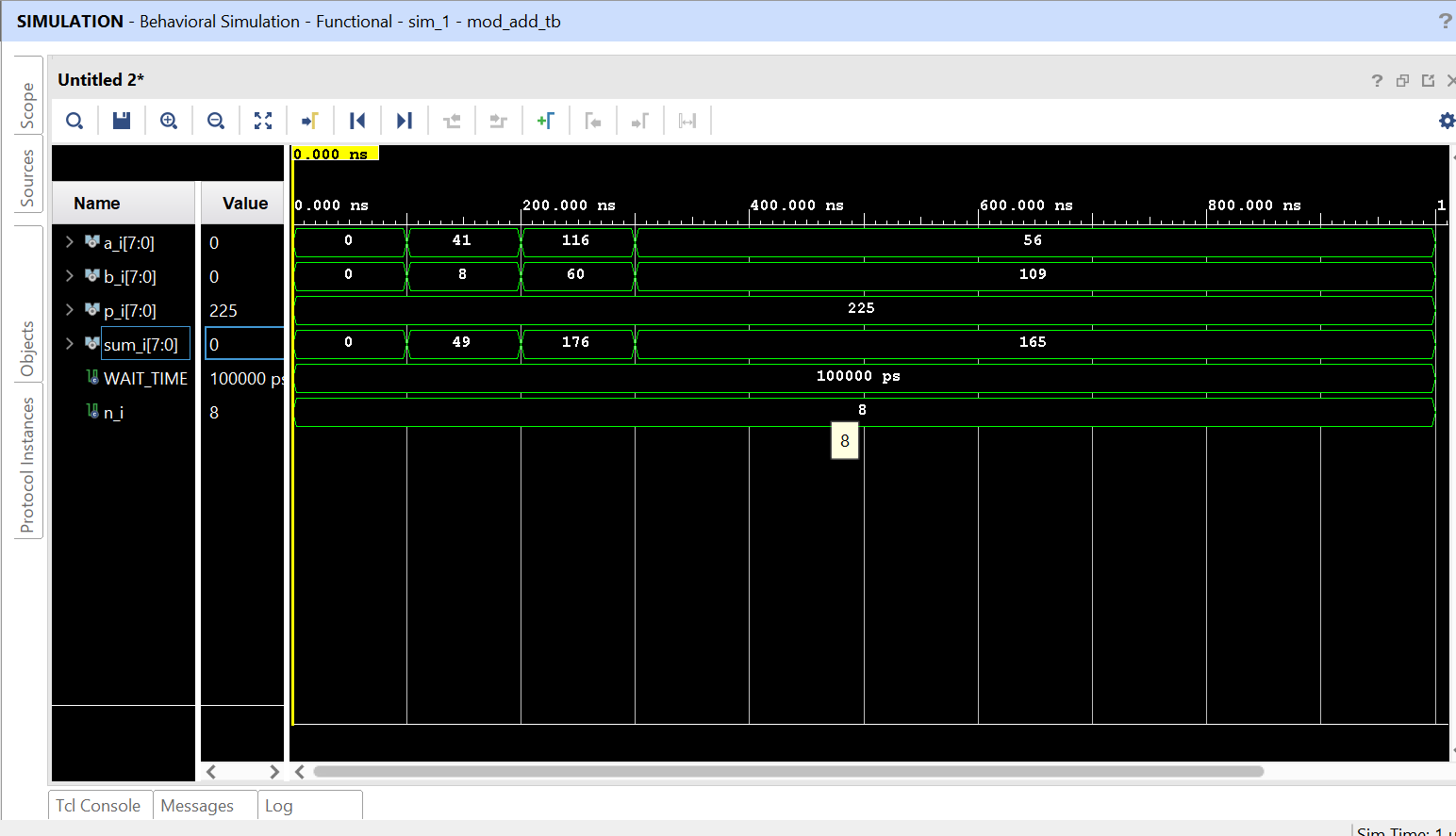
**Purpose**: to perform operations ( addition or multiplication ) on 8-bit input data

**Materials used**: Nexys4 DDR board with Artix -7 FPGA, USB cable, laptop, Vivado Software.

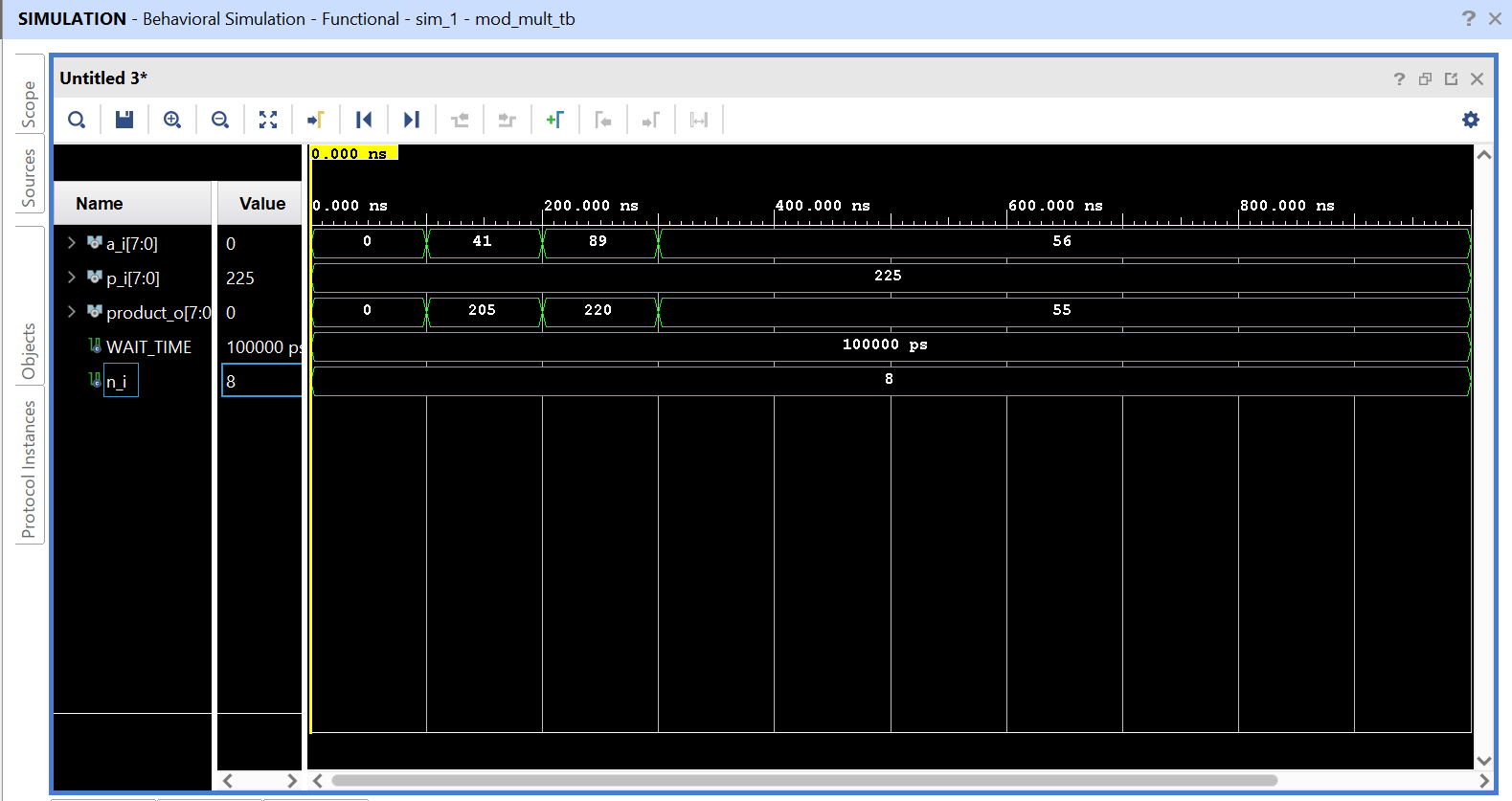
**Results**:

**Waveform**

**Addition : p = 225 Z number ends with 45**

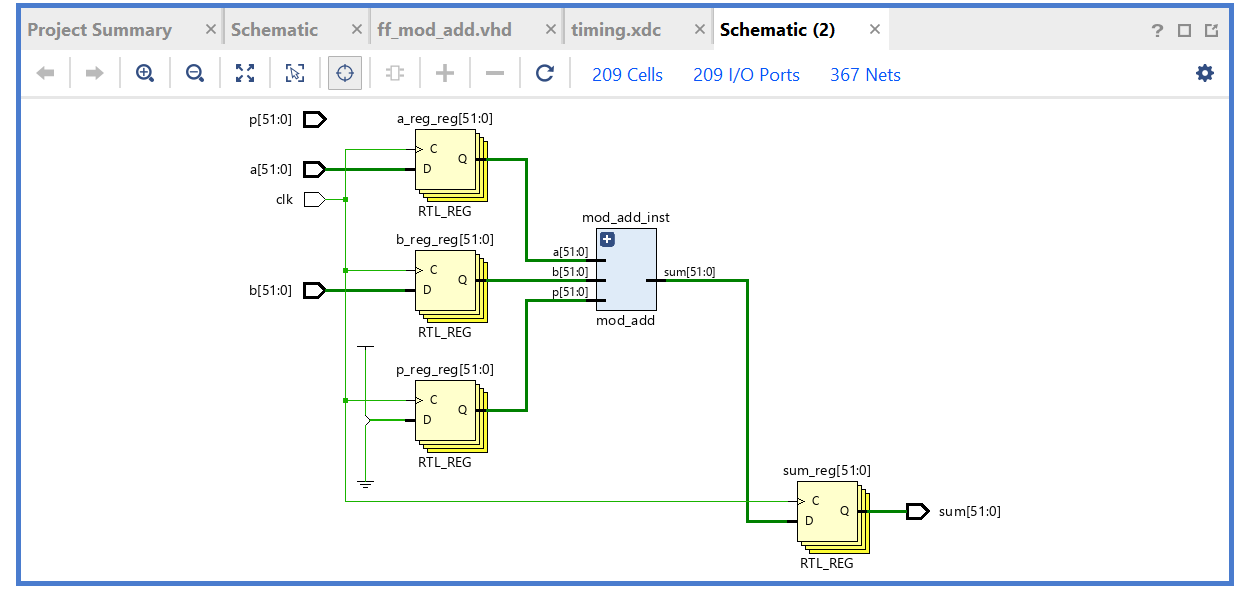


**Multiplication : p = 225 Z number ends with 45**



**Time and Area Report for Mod Add**

**Schematic with flip fops p = 22ba8c1cc230d**



**Info on both Reports**

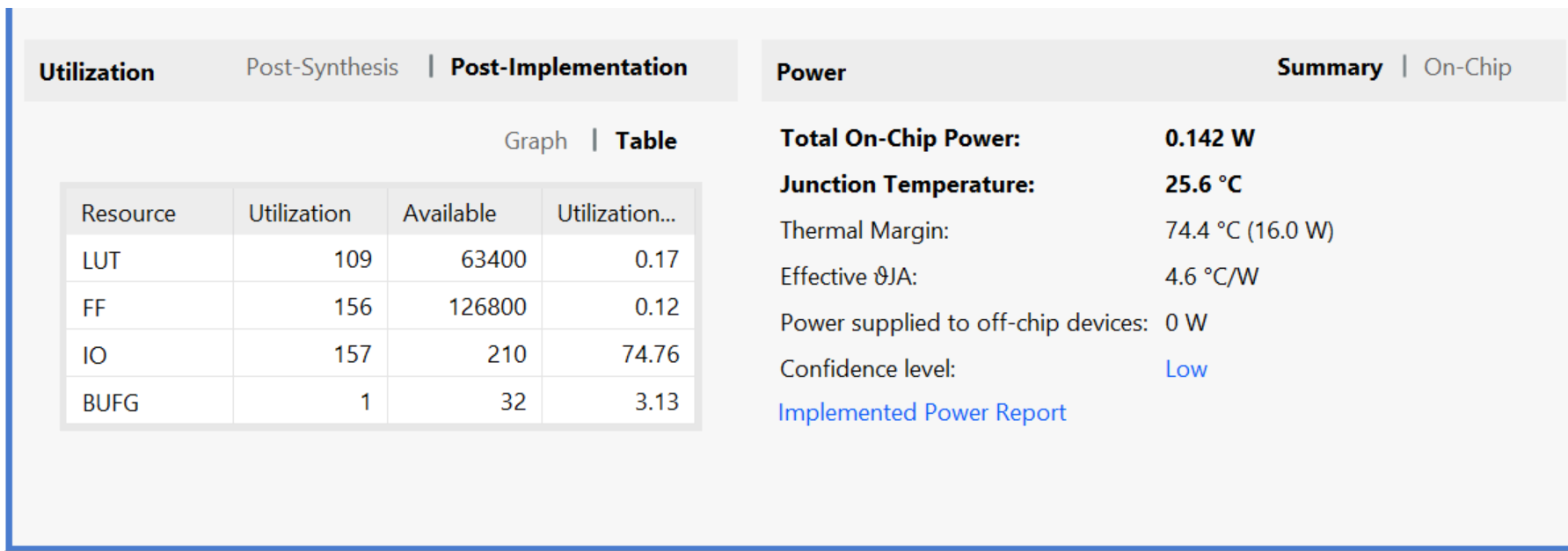
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Slices**  **LUT’s used** | **Slices used** | **Slack** | **CPD** | **M. Frequency** | **Logic levels** | **Data path Delay** |
| **109** | **64** | **3.489 ns** | **6.511ns** | **153586.2 MHz** | **17** | **6.530 ns** |

**CPD = Required – Slack**

**CPD = 10 ns – 3.489 ns**

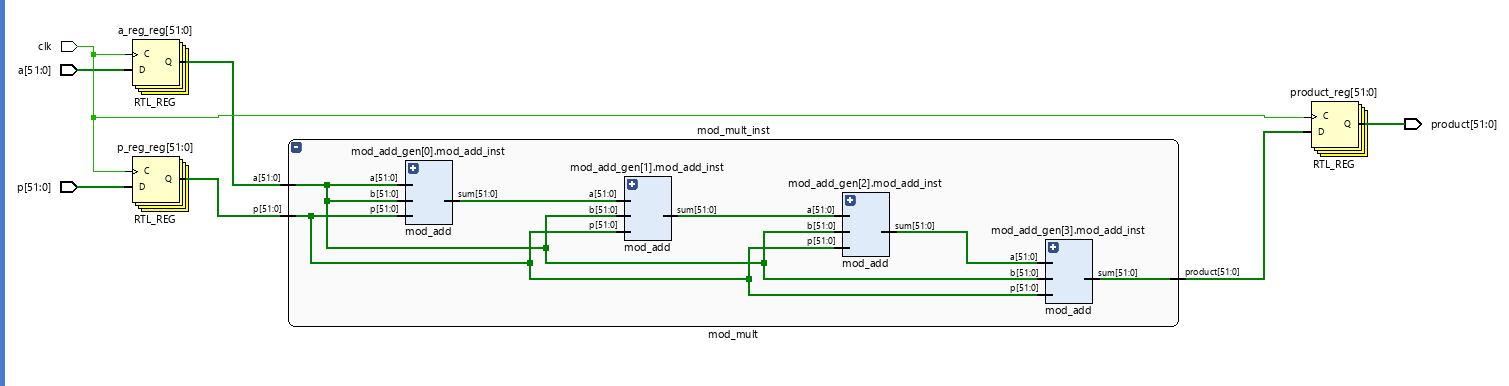
**Frequency in MHz = (1/CPD) \* 10^6**

**Table(add)**



**Time and Area Report for Mult Add**

**Schematic with flip fops p = p\_reg**



**Info on both Reports**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Slices**  **LUT’s used** | **Slices used** | **Slack** | **CPD** | **M. Frequency** | **Logic levels** | **Data path Delay** |
| **416** | **126** | **-4.439 ns** | **14.439 ns** | **69256.87 MHz** | **66** | **14.320 ns** |

**CPD = Required – Slack**

**CPD = 10 – (-4.439)**

**Frequency in MHz = (1/CPD) \* 10^6**

**Table (mult)**

