LAB03 PATH SUM

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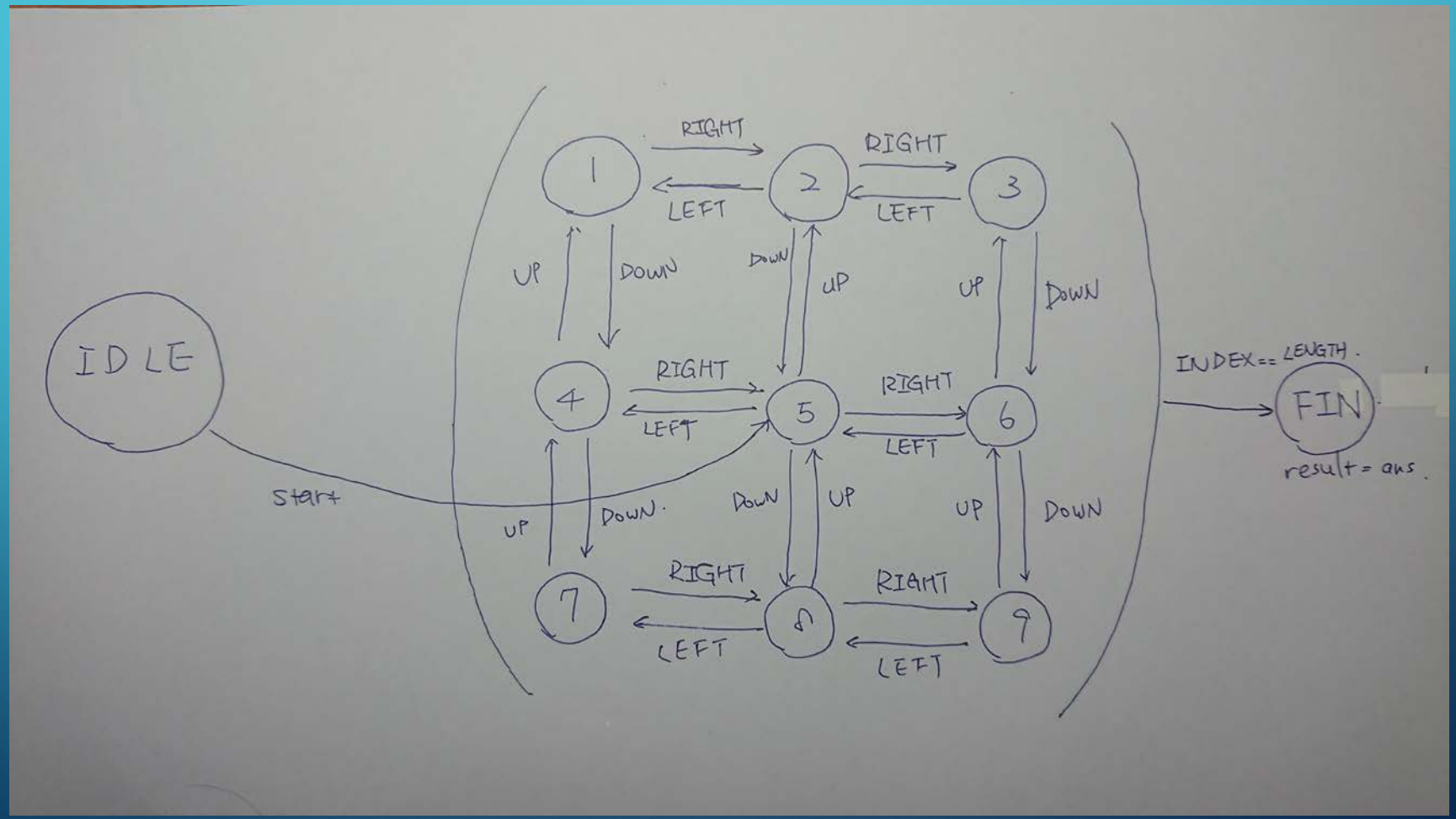
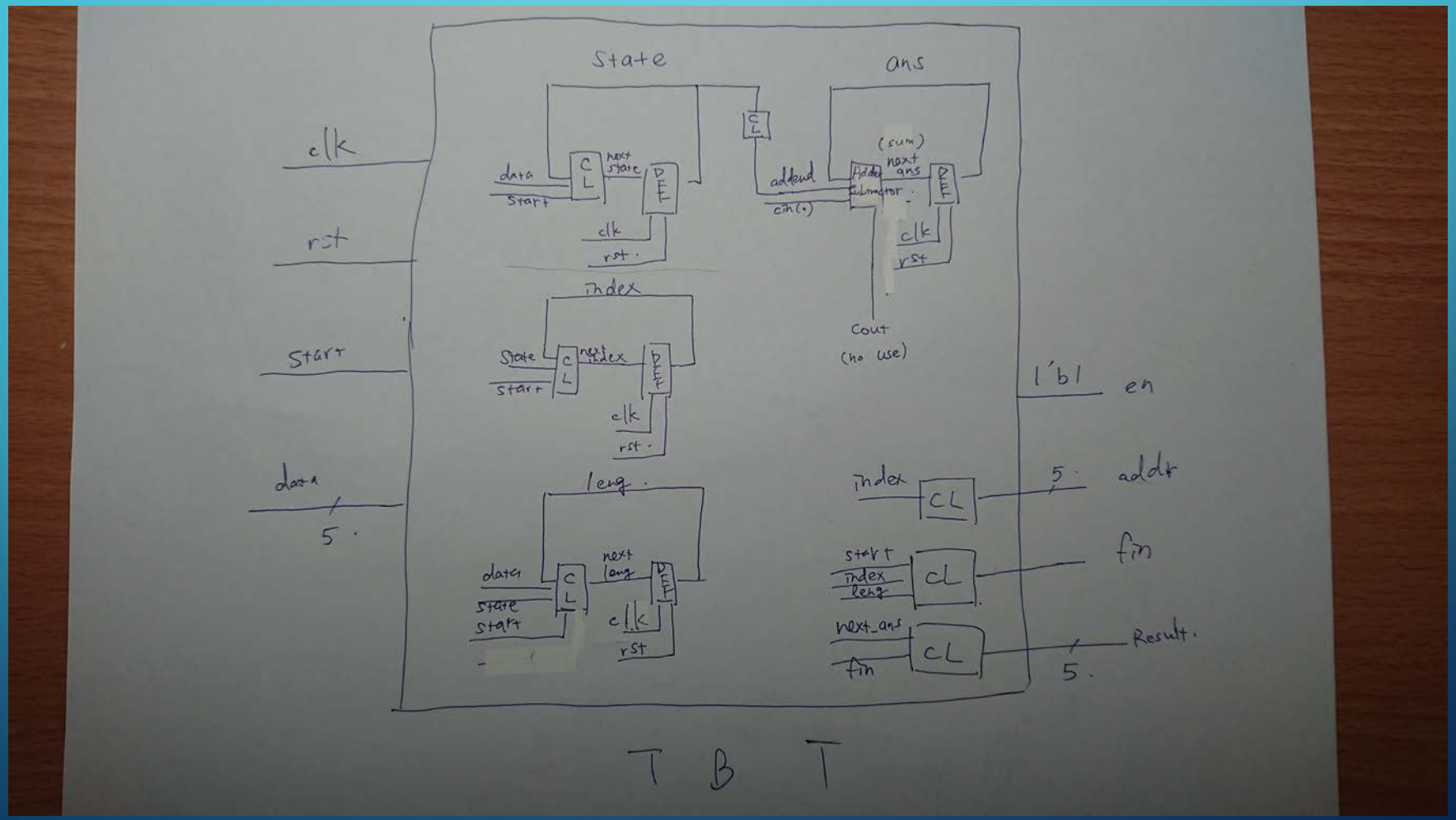
STATE TRANSITION GRAPH



BLOCK DIAGRAM



MAKE SIM

```
                worklib.TBT:v <0x1ee2fd22>
                        streams:   8, words:  7567
                worklib.TBT_tb:v <0x69edb1f1>
                        streams:   5, words:  6396
        Building instance specific data structures.
        Loading native compiled code:     ..................... Done
        Design hierarchy summary:
                                Instances  Unique
                Modules:                3       3
                Primitives:            30       3
                Registers:             16      16
                Scalar wires:           7       -
                Expanded wires:        10       2
                Vectored wires:         3       -
                Always blocks:          3       3
                Initial blocks:         3       3
                Cont. assignments:      3       4
                Pseudo assignments:     2       2
                Simulation timescale:  100ps
        Writing initial simulation snapshot: worklib.TBT_tb:v
Loading snapshot worklib.TBT_tb:v ..................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_L-2016.06-SP1-1, Linux, 09/27/2016
(C) 1996 - 2016 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi3* : Create FSDB file 'TBT.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.


Result =  -1 , Answer =  -1
!!!!! ACCEPTED !!!!!

Simulation complete via $finish(1) at time 390 NS + 0
./TBT_tb.v:85           $finish;
ncsim> exit
```

MAKE SYN

```
*Verdi3* : Create FSDB file 'TBT_syn.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.


Warning!  Timing violation
           $setuphold<setup>( negedge G &&& (SandR == 1):32468 PS, negedge D:32400 PS,  0.112 : 112 PS,  0.084 : 84 PS );
            File: /theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v, line = 26241
           Scope: TBT_tb.tbt.\addend_reg[1]
            Time: 32468 PS


Warning!  Timing violation
           $setuphold<setup>( negedge G &&& (SandR == 1):225853 PS, negedge D:225804 PS,  0.106 : 106 PS,  0.080 : 80 PS );
            File: /theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v, line = 26241
           Scope: TBT_tb.tbt.\addend_reg[0]
            Time: 225853 PS


Warning!  Timing violation
           $setuphold<setup>( negedge G &&& (SandR == 1):285879 PS, negedge D:285830 PS,  0.106 : 106 PS,  0.080 : 80 PS );
            File: /theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v, line = 26241
           Scope: TBT_tb.tbt.\addend_reg[0]
            Time: 285879 PS


Warning!  Timing violation
           $setuphold<setup>( negedge G &&& (SandR == 1):346340 PS, negedge D:346272 PS,  0.112 : 112 PS,  0.084 : 84 PS );
            File: /theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v, line = 26241
           Scope: TBT_tb.tbt.\addend_reg[1]
            Time: 346340 PS


Result =  -1 , Answer =  -1
!!!!! ACCEPTED !!!!!

Simulation complete via $finish(1) at time 390 NS + 0
./TBT_tb.v:85           $finish;
ncsim> exit
```

問題與討論

- 不知道為什麼make syn會產生Timing violation?
  - 根據網路上的說法，這是由於data的set up time跟hold time時間不足而造成的，不過在此次報告中並不影響結果，可能可以透過設定clock的period或是多加register或是buffer來解決問題。(參考資料)
- 了解到在給CL的值是固定的時候(如此次要給adderSubtractor的Cin)可以直接給定值(如.cin(1'b0)).

問題與討論

- 由於最後一次的DFF跑完之後，正確答案是存在next_ans裡面，所以result不能取ans(會取到上個答案).

THANK YOU