MODULE 3
PHYSICS OF SEMICONDUCTOR

Q1. What are direct and indirect band gap semiconductors?

ANS: When electrons recombine with holes some amount of energy is released. When the energy released is in the form of heat, such semiconductors are called indirect band gap semiconductors. Example: Si, Ge. But In some semiconductors, energy released in electron-hole recombination is given in the form of photon. Such semiconductor are called direct band gap semiconductor. Example: GaAs. GaP etc.

Q2. What is Fermi level? Write Fermi Dirac distribution function?

ANS: While filling up the bands, electrons fills the lowest level first, then the next and so on till all the electrons are accommodated, the highest level occupied by the electron is called Fermi level and the corresponding energy is called Fermi Energy.

The Fermi Dirac function is given by

$$f(E) = \frac{1}{1 + e^{\frac{E - E_f}{KT}}}$$

f(E) is the probability of finding the electron in energy level E

E_f is the Fermi level

K is Boltzmann constant K= 1.38 X 10^{-23} J/K

T is temp in Kelvin

Q3. Explain the variation of Fermi level at different temperature in conductors. Discuss the distribution function graph.

ANS: In conductors, conduction and valence band overlaps. The highest level occupied by the charge carrier is called Fermi level.

We know the Fermi Dirac distribution function is f(E) = $\frac{1}{1+e^{\frac{E-E_f}{KT}}}$

1) At T = 0 K

At 0K, electrons occupy the lower energy levels in the C.B leaving upper level vacant. E_f is the maximum energy that an electron can have at 0K.

a) T=0K, for energy levels E below E_f ($E < E_f$)

f (E) = $\frac{1}{1+e^{-\infty}} = \frac{1}{1+0} = 1$

Therefore,f(E) = 1means that all levels below E_f are filled.

b) At T= 0K for energy levels above E_f ($E > E_f$)

f (E) = $\frac{1}{1+e^{\infty}} = \frac{1}{1+\infty} = \frac{1}{\infty} = 0$

Therefore, f(E) =0 means that all levels above E_f are vacant.

c) At T= 0K for E = E_f

f(E) = $\frac{1}{1+e^{\frac{0}{0}}}$ which is in indeterminate.

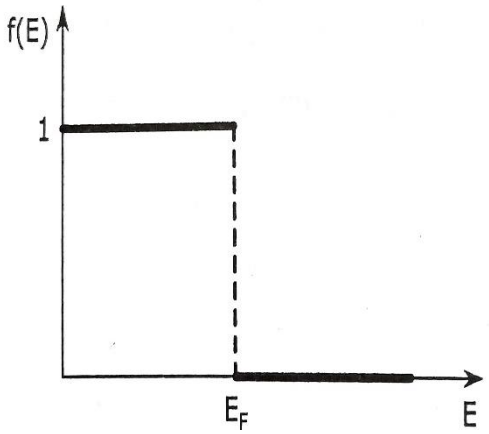


Fig: Distribution function graph for T = 0 K

2) At T> 0K, with the increase in temperature, electrons are excited to vacant levels above Fermi level that are in the levels adjacent to Fermi level. Electrons which are deeper will not find this change. So, the probability of finding electrons at levels E > Ef becomes greater than zero and probability at a few lower levels E < E_f to E_f becomes less than unity.

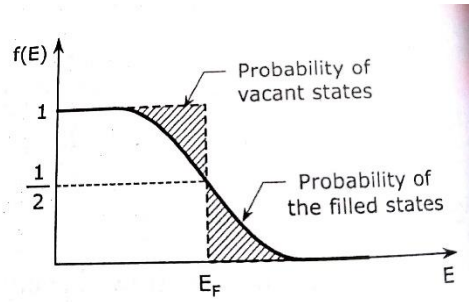


Fig: Distribution function graph for T > 0 K

Q4. Show that Fermi level in an intrinsic semiconductor lies midway of conduction and valence band.

ANS: Let n_c be the number of electrons in CB and n_v be number of electrons in valence band. Total number of electrons in both the band is N = n_c + n_v .

Probability of finding the electron in conduction band is f (E_c) = $\frac{n_c}{N}$

Probability of finding the electron in valence on band is f (E_v) = $\frac{n_v}{N}$

Therefore, n_c = N.f(E_c) that is $n_c = \frac{1}{1+ e^{\frac{Ec - Ef}{KT}}}$

Similarly, n_v = N.f(Ev) that is $n_v = \frac{1}{1+ e^{\frac{Ev - Ef}{KT}}}$

We know N = $n_c + n_v$

Therefore, N = $\frac{N}{1+ e^{\frac{Ec - Ef}{KT}}} + \frac{N}{1+ e^{\frac{Ev - Ef}{KT}}}$

That is, 1 = $\frac{1}{1+e^{\frac{Ec-Ef}{KT}}} + \frac{1}{1+e^{\frac{Ev-Ef}{KT}}}$

Let x = $\frac{Ec-Ef}{KT}$ and y = $\frac{Ev-Ef}{KT}$

Therefore, 1 = $\frac{1}{1+e^{x}} + \frac{1}{1+e^{y}}$

$(1+e^{x})(1+e^{y}) = 1+e^{x}+1+e^{y}$

$1+e^{x}+e^{y}+e^{x}.e^{y} = 1+e^{x}+1+e^{y}$

Therefore, $e^{(x+y)} = 1$

Taking ln on both side

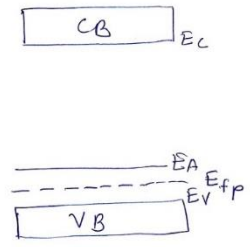
X =y = 0

i.e $\frac{Ec-Ef}{KT} + \frac{Ev-Ef}{KT} = 0$

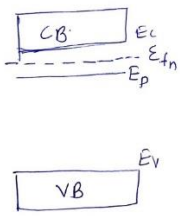
Therefore, $E_c + E_v - 2E_f = 0$

$E_f = \frac{Ec+Ev}{2}$

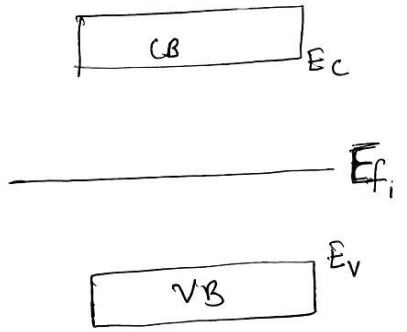
<u>Position of fermi level in P type</u>



<u>Position of fermi level in N type</u>



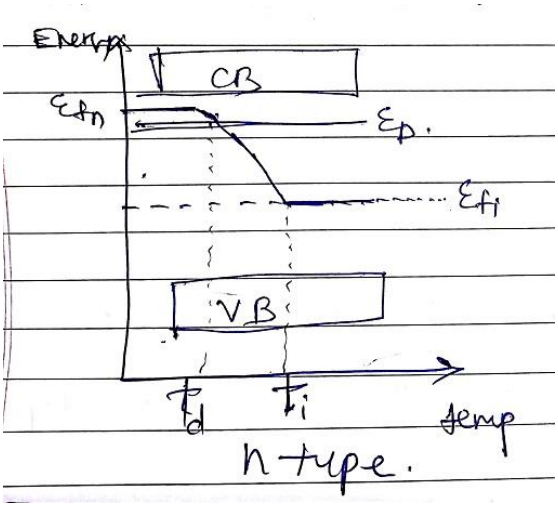
Position of fermi level in an intrinsic semiconductor:



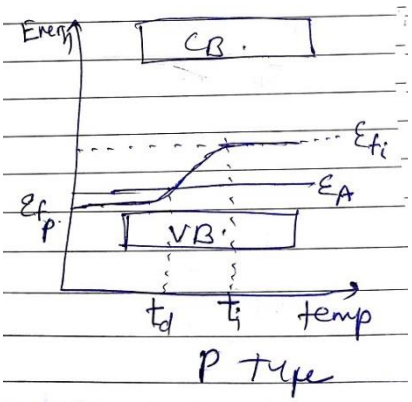
Q5. Draw and explain the energy level diagram to show the effect of temperature and impurity concentration on Fermi level in an extrinsic semiconductor.

ANS: Effect of temperature on N type and P type semiconductor:

N type:



P type:



For n type:

At 0K, donor levels are filled. All the donor electrons are bound to donor atoms. As the temperature increases, donor atom get io0nized and donor electron go into conduction band. At about 100 K all the donor atoms are ionized. Once all the electrons from donor level are excited into CB any further increase does not create additional electrons. This stage is called depletion stage. Further rise in temperature create the transitions from VB to CB.

For n type s/c, At 0 K, Fermi level is located between E_D and E_C

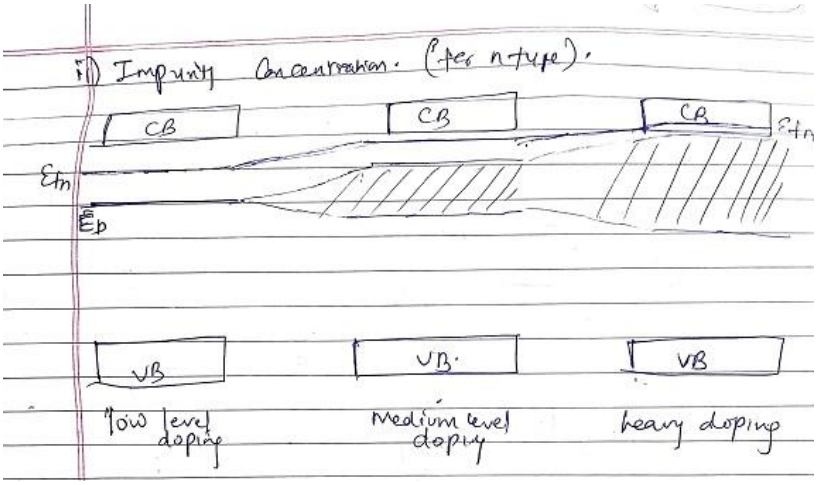
With increase in temperature, donor level gets depleted and E_F shifts downwards. At the temp of depletion t_d , E_F coincides with donor level $E_{fn} = E_D$.

As the temp grows further above t_d Fermi level shifts downward further till intrinsic region starts. At this temp, E_F approaches the intrinsic value.

$E_{Fn} = E_{Fi}$ and extrinsic s/c becomes intrinsic and E_F will be independent of temperature

2) Impurity concentration (for n type)

The addition of donor impurity to an intrinsic s/c leads to the formation of discrete donor levels below the bottom edge of CB. At low impurity concentration, the impurity atoms are spaced far apart and do not interact with each other. With an increase in impurity concentration, impurity atoms separation in crystal decreases and they tend to interact. Consequently, donor levels also undergo splitting and forms a band below the CB. The larger the doping concentration, the broader is the impurity band and at one stage it overlaps on the CB. It results in the accessibility of upper vacant levels in CB to the donor electrons. This broadening of donor level is accompanied by a decrease in the width of forbidden gap and also by upward displacement of Fermi level. For heavily doped n type S/C. Fermi level lies within the CB.



Q6. Define the following terms:

i) Mobility: It is defined as drift velocity per unit electric field. $\mu = v_d / E$

It signifies how swiftly the charge carrier responds to the electric field. Its unit is m^2 / V-Sec.

ii) Drift velocity: The net movement of electrons under the influence of external electric field is called drift and the corresponding velocity is called drift velocity. v_d

iii) Resistance: The opposition to the electron motion in material is manifest as resistance. 'R' is geometry dependent property. $R \alpha L / A$ i.e $R = \rho L/A$. ρ is called resistivity. Its unit is Ω m.

iv) Reciprocal of resistance is called conductance G and reciprocal of resistivity is called conductivity

$1/ \Omega$ m

v) Relation between Mobility and conductivity:

Let us consider a rectangular slab of length L, area of cross section A. Let n be the concentration of electron in it. The total number of electrons in the solid N = nAL

Total charge on an electron Q= Ne

Current through solid I = Q / t,

I = neAL/ t

$I = neA v_d$ as $v_d = L / t$

Current density J = I / A

Therefore, $J = nev_d$

Also, we know $J = \sigma E$

Therefore $\sigma E = nev_d$

But, $\mu = v_d / E$

Therefore $\sigma = ne\mu$

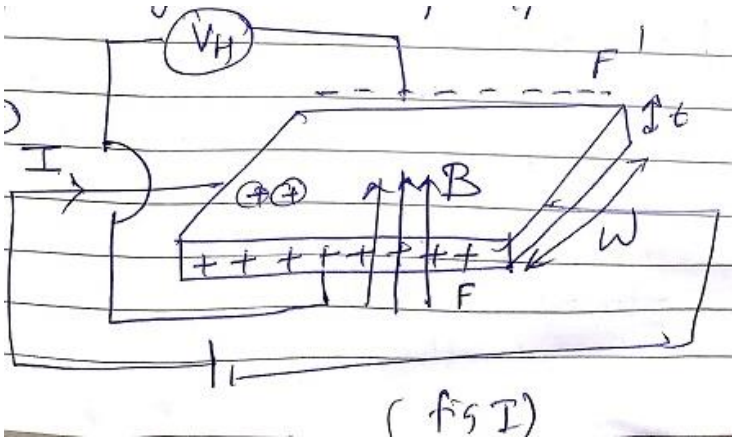
Q 7. State Hall Effect. Derive an expression for Hall Voltage, hall coefficient and Hall angle.

ANS: If a metal or S/C carrying current 'I' is placed in a transverse magnetic field, then potential difference is produced in the direction normal to both current and field. This phenomenon is called Hall Effect.

Let us consider a rectangular plate of p type S/C. when a potential difference is applied across its end a current of strength 'I' flows through it in x direction. Holes are majority charge carrier I p type S/C

Therefore $I = peAv_d$

$J = pev_d$



When magnetic field is not applied, holes move in an orderly way parallel to F and F'. But on the application of magnetic field 'B', holes experience side way deflection due to Lorentz force F_L..

Because of this force, holes are deflected towards front ‘F’ and pile up there. As the holes pile up on the front face, equal and opposite charge is left on the rear face. As a result an electric field is produced across F and F’. The direction of which is from F to F’. It is as such that it opposes further piling of holes on front face. A condition of equilibrium is reached when force due to electric field balances force due to magnetic field and again holes flow along the axis.

For equilibrium,

$F_E = F_L$

i.e $eE_H = eBv_d$

$V_H / w = B.J_x / pe$

Therefore $V_H = w\ B.J_x / pe$ OR $V_H = wBI / Ape$

$A = w \times t$

Therefore, $V_H = BI / pet$

Hall voltage is areal voltage and can be measured by a voltmeter. Hall coefficient R_H is defined as hall field per unit current density per unit magnetic field.

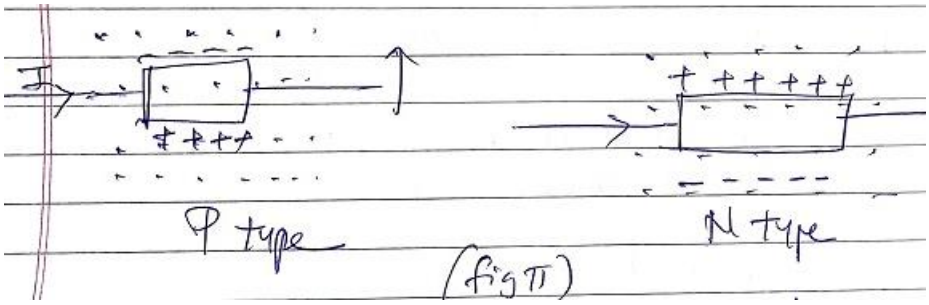
$R_H = E_H / J_X . B$

Therefore, $R_H = V_H / w / J_X . B$

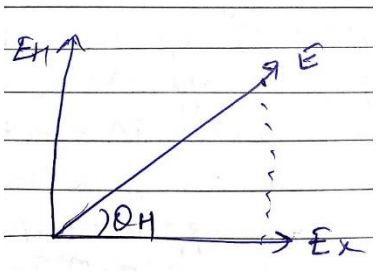
$R_H = B.J_x / pe / J_X . B$

$R_H = 1/ pe$ or $R_H = -1/ ne$

With the same direction of B and I as shown in figure if hall voltage is negative then it is ‘n’ type S/C.



The net Electric field E is a vector sum of E_x and E_H and act at an angle Θ_H w.r.t x axis.



tan $\Theta_H = E_H / E_X$

tan $\Theta_H = V_H / w \ / J_X.\rho$

tan $\Theta_H = B/pe\rho$

tan $\Theta_H = (R_H.\sigma)\ .B$

tan $\Theta_H = \mu_H.B$

where $\mu_H = R_H.\sigma$

Application:

- To determine type of semiconductor
- To determine charge carrier concentration
- To determine mobility if conductivity is known
- To determine magnetic field

Q 8 Show that ratio of Hall field to electric field E in n type S/C wafer is given by $E_H / E = B/ne\rho$

ANS: we know, $V_H = w\ B.J_x / ne$

i.e $V_H / w = B.J_x / pe$

also $J_X = \sigma E$ and $V_H / w = E_H$

therefore $E_H = B\sigma E/ne$

therefore $E_H /E = B/ne\rho$

Q9. Obtain the expression for conductivity in intrinsic and extrinsic S/C?

ANS: Intrinsic conductivity:

The current in S/C is composed of two current viz electron drifting in CB and holes drifting in VB

Therefore $I = I_e + I_h$

i.e $J = J_e + J_h$

We know $J = \sigma E$

Therefore $J = (\sigma_e + \sigma_h) E$

$$J = ne\mu_e E + pe \mu_h E$$

For intrinsic semiconductor $n = p = n_i$

Therefore, $J = n_i e (\mu_e + \mu_h) E$

Where $\sigma = n_i e (\mu_e + \mu_h)$

For extrinsic semiconductor:

N type: $n_n = N_D + P_n$

But $n_n >> P_n$

Therefore $n_n = N_D$

Therefore extrinsic conductivity $\sigma_n = ne \mu_e$

or $\sigma_n = N_D .e.\mu_e$

P type: $P_p = N_A + n_p$

But $P_p >> n_p$

$P_p = N_A$

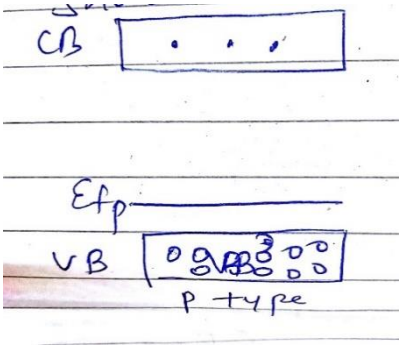
Therefore extrinsic conductivity, $\sigma_p = P. e. \mu_h$

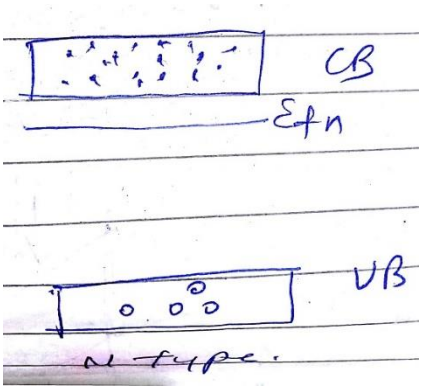
$\sigma_p = N_A . e.\mu_h$

Q 10 . Explain P-N Junction diode with the help of energy band diagram.

ANS: A junction between P type and N type S/C is called PN junction. It may be formed from a single crystal by doping part of it with acceptor impurities and remaining with donors.

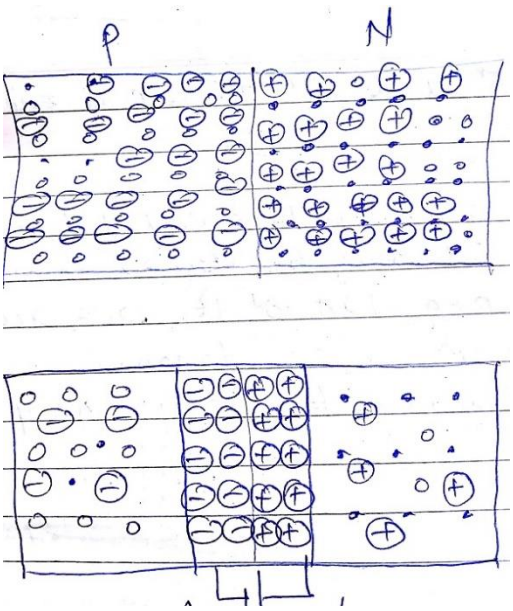
Energy band diagram for P type and n type S/C are shown below.

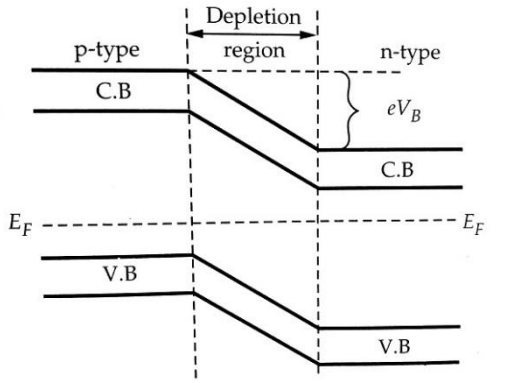




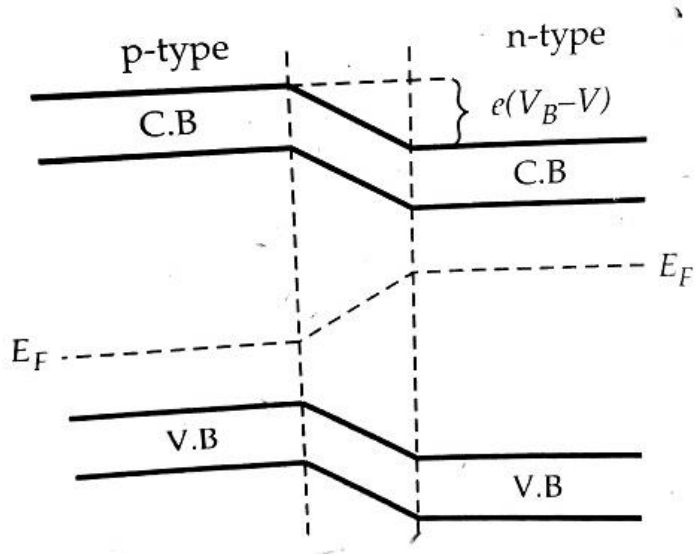
The Fermi level E_{FP} and E_{Fn} are at different levels. At the instant of joining the levels E_{Fp} and E_{fn} in the two S/Cs are not aligned. The probability of occupancy of energy levels in CB on N Side is high while it is low in P side. Therefore, the electrons occupying the level in CB on N side tends to move into CB level on P side. As electrons leave 'N 'region, E_{Fn} moves downward. Since the fermilevel is fixed relative to band structure of the region its movement causes downward shift of entire band structure on N side.

Similarly, the probability of occupancy in VB levels by holes on P side is high whereas it is low in N side. As a result holes tend to migrate into VB level on N side. As the holes leaves the region fermilevel E_{Fp} shifts upward because the direction of decrease in hole energy is upwards. The shifting of energy band continues till E_{Fp} and E_{Fn} are aligned. When they come to same level, the carrier migration ceases and equilibrium is achieved.



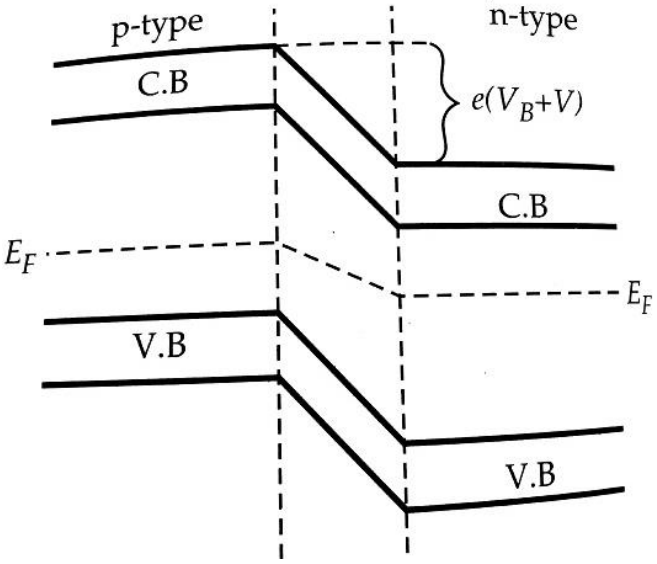


FORWARD BIAS:



Forward biasing increases the electron density in CB of n side. As a result fermilevel E_{Fn} moves upwards. Similarly due to the increase in hole density in VB of p side the Fermi level E_{Fp} moves downwards. The Fermi levels E_{Fn} and E_{Fp} are displaced relatively by an amount equal to the applied voltage.

REVERSE BIASED PN JUNCTION:



The diode is said to be Reversed biased when p type is connected to negative terminal and n type to positive terminal of battery. The externally applied field is now in the same direction as the internal field. Holes and electrons are attracted towards the respective terminals of battery as

a result width of deletion layer increases. This does not allow diffusion of majority carriers but minority can drift across the junction.

The negative terminal supplies electrons to p type which raises the Fermi level. The positive terminal takes away free electrons from n type which lowers the Fermi level.

Q 11. Explain principle, construction, advantages, demerits and application of LED?

ANS: LED: (light emitting diode)

Light emitting diode is a pn junction that under appropriate forward bias circumstances can serve as a light emitter. LED can emit spontaneous radiation in the visible, UV, IR region of Electromagnetic spectrum.

When electron recombines with holes the energy is emitted which is called as activation energy. In certain s/c like Ge, Si, energy released in electron hole recombination is given off in the form of heat but there are other S/C like GaAs, GaP, GaAsP, where energy release in electron hole pair recombination is given off in the optical region. Such s/c are used for the LEDs.

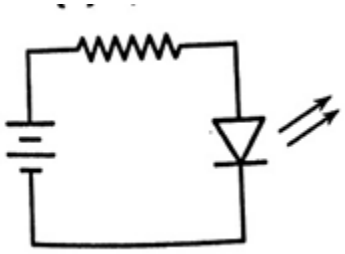
Principle:

The main principle of LED is electroluminescence. luminencsce means emission of optical radiation as a result of electronic excitation of a material. In electroluminescence the source of I/P energy is electric field or current.

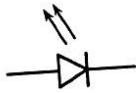
Construction:

LEDs are constructed by depositing S/c layer on the substrate. The active region exists between p and n region. As electron hole recombine light emerge out through the active region but in all the direction. So, to avoid this, it is placed in a small reflective cup so as to focus the light in the desired direction.

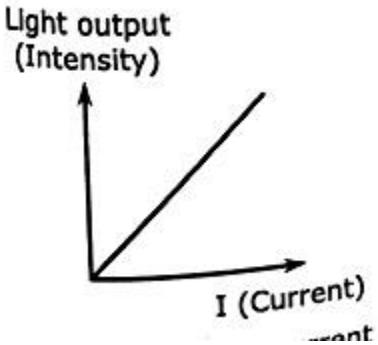
LED emits light only in Forward Bias condition.



Symbol



The output light varies linearly with the forward current



An eye is only sensitive to light of energy.

When LEDs are forward biased, the electron in n region cross the junction and recombine with the hole in p region with the release of energy in the form of photon. That energy of photon is equal to the energy of band gap.

$Eg = h\vartheta$ $Eg = hc/\lambda$

As an eye is only sensitive to light of energy $h\vartheta \geq 1.8$ ev, S/C with the band gap greater than 1.8ev are chosen for the LED.

For example Eg =2.25 ev which is for Gap then λ = 6.634 X 10 -34 X 3X 10 8 / 2.25 ev

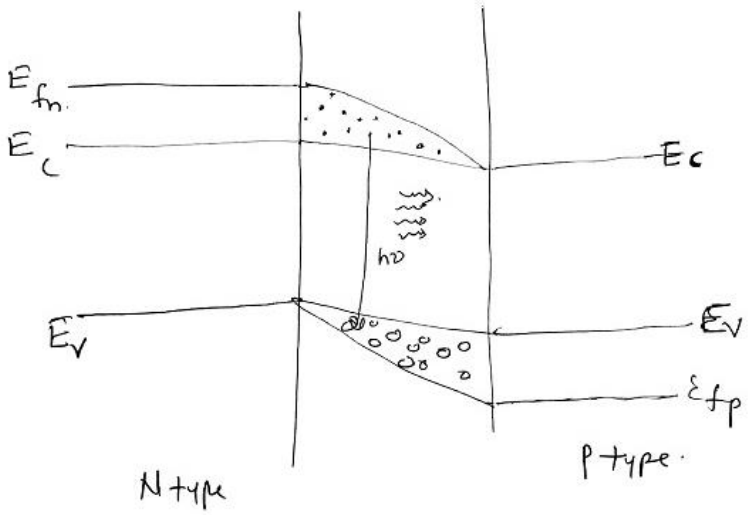
Λ = 5511 Å (green color)

That means gap emits green light. The color of emitted light is decided by its wavelength which depends on the band gap of the material

GaAs ---------- IR region

GaAsP ---------- Red or Yellow

GaP ---------- Green



Advantages of LED

- LEDs are small in size, light in weight
- Available in different color
- They have long life
- They are suitable for high operational speed
- They can be easily interfaced with other electronic circuits
- Since the output light is proportional to the current flowing through it. The brightness can be controlled by varying current flowing through it.

Disadvantages of LED

Over current can damage it

Output power can be affected by change in temperature

Efficiency of LED is low

APPLICATION:

1. IR LED s are used in remote control devices
2. They can be used a indicators in various electronic circuits
3. In seven segment or alpha numeric display
4. In the optocouplers

5. In on-off switches in most electrical appliances
6. In fiber optic communication, LEDs are often used as an optical source.

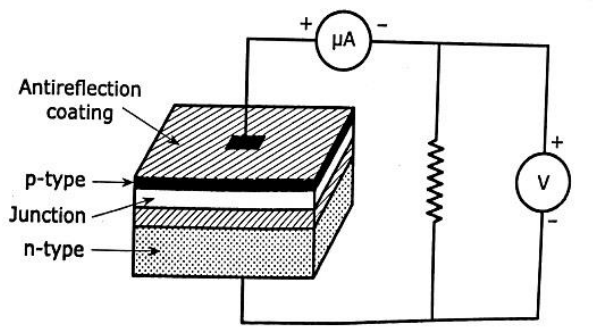
Q 12. What is photovoltaic effect? Explain the principle and working of Solar cell?

ANS:

Certain materials produce small amount of voltage when exposed to light. This phenomenon is called as photovoltaic effect is different than photoelectric effect. In photoelectric effect, when radiation is incident on the surface electrons are ejected from the surface.

Solar cell is a S/C device based on the principle of photovoltaic effect. It converts incident sunlight into electricity.

AS photovoltaic or solar cell generally consists of a P-N junction in which an ‘n ‘region is diffused onto a base ‘p’ region or vice versa. The doping is very high. The top layer is very thin so that the incident light falls into junction. Additionally, the top layer is coated with anti reflecting film to minimize reflection of incident solar radiation.



When sunlight falls on the solar cell the photon with energy hϑ greater than the forbidden energy gap Eg of the semiconducting material generates more electrons holes pairs in the depletion region. The internal built in potential barrier creates a field that assists the photo generated carriers in the vicinity of the junction to cross the junction. This give rise to a voltage at the junction called as photo voltage.

A solar cell generates a net potential of about 0.6ev, by connecting several solar cells in series a desired voltage can be obtained.

Advantage of solar cell

- Solar energy is nonconventional source of energy as no fuel is used to generate electrical energy
- It is a clean source of energy

- Pollution free
- Suitable for low power application like calculator
- Maintenance free which makes cost effective
- Useful in remote area where no other source of energy can be frequently transported.

Disadvantages

1. For high power application, requires large space and is costly.
2. Affected by availability of sunlight that varies from day to night, place to lace, season to season
3. Efficiency is low

Application:

1. Solar cells are used in battery charging system
2. Few countries USA, Germany have photovoltaic power plants
3. Solar cells are used in satellite, space vehicle and in remote places as a source of energy.

Q13. Explain various breakdown mechanisms?

An ordinary PN Junction normally does not conduct when it is reverse biased. If the reverse bias is increased a point is reached when the junction breaks down and starts conducting heavily. The critical value of the voltage is called the breakdown voltage of the junction.

Once the breakdown occurs very small increase in voltage causes a large change in reverse current. The resistance offered by the Junction will be nearly zero at this point. Breakdown should be avoided as it permanently damages the crystal structure of two regions and renders the junction useless.

The breakdown voltage depends on the width of depletion region which in turn depends on the doping level of p and n region.

The large current at breakdown is caused by to mechanisms – Avalanche effect and zener effect.

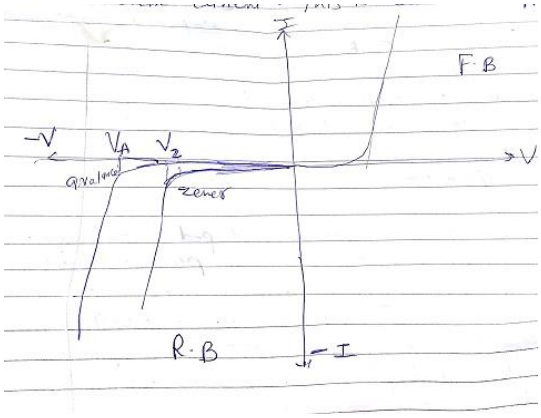
1. Avalanche effect:

When p and n regions are lightly doped, a breakdown due to avalanche effect can take place in it. The reverse bias voltage accelerates minority carriers across the junction. The velocity of minority carriers is proportional to the applied bias voltage. Hence at high voltage, the minority carriers are accelerated to such an extent that they acquire sufficient kinetic energy to knock off the electrons from atoms in the depletion region. The process generates mobile electron hole pairs, which in turn gets accelerated by the electric field and causes further ionization of more

atoms. Such cumulative action leads to avalanche of charge carriers and leads to a sharp rise in the reverse current.

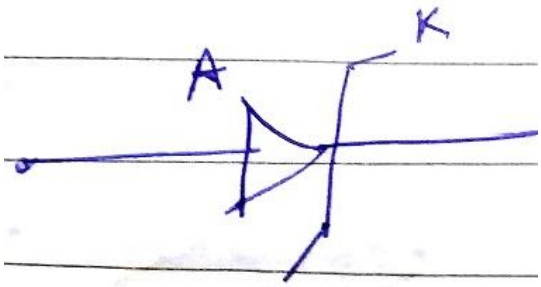
2. Zener breakdown:

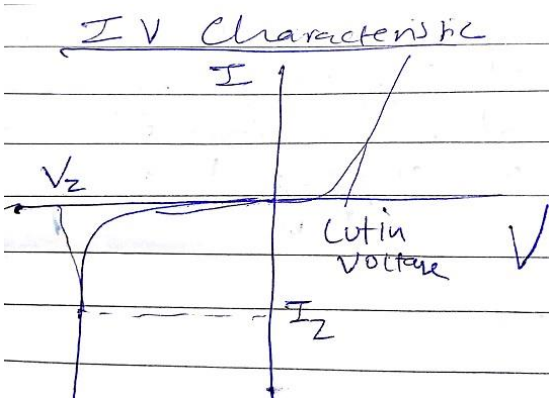
When p and n region are heavily doped, the depletion layer at the junction will be narrow. This breakdown occurs in a heavily doped PN junction which requires a relatively low reverse voltage. In reverse biasing barrier is narrow and thus under the effect of even a small reverse bias, electron can tunnel through it causing a sudden large reverse current. This is called Zener breakdown.



Q 14. Explain Zener diode as a voltage regulator?

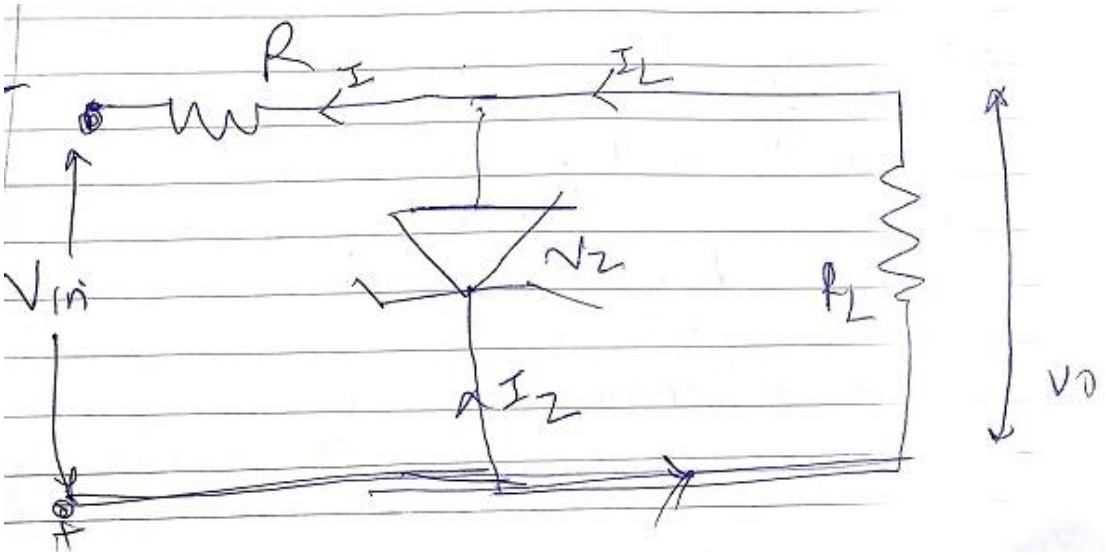
ANS: Zener diode is a junction formed by combining highly doped PN junction semiconductor. It works on a principle of Zener breakdown and is operated in reverse breakdown region. In reverse breakdown region high current flows through the diode leading to high power dissipation. Hence Zener diodes are provided with adequate power dissipation capabilities to operate in reverse breakdown region.





When reverse bias is applied across the diode electric field is generated by uncovered charges at the depletion region. The electric field intensity across junction increases as doping levels are increased.

This field exerts a sufficiently strong force on a bound electron enough to tear it out its covalent bond. The new electron hole pair created increases reverse current and actually enters breakdown region. This process is called Zener breakdown. It occurs at a voltage much less than the avalanche breakdown voltage. The reverse voltage across the diode is almost independent of current flowing through it except for small variation quantified by dynamic resistance of Zener diode. That means if we connect a load across the Zener diode with a resistance and supply voltage. It will provide almost constant voltage across the load independent of load and supply voltage variation. This means Zener diode acts as a voltage regulator. The minimum current that should be allowed through Zener diode to ensure that it is in breakdown region is called knee current. For current lower than knee current, regulation will be poor.



Application:

Used as voltage regulator

Switching application

Used in over voltage protection circuits

Clipping and clamping circuits.

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