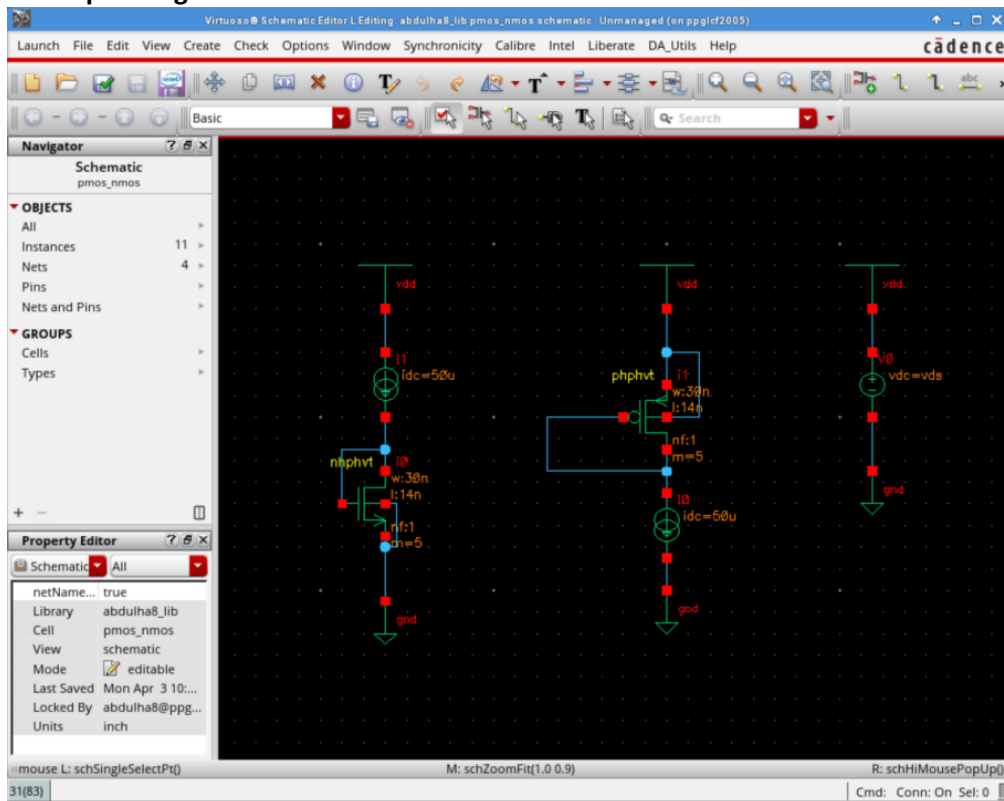


Specifications:

- VDD = 1.8V
- $A_v \geq 70\text{dB}$
- $CL = 10\text{pF}$
- $PM = 60^\circ$
- $SR = 10\text{V}/\mu\text{s}$
- $ICMR^+ = 1.6\text{V}$
- $ICMR^- = 1\text{V}$
- $GB \geq 10\text{MHz}$

Dc – Operating Points



NMOS:

- $W/L=30n*5/14n$ (mult of 2)
- $\beta_{eff} = \mu_n C_{ox}(W/L) = 1.737\text{m}$
- $1.72\text{m} = \mu_n C_{ox} (30*5/14)$
- $\mu_n C_{ox} = 1.737\text{m}/10.71 = 162.18u$
- $V_{thn} = 366\text{mV}$

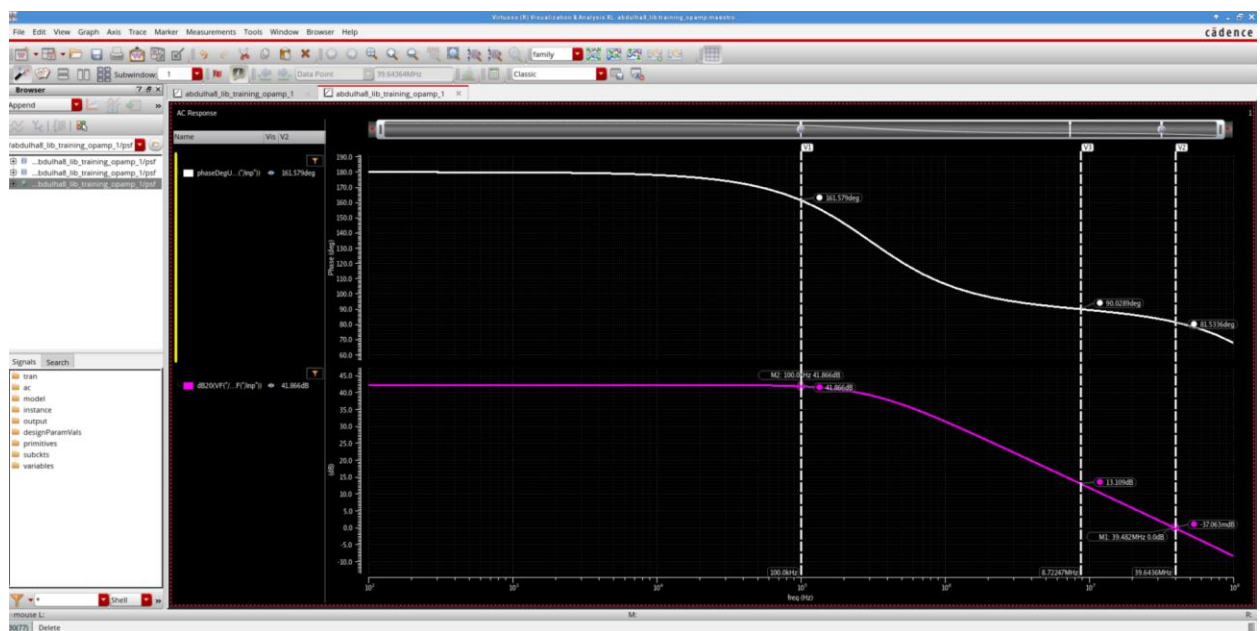
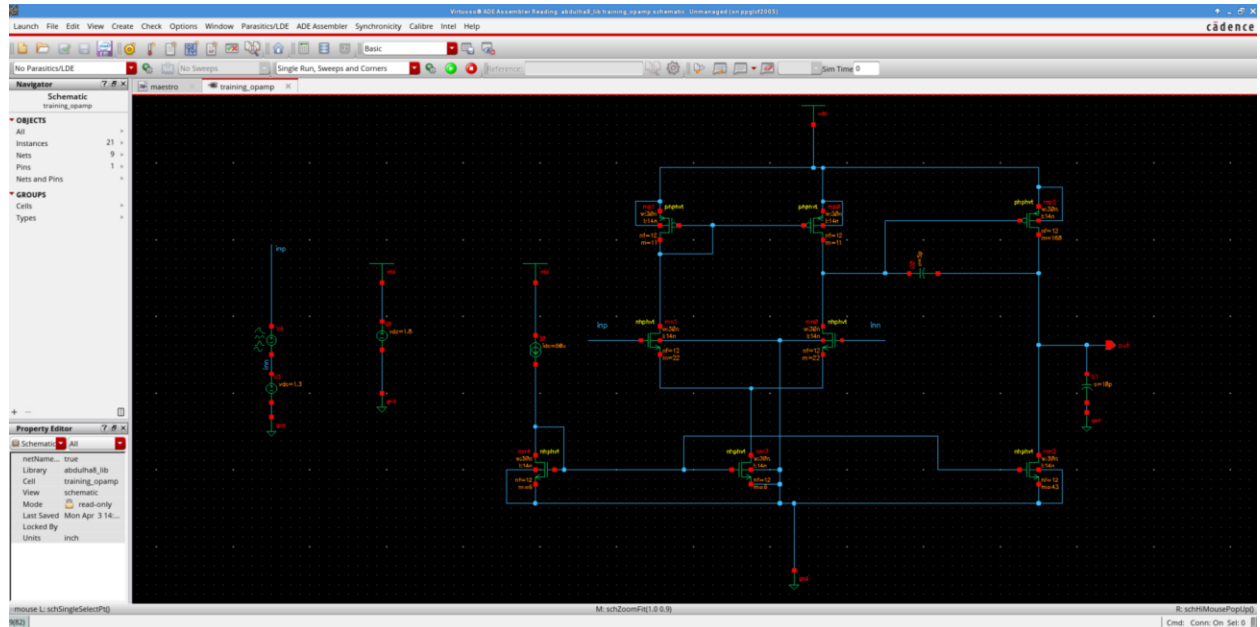
PMOS:

- $W/L = 30n \cdot 5 / 14n$ (mult of 5)
- $\beta_{eff} = \mu_p C_{ox}(W/L) = 1.727m$
- $1.476m = \mu_p C_{ox} (30n \cdot 5 / 14n)$
- $\mu_p C_{ox} = 1.727m / 10.71 = 161.25u$
- $V_{thp} = 335.9mV$

Design of Two Stages Op-Amp based on the Specs:

- $C_c = 0.22 C_L$, $C_c > 2.2pF$, $C_c = 5pF$
- $I_5 = SR \cdot CC$
- $I_5 = 10/1\mu \cdot 5p = 50\mu A$
- $gm_{1,2} = GB \times CC \times 2\pi$
- $gm_{1,2} = 10M \times 5pF \times 2\pi$
- $gm_{1,2} = 314.15\mu$
- $(W/L)_{1,2} = (314.15\mu)^2 / 2(25\mu) \cdot (162.18u) = 12.17 \approx 12$
- $(W/L)_{3,4} = \frac{2(25)}{161.25(1.8 - 1.6 - 335.9mV + 366mV)^2} = 5.85 \approx 6$
- $V_{DSAT5} \geq 1 - \sqrt{\frac{2(25)}{(162.18)(12)}} - 0.366 = 0.4737 \approx 0.5$
- $(W/L)_5 = \frac{2(50)}{(162.18)(0.5)^2} = 2.378 \approx 2.4$
- $gm_6 = 10(314.15\mu) = 3.1415m$
- $gm_4 = \sqrt{2(25) * 161.25u * 6} = 219.9 \mu$
- $(W/L)_6 = \frac{3.1415m}{219.9 \mu} * 2 = 28.57 \approx 29$

- $I_{6,7} = 10 \times 29/6 = 48.33\mu\text{A}$
- $(W/L)_7 = \frac{48.33}{50} \times 2.4 = 2.319$



Gain = 41.86dB

