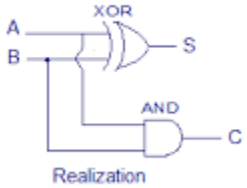
1) Implementation of half adder using gate level modeling.

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Truth table

Schematic



Realization

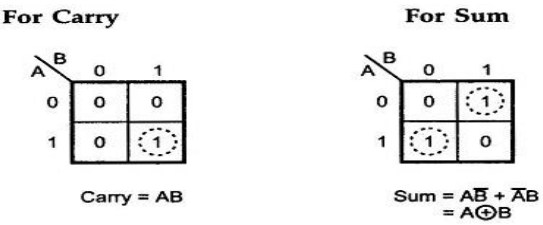


Fig. 3.12 Maps for half-adder

DESIGN:

```
module HA(
input a,
input b,
output c_out,
output sum);

  xor x1(sum,a,b);
  and A1(c_out,a,b);

endmodule
```

Testbench:

```
//2Q. gate level implementation of half adder [test bench)
module tb;

  reg in1,in2;
  wire  sum;
  wire carry;

  HA h1 ( .sum(sum), .b(in2),.a(in1),.c_out(carry));

  initial begin
      $monitor (" %b + %b = %b =%d",in1,in2,{carry,sum},{carry,sum});
      {in1,in2}=2'b00; #10;
      {in1,in2}=2'b01; #10;
      {in1,in2}=2'b10; #10;
      {in1,in2}=2'b11; #10;
  end
endmodule
```

run.do

```
# cd {C:\Users\alisy\Documents\verilog\class1\Q02_half adder}
#environment creation
vlib work

#compilation
vlog HA_G.v
vlog HA_G_tb.v

#simulation
vsim work.tb
run -all
```