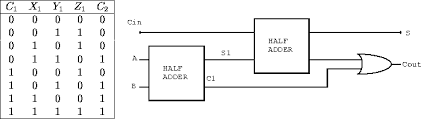
1. Implementation of Fulladder using half adders



**Design:**

module FA ( input a,

input b,

input c\_in,

output sum,

output c\_out

);

HA h1( .a(a),

.b(b),

.c\_out(w2),

.sum(w1));

HA h2( .a(w1),

.b(c\_in),

.c\_out(w3),

.sum(sum) );

or o1(c\_out,w2,w3);

endmodule

**TestBench:**

module tb;

reg in1,in2,c\_in;

wire sum;

wire carry;

integer i;

FA f1 (

.a(in1),

.b(in2),

.c\_in(c\_in),

.sum(sum),

.c\_out(carry)

);

initial begin

$monitor (" %b + %b + %b = %b = %d",in1,in2,c\_in,{carry,sum},{carry,sum});

for (i=0;i<8;i=i+1) begin

{in1,in2,c\_in}=i;

#10;

end

end

endmodule